Serially Controlled, 1.5 Ω, On-Resistance, High Voltage, *i*CMOS, Quad SPST Switch

Data Sheet

ADGS1412

FEATURES

- SPI interface with error detection
- Includes CRC, invalid read/write address, and SCLK count error detection
- Supports burst and daisy-chain mode
- Industry-standard SPI Mode 0 Interface-compatible
- 1.5 Ω typical on resistance at 25°C
- 0.3 Ω typical on-resistance flatness at 25°C
- 0.1 Ω typical on-resistance match between channels at 25°C
- Fully specified at ±15 V, ±5 V, and +12 V
- V_{SS} to V_{DD} analog signal range

APPLICATIONS

- Automated test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Audio signal routing
- Video signal routing
- Communications systems
- Relay replacement

GENERAL DESCRIPTION

The ADGS1412 contains four independent single-pole/single-throw (SPST) switches. An serial peripheral interface (SPI) controls the switches. The SPI interface has robust error detection features such as cyclic redundancy check (CRC) error detection, invalid read/write address detection, and SCLK count error detection.

It is possible to daisy-chain multiple ADGS1412 devices together. Daisy-chain mode enables the configuration of multiple devices with a minimal amount of digital lines. The ADGS1412 can also operate in burst mode to decrease the time between SPI commands.

*i*CMOS construction ensures ultralow power dissipation, making the device ideally suited for portable and battery-powered instruments.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The on-resistance profile is flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals.

FUNCTIONAL BLOCK DIAGRAMS

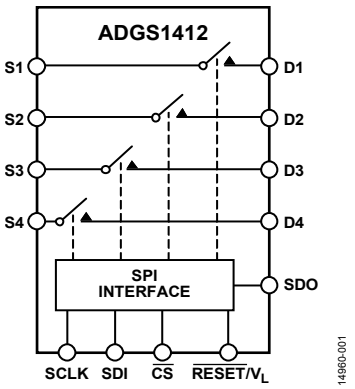

Figure 1.

PRODUCT HIGHLIGHTS

1. SPI interface removes the need for parallel conversion, logic traces and reduces GPIO channel count.
2. Daisy-chain mode removes additional logic traces when multiple devices are used.
3. CRC error detection, invalid read/write address detection, and SCLK count error detection ensures a robust digital interface.
4. CRC and error detection capabilities allow the use of the ADGS1412 in safety critical systems.
5. Minimum distortion.

Rev. A

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ADGS1412* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADGS1412 Evaluation Board

DOCUMENTATION

Data Sheet

- ADGS1412: Serially-Controlled, 1.5 Ω On Resistance High Voltage, iCMOS, Quad SPST Switch Data Sheet

User Guides

- UG-1067: Evaluation Board for ADGS1412 Serially Controlled, 1.5 Ω On Resistance, High Voltage, Quad SPST Switch

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADGS5412 - No-OS Driver

TOOLS AND SIMULATIONS

- ADGS1412 IBIS Model
- ADGS1412 SPICE Macro Model

DESIGN RESOURCES

- ADGS1412 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADGS1412 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

3/2017—Rev. 0 to Rev. A

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10/2016—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, V_L = 2.7 V to 5.5 V, and GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	1.5			Ω typ	V_S = ±10 V, I_S = −10 mA, see Figure 28
	1.8	2.3	2.6	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	0.3			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.03			nA typ	V_S = ±10 V, V_D = ∓ 10 V, see Figure 31
	±0.55	±2	±12.5	nA max	
Drain Off Leakage, I_D (Off)	±0.03			nA typ	V_S = ±10 V, V_D = ∓ 10 V, see Figure 31
	±0.55	±2	±12.5	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.15			nA typ	V_S = V_D = ±10 V, see Figure 27
	±2	±4	±30	nA max	
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2	V min	3.3 V < V_L ≤ 5.5 V
			1.35	V min	2.7 V ≤ V_L ≤ 3.3 V
Low, V_{INL}			0.8	V max	3.3 V < V_L ≤ 5.5 V
			0.8	V max	2.7 V ≤ V_L ≤ 3.3 V
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_L
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
Digital Output Capacitance, C_{OUT}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	115			ns typ	R_L = 300 Ω, C_L = 35 pF
	135	150	160	ns max	V_S = 10 V, see Figure 34
t_{OFF}	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	190	210	225	ns max	V_S = 10 V, see Figure 34
Charge Injection, Q_{INJ}	−20			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 35
Off Isolation	−76			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 30
Channel to Channel Crosstalk	−100			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 29
Total Harmonic Distortion + Noise	0.014			% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz, see Figure 32
−3 dB Bandwidth	170			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 33
Insertion Loss	−0.2			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
C_S (Off)	22			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	23			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	113			pF typ	V_S = 0 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			µA typ	All switches open
			1	µA max	
	220			µA typ	All switches closed, V_L = 5.5 V
			380	µA max	
	230			µA typ	All switches closed, V_L = 2.7 V
			380	µA max	
I_L					
Inactive	6.3			µA typ	Digital inputs = 0 V or V_L
			8.0	µA max	
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 5.5 V
		2	2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_L
			1.0	µA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, V_L = 2.7 V to 5.5 V, and GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	3.3			Ω typ	V_S = ±4.5 V, I_S = −10 mA, see Figure 28
	4	4.9	5.4	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.13			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.22	0.23	0.25	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	0.9			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	1.1	1.24	1.31	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.03			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V, see Figure 31
	±0.55	±2	±12.5	nA max	
Drain Off Leakage, I_D (Off)	±0.03			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V, see Figure 31
	±0.55	±2	±12.5	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.05			nA typ	V_S = V_D = ±4.5V, see Figure 27
	±1.0	±4	±30	nA max	
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2	V min	3.3 V < V_L ≤ 5.5 V
			1.35	V min	2.7 V ≤ V_L ≤ 3.3 V
Low, V_{INL}			0.8	V max	3.3 V < V_L ≤ 5.5 V
			0.8	V max	2.7 V ≤ V_L ≤ 3.3 V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Input Current, I_{INL} or I_{INH}	0.001			µA typ	$V_{IN} = V_{GND}$ or V_L
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
Digital Output Capacitance, C_{OUT}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	265			ns typ	R_L = 300 Ω, C_L = 35 pF
	350	390	430	ns max	V_S = 3 V, see Figure 34
t_{OFF}	280			ns typ	R_L = 300 Ω, C_L = 35 pF
	365	400	435	ns max	V_S = 3 V, see Figure 34
Charge Injection, Q_{INJ}	10			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 35
Off Isolation	−76			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 30
Channel to Channel Crosstalk	−100			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 29
Total Harmonic Distortion + Noise	0.03			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz, see Figure 32
−3 dB Bandwidth	130			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 33
Insertion Loss	−0.3			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
C_S (Off)	32			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	33			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	116			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_L, V_L = 5.5 V
			1.0	µA max	
	14			µA typ	All switches closed, V_L = 2.7 V
			20	µA max	
I_L					
Inactive	6.3			µA typ	Digital inputs = 0 V or V_L
			8.0	µA max	
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 5.5 V
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_L
			1.0	µA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L = 2.7 V to 5.5 V, and GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	2.8			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA, see Figure 28
	3.5	4.3	4.8	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.13			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.21	0.23	0.25	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	0.6			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1.1	1.2	1.3	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 31
	±0.55	±2	±12.5	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 31
	±0.55	±2	±12.5	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.15			nA typ	V_S = V_D = 1 V/10 V, see Figure 27
	±1.5	±4	±30	nA max	
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2	V min	3.3 V < V_L ≤ 5.5 V
			1.35	V min	2.7 V ≤ V_L ≤ 3.3 V
Low, V_{INL}			0.8	V max	3.3 V < V_L ≤ 5.5 V
			0.8	V max	2.7 V ≤ V_L ≤ 3.3 V
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_L
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
Digital Output Capacitance, C_{OUT}	4			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	190			ns typ	R_L = 300 Ω, C_L = 35 pF
	240	270	300	ns max	V_S = 8 V, see Figure 34
t_{OFF}	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	215	240	265	ns max	V_S = 8 V, see Figure 34
Charge Injection, Q_{INJ}	10			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 35
Off Isolation	−76			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 30
Channel to Channel Crosstalk	−100			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 29
Total Harmonic Distortion + Noise	0.06			% typ	R_L = 110 Ω, 6 V p-p, f = 20 Hz to 20 kHz, see Figure 32
−3 dB Bandwidth	130			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 33
Insertion Loss	−0.3			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
C_S (Off)	29			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	30			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	116			pF typ	V_S = 6 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			µA typ	All switches open
			1.0	µA max	
	220			µA typ	All switches closed, V_L = 5.5 V
			380	µA max	
	250			µA typ	All switches closed, V_L = 2.7 V
			430	µA max	
I_L					
Inactive	6.3			µA typ	Digital inputs = 0 V or V_L
			8.0	µA max	
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 5.5 V
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and V_L, V_L = 2.7 V
			1.0	mA max	
V_{DD}			5/20	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 4. Four Channels On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx[1]				
V_{DD} = 15 V, V_{SS} = −15 V (θ_{JA} = 54°C/W)	297	165	79	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V (θ_{JA} = 54°C/W)	240	142	74	mA maximum
V_{DD} = 5 V, V_{SS} = −5 V (θ_{JA} = 54°C/W)	224	135	72	mA maximum

[1] Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

Table 5. One Channel On

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx[1]				
V_{DD} = 15 V, V_{SS} = −15 V (θ_{JA} = 54°C/W)	531	235	87	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V (θ_{JA} = 54°C/W)	433	210	85	mA maximum
V_{DD} = 5 V, V_{SS} = −5 V (θ_{JA} = 54°C/W)	404	202	84	mA maximum

[1] Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

TIMING CHARACTERISTICS

V_L = 2.7 V to 5.5 V, GND = 0 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterization, not production tested.

Table 6.

Parameter	Limit	Unit	Test Conditions/Comments
TIMING CHARACTRISTICS			
t_1	20	ns min	SCLK period
t_2	8	ns min	SCLK high pulse width
t_3	8	ns min	SCLK low pulse width
t_4	10	ns min	$\overline{CS}$ falling edge to SCLK active edge
t_5	6	ns min	Data setup time
t_6	8	ns min	Data hold time

Parameter	Limit	Unit	Test Conditions/Comments
t_7	10	ns min	SCLK active edge to $\overline{CS}$ rising edge
t_8	20	ns max	$\overline{CS}$ falling edge to SDO data available
t_9[1]	20	ns max	SCLK falling edge to SDO data available
t_{10}	20	ns max	$\overline{CS}$ rising edge to SDO returns to high impedance
t_{11}	20	ns min	$\overline{CS}$ high time between SPI commands
t_{12}	8	ns min	$\overline{CS}$ falling edge to SCLK becomes stable
t_{13}	8	ns min	$\overline{CS}$ rising edge to SCLK becomes stable

[1] Measured with the 1 kΩ pull-up resistor to V_L and 20 pF load. t_9 determines the maximum SCLK frequency when SDO is used.

Timing Diagrams

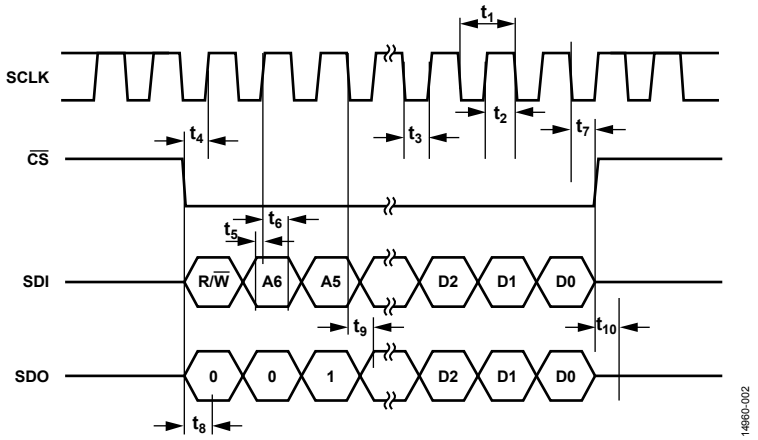

Figure 2. Address Mode Timing Diagram

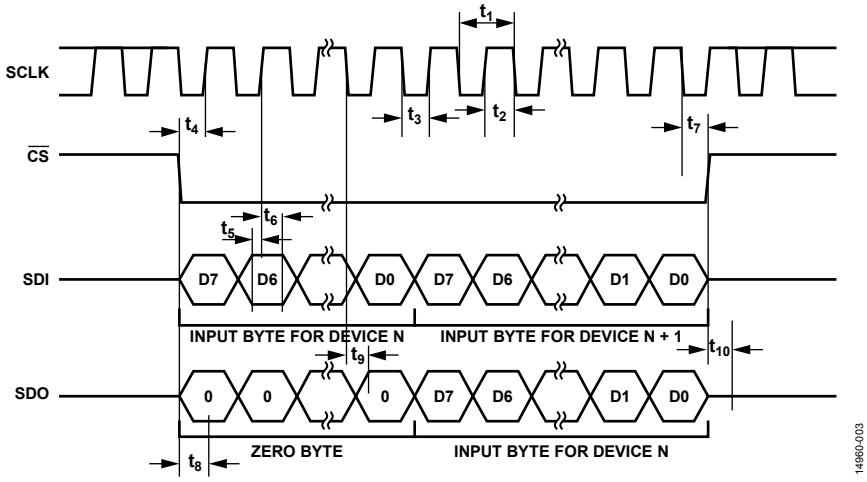

Figure 3. Daisy Chain Timing Diagram

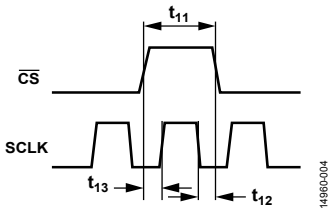

Figure 4. SCLK/$\overline{CS}$ Timing Relationship

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to +5.75 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	−0.3 V to +5.75 V
Peak Current, Sx or Dx Pins[2]	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2, 3]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

[1] Overvoltages at the digital Sx and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.
[3] See Table 4 and Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JCB}[1]	Unit
CP-24-17[2]	54	3	°C/W

[1] θ_{JCB} is the junction to the bottom of the case value.
[2] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

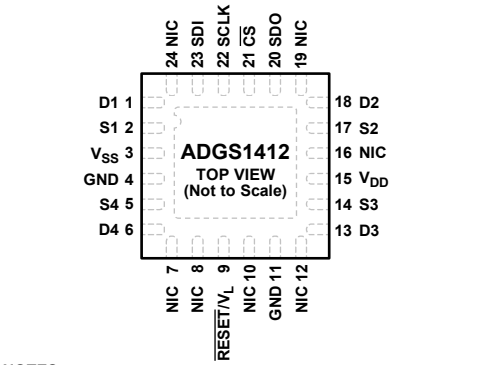

Figure 5. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D1	Drain Terminal 1. This pin can be an input or output.
2	S1	Source Terminal 1. This pin can be an input or output.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, tie this pin to ground.
4, 11	GND	Ground (0 V) Reference.
5	S4	Source Terminal 4. This pin can be an input or output.
6	D4	Drain Terminal 4. This pin can be an input or output.
7, 8, 10, 12, 16, 19, 24	NIC	Not Internally Connected.
9	$\overline{RESET}/V_L$	$\overline{RESET}$/Logic Power Supply Input (V_L). Under normal operation, drive the $\overline{RESET}/V_L$ pin with a 2.7 V to 5.5 V supply. Pull the $\overline{RESET}$ pin low to complete a hardware reset. After a reset, all switches open, and the appropriate registers are set to their default.
13	D3	Drain Terminal 3. This pin can be an input or output.
14	S3	Source Terminal 3. This pin can be an input or output.
15	V_{DD}	Most Positive Power Supply Potential.
17	S2	Source Terminal 2. This pin can be an input or output.
18	D2	Drain Terminal 2. This pin can be an input or output.
20	SDO	Serial Data Output. This pin can be used for daisy chaining a number of these devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK. Pull this open-drain output to V_L with an external resistor.
21	$\overline{CS}$	Active Low Control Input. $\overline{CS}$ is the frame synchronization signal for the input data.
22	SCLK	Serial Clock Input. Data is captured on the positive edge of SCLK. Data can be transferred at rates of up to 50 MHz.
23	SDI	Serial Data Input. Data is captured on the positive edge of the serial clock input.
	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the substrate, V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

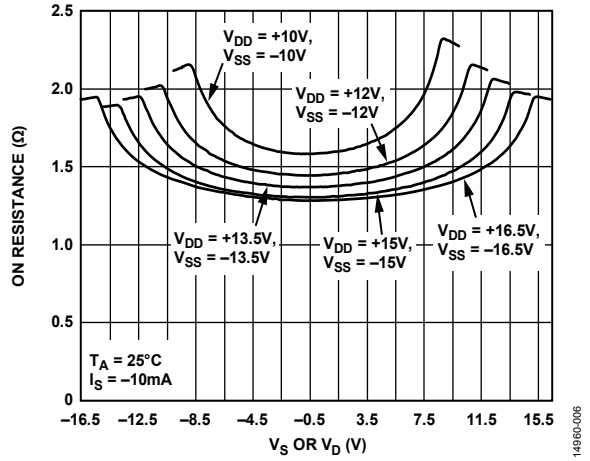

Figure 6. On Resistance vs. V_S or V_D for Various Dual Supplies

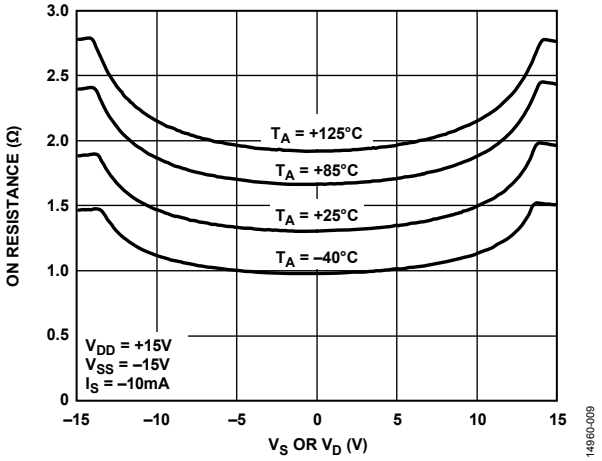

Figure 9. On Resistance vs. V_S or V_D for Various Temperatures, ±15 V Dual Supply

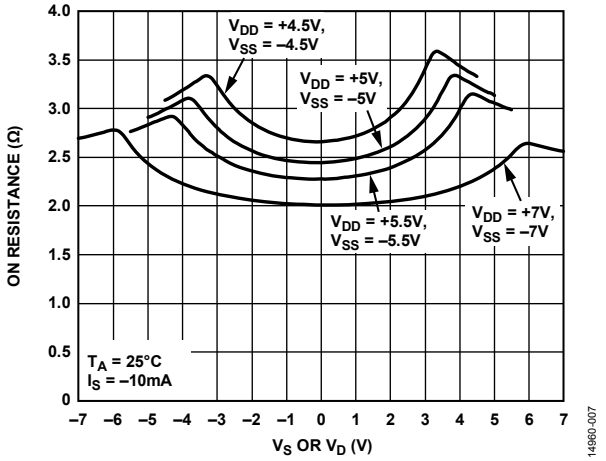

Figure 7. On Resistance vs. V_S or V_D for Various Dual Supplies

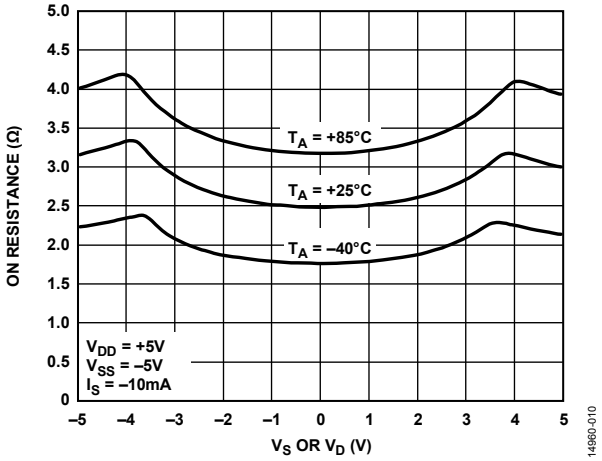

Figure 10. On Resistance vs. V_S or V_D for Various Temperatures, ±5 V Dual Supply

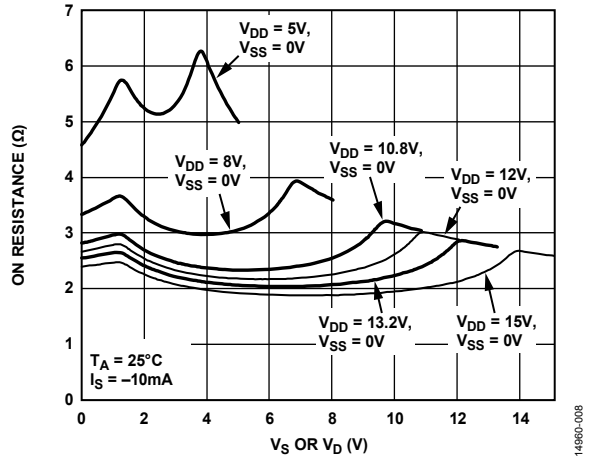

Figure 8. On Resistance vs. V_S or V_D for Various Single Supplies

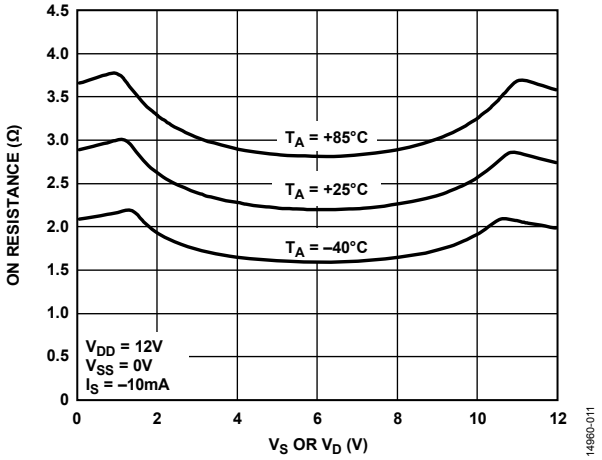

Figure 11. On Resistance vs. V_S or V_D for Various Temperatures, 12 V Single Supply

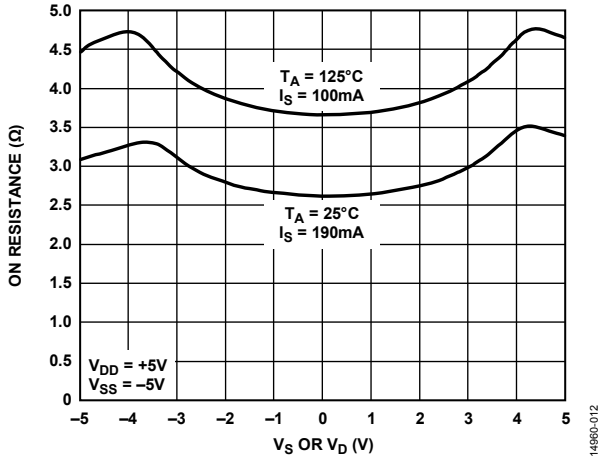

Figure 12. On Resistance vs. V_S or V_D for Various Current Levels and Temperatures, ±5 V Dual Supply

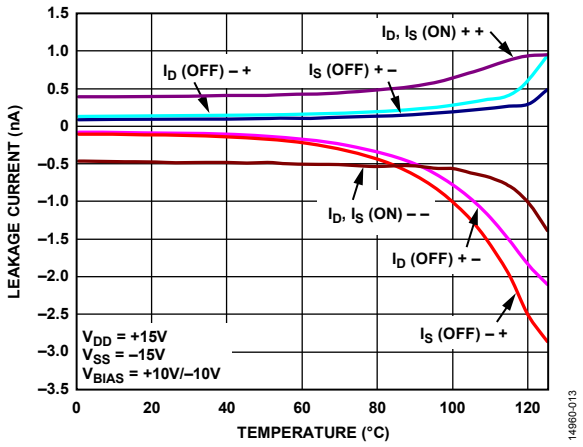

Figure 13. Leakage Current vs. Temperature, ±15 V Dual Supply

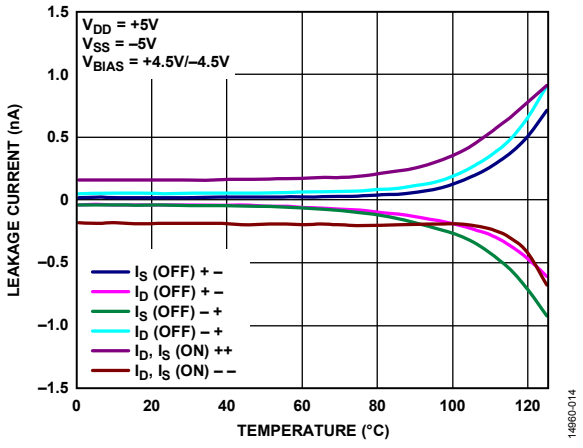

Figure 14. Leakage Current vs. Temperature, ±5 V Dual Supply

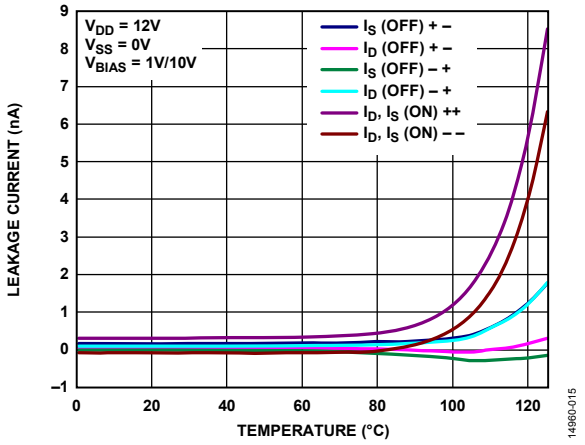

Figure 15. Leakage Current vs. Temperature, 12 V Single Supply

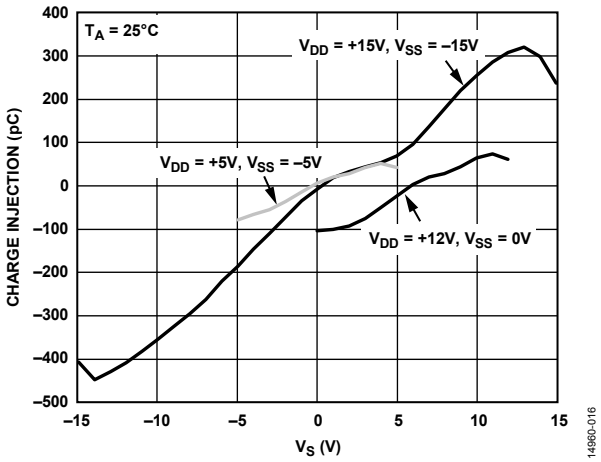

Figure 16. Charge Injection vs. Source Voltage (V_S)

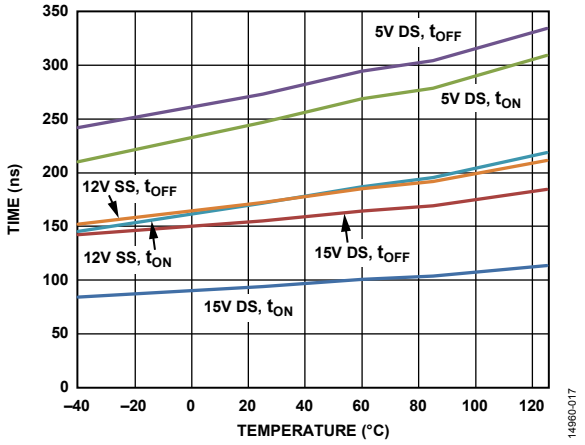

Figure 17. t_{ON}/t_{OFF} Time vs. Temperature for Single Supply (SS) and Dual Supply (DS)

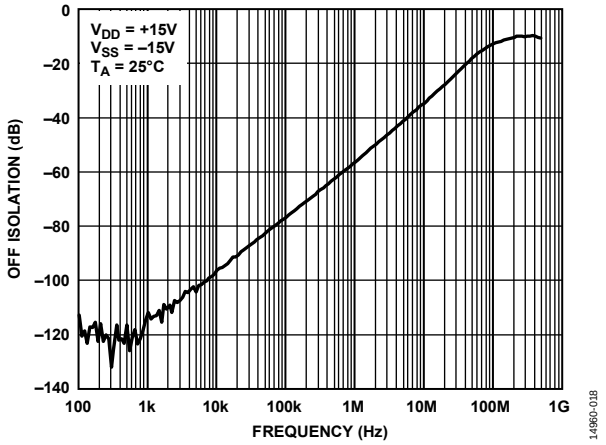

Figure 18. Off Isolation vs. Frequency, ±15 V Dual Supply

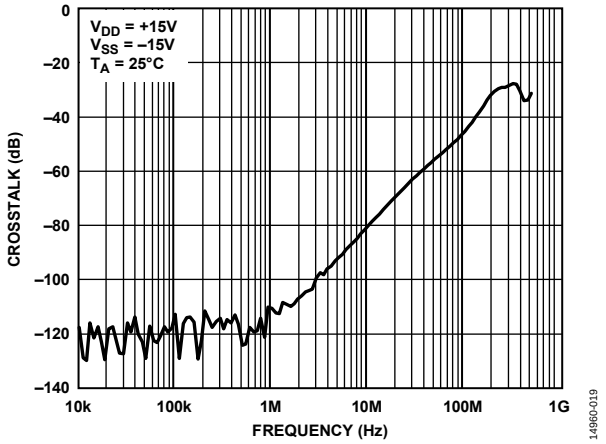

Figure 19. Crosstalk vs. Frequency, ±15 V Dual Supply

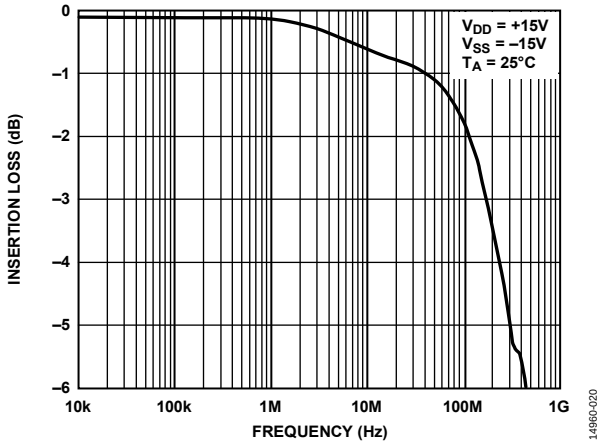

Figure 20. Insertion Loss vs. Frequency, ±15 V Dual Supply

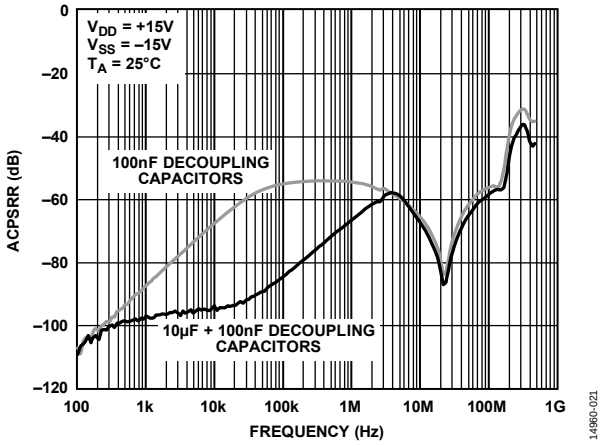

Figure 21. AC Power Supply Rejection Ratio (ACPSRR) vs. Frequency, ±15 V Dual Supply

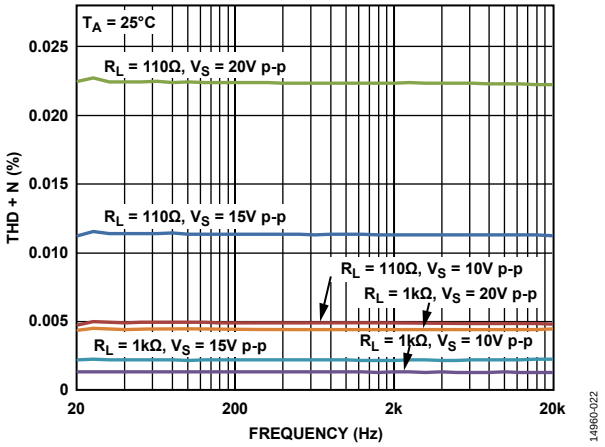

Figure 22. THD + N vs. Frequency, ±15 V Dual Supply

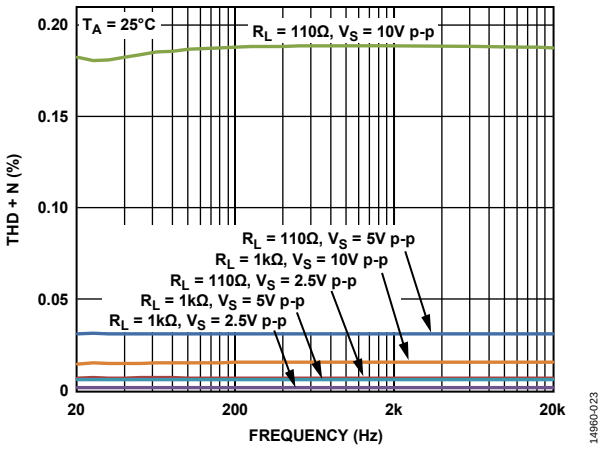

Figure 23. THD + N vs. Frequency, ±5 V Dual Supply

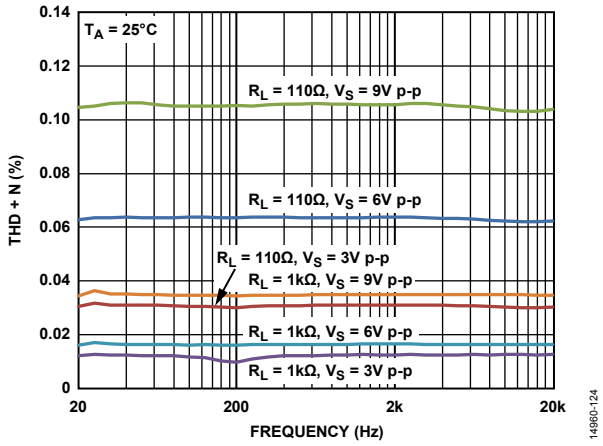

Figure 24 . THD + N vs. Frequency, 12 V Single Supply

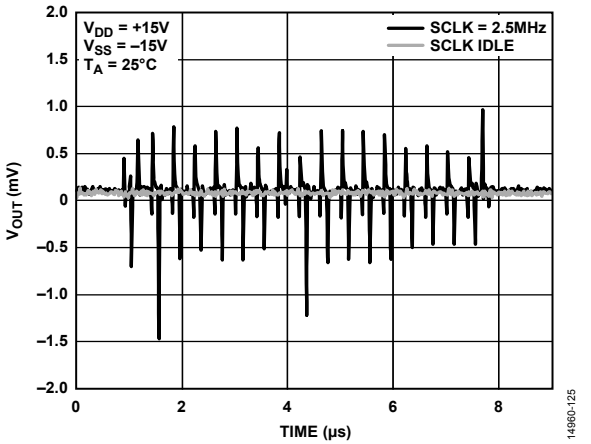

Figure 25. Digital Feedthrough

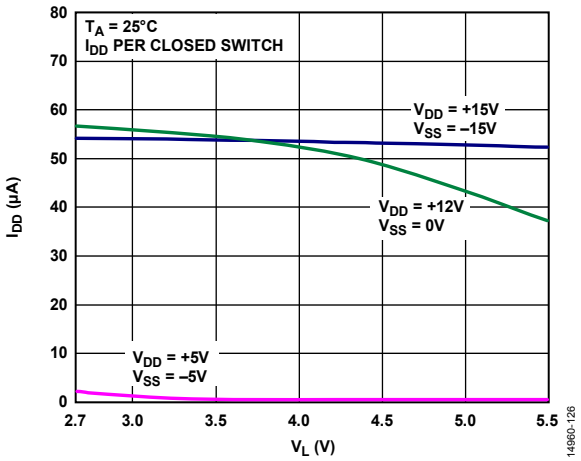

Figure 26. I_{DD} vs. V_L

TEST CIRCUITS

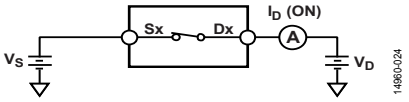

Figure 27. On Leakage

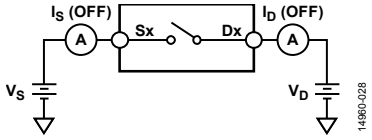

Figure 31. Off Leakage

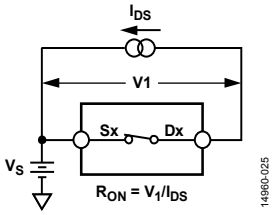

Figure 28. On Resistance

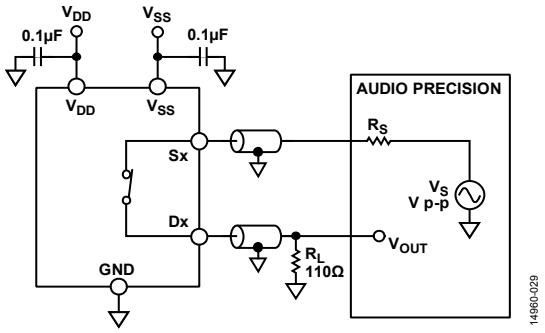

Figure 32. THD + Noise

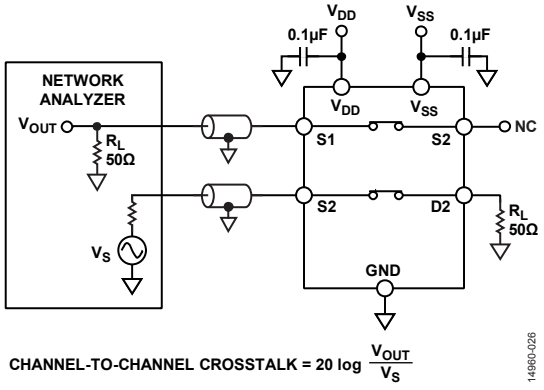

Figure 29. Channel to Channel Crosstalk

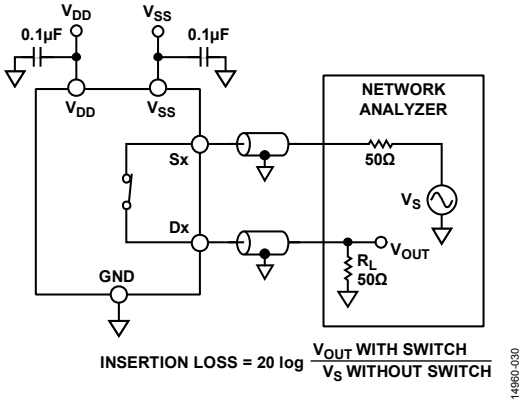

Figure 33. −3 dB Bandwidth

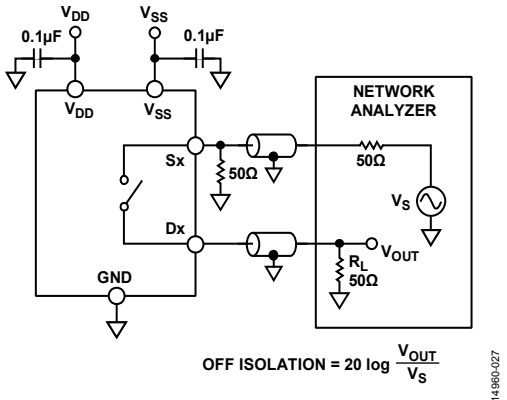

Figure 30. Off Isolation

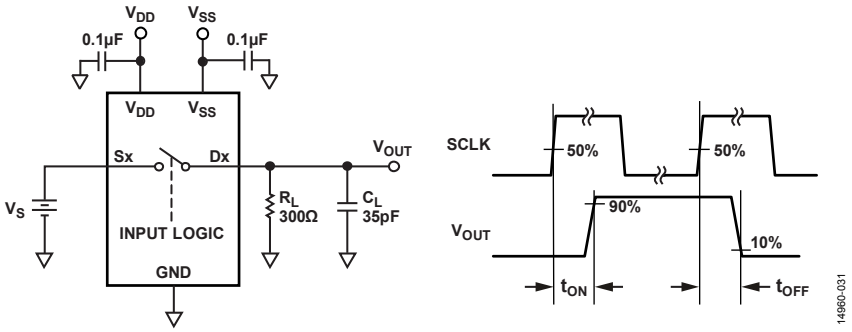

Figure 34. Switching Times, t_{ON} and t_{OFF}

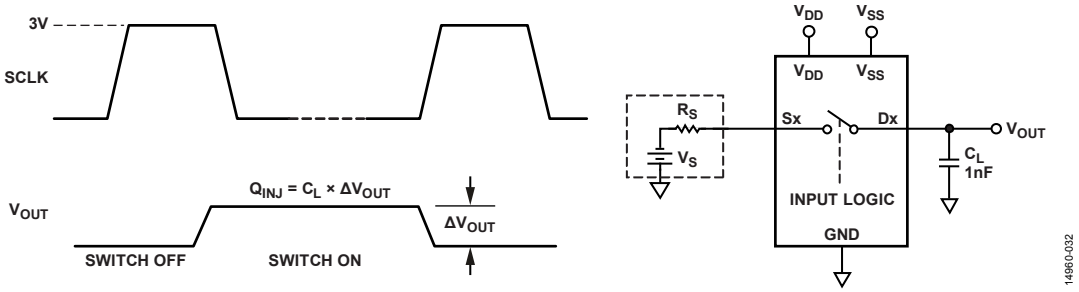

Figure 35. Charge Injection, Q_{INJ}

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal Dx and Terminal Sx, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between Terminal Dx and Terminal Sx.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} represents the delay between applying the digital control input and the output switching on.

t_{OFF}
t_{OFF} represents the delay between applying the digital control input and the output switching off.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

−3 dB Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. ACPSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATION

The ADGS1412 is a set of serially controlled, quad SPST switches with error detection features. SPI Mode 0 can be used with the device, and it operates with SCLK frequencies up to 50 MHz. The default mode for the ADGS1412 is address mode in which the registers of the device are accessed by a 16-bit SPI command that is bounded by $\overline{CS}$. The SPI command becomes 24 bit if the user enables CRC error detection. Other error detection features include SCLK count error and invalid read/write error. If any of these SPI interface errors occur, they are detectable by reading the error flags register. The ADGS1412 can also operate in two other modes, namely burst mode and daisy-chain mode.

The interface pins of the ADGS1412 are $\overline{CS}$, SCLK, SDI, and SDO. Hold $\overline{CS}$ low when using the SPI interface. Data is captured on the SDI on the rising edge of SCLK, and data is propagated out on the SDO on the falling edge of SCLK. SDO has an open-drain output; thus, connect a pull-up to this output. When not pulled low by the ADGS1412, SDO is in a high impedance state.

ADDRESS MODE

Address mode is the default mode for the ADGS1412 upon power up. A single SPI frame in address mode is bounded by a $\overline{CS}$ falling edge and the succeeding $\overline{CS}$ rising edge. It is comprised of 16 SCLK cycles. The timing diagram for address mode is shown in Figure 36. The first SDI bit indicates if the SPI command is a read or write command. When the first bit is set to 0, a write command is issued, and if the first bit is set to 1, a read command is issued. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command, because during these clock cycles SDO propagates out the data contained in the addressed register.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the 9th to the 16th SCLK falling edge during SPI reads. A register write occurs on the 16th SCLK rising edge during SPI writes.

During any SPI command, SDO sends out eight alignment bits on the first eight SCLK falling edges. The alignment bits observed at SDO are 0x25.

ERROR DETECTION FEATURES

Protocol and communication errors on the SPI interface are detectable. There are three detectable errors, which are incorrect SCLK error detection, invalid read and write address error detection, and CRC error detection. Each of these errors has a corresponding enable bit in the error configuration register. In addition, there is an error flag bit for each of these errors in the error flags register.

Cyclic Redundancy Check (CRC) Error Detection

The CRC error detection feature extends a valid SPI frame by 8 SCLK cycles. These eight extra cycles are needed to send the CRC byte for that SPI frame. The CRC byte is calculated by the SPI block using the 16-bit payload: the R/$\overline{W}$ bit, Register Address Bits[6:0], and Register Data Bits[7:0]. The CRC polynomial used in the SPI block is $x^8 + x^2 + x^1 + 1$ with a seed value of 0. For a timing diagram with CRC enabled, see Figure 37. Register writes occur at the 24th SCLK rising edge with CRC Error Checking enabled.

During a SPI write, the microcontroller/CPU provides the CRC byte through SDI. The SPI block checks the CRC byte just before the 24th SCLK rising edge. On this same edge, the register write is prevented if an incorrect CRC byte is received by the SPI interface. The CRC error flag is asserted in the error flags register in the case of the incorrect CRC byte being detected.

During a SPI read, the CRC byte is provided to the microcontroller through SDO.

The CRC error detection feature is disabled by default and can be configured by the user through the error configuration register.

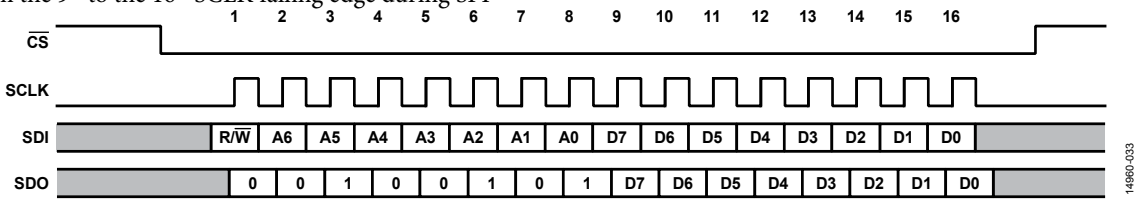

Figure 36. Address Mode Timing Diagram

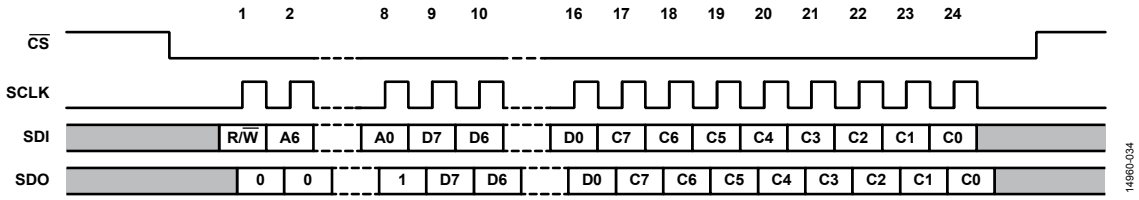

Figure 37. Timing Diagram with CRC Enabled

SCLK Count Error Detection

SCLK count error detection allows the user to detect if an incorrect number of SCLK cycles are sent by the microcontroller/CPU. When in address mode, with CRC disabled, 16 SCLK cycles are expected. If 16 SCLK cycles are not detected, the SCLK count error flag asserts in the error flags register. When less than 16 SCLK cycles are received by the device, a write to the register map never occurs. When the ADGS1412 receives more than 16 SCLK cycles, a write to the memory map still occurs at the 16th SCLK rising edge, and the flag asserts in the error flags register. With CRC enabled, the expected number of SCLK cycles becomes 24. SCLK count error detection is enabled by default and can be configured by the user through the error configuration register.

Invalid Read/Write Address Error

An invalid read/write address error detects when a nonexistent register address is a target for a read or write. In addition, this error asserts when a write to a read only register is attempted. The invalid read/write address error flag asserts in the error flags register when an invalid read/write address error happens. The invalid read/write address error is detected on the nineth SCLK rising edge, which means a write to the register never occurs when an invalid address is targeted. Invalid read/write address error detection is enabled by default and can be disabled by the user through the error configuration register.

CLEARING THE ERROR FLAGS REGISTER

To clear the error flags register, write the special 16-bit SPI frame, 0x6CA9, to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must also send the correct CRC byte for a successful error clear command. At the 16th or 24th SCLK rising edge, the error flags register resets to zero.

BURST MODE

The SPI interface can accept consecutive SPI commands without the need to de-assert the $\overline{CS}$ line, which is called burst mode. Burst mode is enabled through the burst enable register. This mode uses the same 16-bit command to communicate with the device. In addition, the response of the device at SDO is still aligned with the corresponding SPI command. Figure 38 shows an example of SDI and SDO during burst mode.

The invalid read/write address and CRC error checking functions operate similarly during burst mode as they do during address mode. However, SCLK count error detection operates in a slightly different manner. The total number of SCLK cycles within a given $\overline{CS}$ frame are counted, and if the total is not a multiple of 16, or a multiple of 24 when CRC is enabled, the SCLK count error flag asserts.

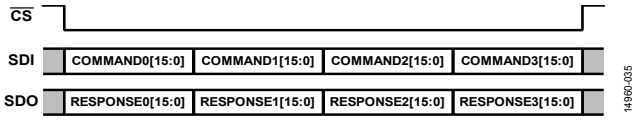

Figure 38. Burst Mode Frame

SOFTWARE RESET

When in address mode, the user can initiate a software reset. To do so, write two consecutive SPI commands, namely 0xA3 followed by 0x05, targeting Register 0x0B. After a software reset, all register values are set to default.

DAISY-CHAIN MODE

The connection of several ADGS1412 devices in a daisy-chain configuration is possible, and Figure 39 illustrates this setup. All devices share the same $\overline{CS}$ and SCLK line, whereas the SDO of a device forms a connection to the SDI of the next device, creating a shift register. In daisy-chain mode, SDO is an eight-cycle delayed version of SDI. When in daisy-chain mode, all commands target the switch data register. Therefore, it is not possible to make configuration changes while in daisy-chain mode.

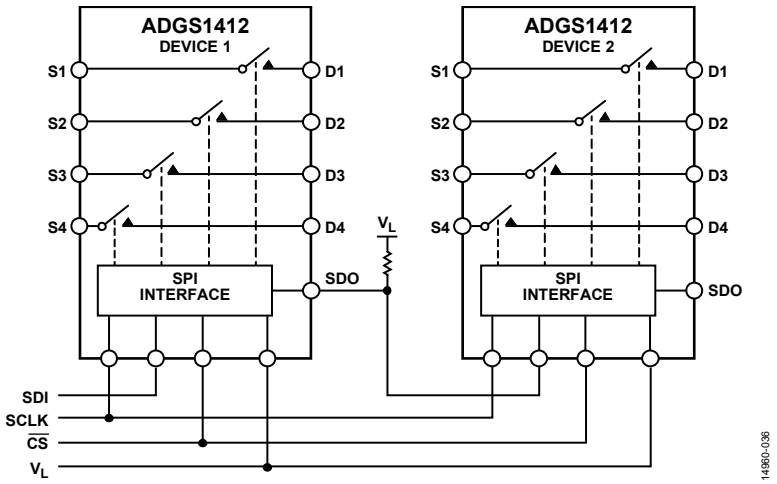

Figure 39. Two ADGS1412 Devices Connected in a Daisy-Chain Configuration

The ADGS1412 can only enter daisy-chain mode when in address mode by sending the 16-bit SPI command, 0x2500 (see Figure 40). When the ADGS1412 receives this command, the SDO of the device sends out the same command because the alignment bits at SDO are 0x25, which allows multiple daisy-connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 41. When $\overline{CS}$ goes high, Device 1 writes Command 0, Bits[7:0] to its switch data register of, Device 2 writes Command 1, Bits[7:0] to its switches, and so on. The SPI block uses the last eight bits it received through SDI to update the switches. After entering daisy-chain mode, the first eight bits sent out by SDO on each device in the chain are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset back to zero.

An SCLK rising edge reads in data on SDI while data is propagated out SDO on an SCLK falling edge. The expected number of SCLK cycles must be a multiple of eight before $\overline{CS}$ goes high. When this is not the case, the SPI interface sends the last eight bits received to the switch data register.

POWER-ON RESET

The digital section of the ADGS1412 goes through an initialization phase during V_L power up. This initialization also occurs after a hardware or software reset. After V_L power-up or a reset, ensure that a minimum of 120 µs from the time of power-up or reset before any SPI command is issued. Ensure that V_L does not drop out during the 120 µs initialization phase because it may result in incorrect operation of the ADGS1412.

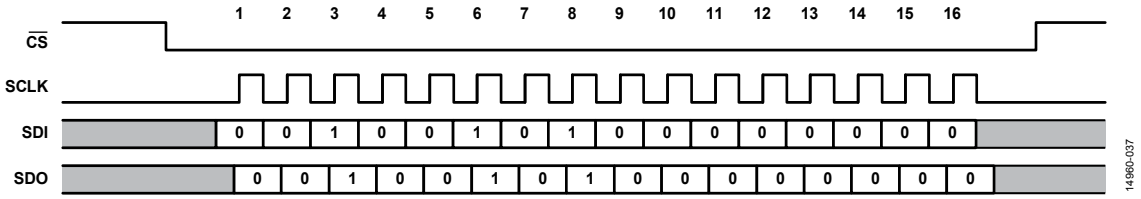

Figure 40. SPI Command to Enter Daisy-Chain Mode

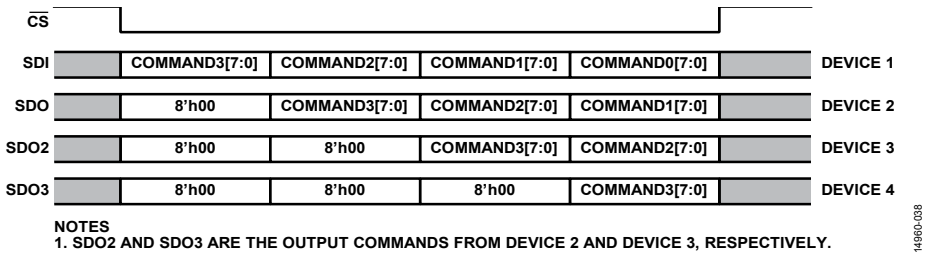

Figure 41. Example of a SPI Frame Where Four ADGS1412 Devices Connect in Daisy-Chain Mode

APPLICATIONS INFORMATION

POWER SUPPLY RAILS

To guarantee correct operation of the ADGS1412, 0.1 µF decoupling capacitors are required.

The ADGS1412 can operate with bipolar supplies between ±4.5 V and ±16.5 V. The supplies on V_{DD} and V_{SS} do not have to be symmetrical; however, the V_{DD} to V_{SS} range must not exceed 33 V. The ADGS1412 can also operate with single supplies between 5 V and 20 V with V_{SS} connected to GND.

The voltage range that can be supplied to V_L is from 2.7 V to 5.5 V.

The device is fully specified at ±15 V, +5 V, and +12 V analogue supply voltage ranges.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 42. The ADP5070 (dual switching regulator) generates a positive and negative supply rail for the ADGS1412, amplifier, and/or a precision converter in a typical signal chain. Also shown in Figure 42 are two optional LDOs, ADP7118 and ADP7182 positive and negative LDOs respectively, that can be used to reduce the output ripple of the ADP5070 in ultralow noise sensitive applications.

The ADM7160 can be used to generate V_L voltage that is required to power digital circuitry within the ADGS1412.

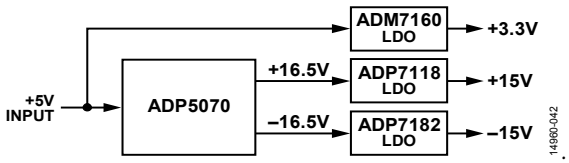

Figure 42. Bipolar Power Solution

Table 10. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADM7160	5.5 V, 200 mA, ultralow noise, linear regulator
ADP7118	20 V, 200 mA, low noise, CMOS LDO linear regulator
ADP7182	−28 V, −200 mA, low noise, LDO linear regulator

REGISTER SUMMARY

Table 11. Register Summary

Register (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
0x01	SW_DATA	Reserved				SW4_EN	SW3_EN	SW2_EN	SW1_EN	0x00	R/W
0x02	ERR_CONFIG	Reserved					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/W
0x03	ERR_FLAGS	Reserved					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	Reserved							BURST_MODE_EN	0x00	R/W
0x0B	SOFT_RESETB	SOFT_RESETB								0x00	R/W

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x01, Reset: 0x00, Name: SW_DATA

The switch data register controls the status of the four switches of the ADGS1412.

Table 12. Bit Descriptions for SW_DATA

Bits	Bit Name	Settings	Description	Default	Access
[7:4]	Reserved		These bits are reserved; set these bits to 0.	0x0	R
3	SW4_EN		Enable bit for SW4.	0x0	R/W
		0	SW4 open.		
		1	SW4 closed.		
2	SW3_EN		Enable bit for SW3.	0x0	R/W
		0	SW3 open.		
		1	SW3 closed.		
1	SW2_EN		Enable bit for SW2.	0x0	R/W
		0	SW2 open.		
		1	SW2 closed.		
0	SW1_EN		Enable bit for SW1.	0x0	R/W
		0	SW1 open.		
		1	SW1 closed.		

ERROR CONFIGURATION REGISTER

Address: 0x02, Reset: 0x06, Name: ERR_CONFIG

The error configuration register allows the user to enable and disable the relevant error features as required.

Table 13. Bit Descriptions for ERR_CONFIG

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	Reserved		These bits are reserved; set these bits to 0.	0x0	R
2	RW_ERR_EN		Enable bit for detecting invalid read/write address.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
1	SCLK_ERR_EN		Enable bit for detecting the correct number of SCLK cycles in a SPI frame. 16 SCLK cycles are expected when CRC is disabled and burst mode is disabled. 24 SCLK cycles are expected when CRC is enabled and burst mode is disabled. A multiple of 16 SCLK cycles are expected when CRC is disabled and burst mode is enabled. A multiple of 24 SCLK cycles are expected when CRC is enabled and burst mode is enabled.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
0	CRC_ERR_EN		Enable bit for CRC error detection. SPI frames are 24 bits wide when enabled.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

ERROR FLAGS REGISTER

Address: 0x03, Reset: 0x00, Name: ERR_FLAGS

The error flags register allows the user to determine if an error has occurred. To clear the error flags register, write the special 16-bit SPI command 0x6CA9 to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must include the correct CRC byte during the SPI write for the clear error flags register command to succeed.

Table 14. Bit Descriptions for ERR_FLAGS

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	Reserved		These bits are reserved and are set to 0.	0x0	R
2	RW_ERR_FLAG		Error flag for invalid read/write address. The error flag asserts during a SPI read if the target address does not exist. The error flag also asserts when the target address of a SPI write is does not exist or is read only.	0x0	R
		0	No error.		
		1	Error.		
1	SCLK_ERR_FLAG		Error flag for the detection of the correct number of SCLK cycles in a SPI frame.	0x0	R
		0	No error.		
		1	Error.		
0	CRC_ERR_FLAG		Error flag that determines if a CRC error has occurred during a register write.	0x0	R
		0	No error.		
		1	Error.		

BURST ENABLE REGISTER

Address: 0x05, Reset: 0x00, Name: BURST_EN

The burst enable register allows the user to enable or disable burst mode. When enabled, the user can send multiple consecutive SPI commands without deasserting $\overline{CS}$.

Table 15. Bit Descriptions for BURST_EN

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	Reserved		These bits are reserved; set these bits to 0.	0x0	R
0	BURST_MODE_EN		Burst mode enable bit.	0x0	R/W
		0	Disabled.		
		1	Enabled.		

SOFTWARE RESET REGISTER

Address: 0x0B, Reset: 0x00, Name: SOFT_RESETB

Use the software reset register to perform a software reset. Consecutively, write 0xA3 followed by 0x05 to this register, and the registers of the device reset to their default state.

Table 16. Bit Descriptions for SOFT_RESETB

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	SOFT_RESETB		To perform a software reset, consecutively write 0xA3 followed by 0x05 to this register.	0x0	R

OUTLINE DIMENSIONS

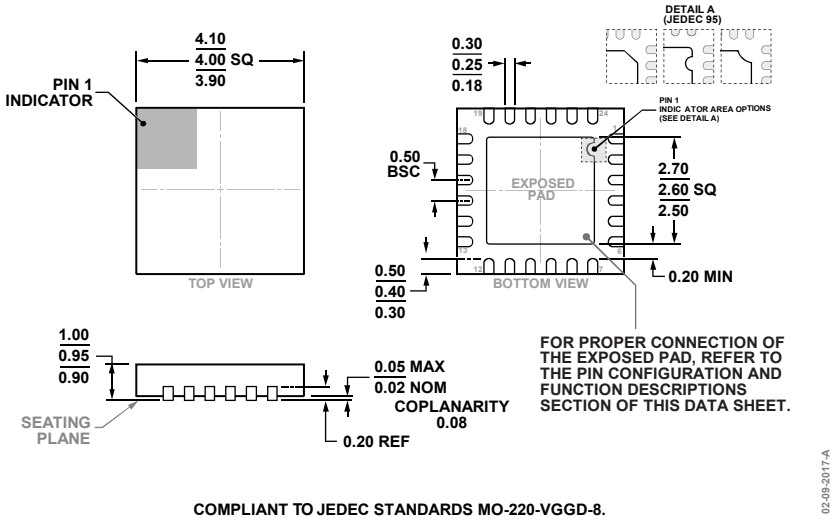

Figure 43. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.95 mm Package Height
(CP-24-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADGS1412BCPZ	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-17
ADGS1412BCPZ-RL7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-17

[1] Z = RoHS Compliant Part.