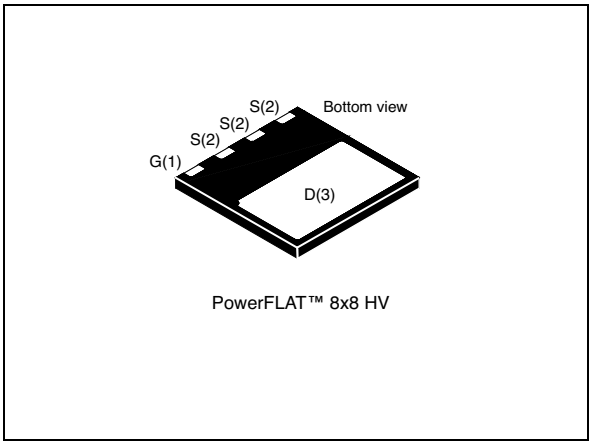
# STL17N65M5

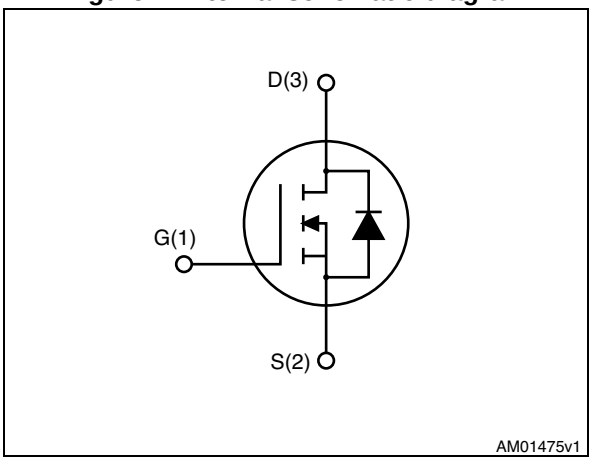
# N-channel 650 V, 0.338 Ω typ., 10 A MDmesh™ V Power MOSFET in a PowerFLAT™ 8x8 HV package

**Datasheet - preliminary data**




PowerFLAT™ 8x8 HV

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DS}$ @ $T_{Jmax}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STL17N65M5 | 710 V | 0.374 Ω | 10 A(1) |

1. The value is rated according to $R_{thj\text{-}case}$ and limited by package

- Worldwide best $R_{DS(on)}$ * area
- Higher $V_{DSS}$ rating and high dv/dt capability
- Excellent switching performance

## Applications

- Switching applications

## Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL17N65M5 | 17N65M5 | PowerFLAT™ 8x8 HV | Tape and reel |

# contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 650 | V |
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | 10 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 100 °C | 5.8 | A |
| $I_{DM}$ (1),(2) | Drain current (pulsed) | 40 | A |
| $I_D$ (3) | Drain current (continuous) at $T_{amb}$ = 25 °C | 1.8 | A |
| $I_D$ (3) | Drain current (continuous) at $T_{amb}$ = 100 °C | 1.2 | A |
| $P_{TOT}$ (3) | Total dissipation at $T_{amb}$ = 25 °C | 2.8 | W |
| $P_{TOT}$ (1) | Total dissipation at $T_C$ = 25 °C | 70 | W |
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max) | 2.5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 160 | mJ |
| dv/dt (4) | Peak diode recovery voltage slope | 15 | V/ns |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | 150 | °C |

1. The value is rated according to $R_{thj\text{-}case}$.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch², 2oz Cu.
4. $I_{SD} \leq 10$ A, di/dt $\leq$ 400 A/$\mu$s, $V_{Peak} < V_{(BR)DSS}$, $V_{DD}$=400 V

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 1.79 | °C/W |
| $R_{thj\text{-}amb}$ (1) | Thermal resistance junction-ambient max | 45 | °C/W |

1. When mounted on FR-4 board of inch², 2oz Cu.

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{DS}$ = 650 V, $V_{GS}$ = 0<br>$V_{DS}$ = 650 V, $V_{GS}$ = 0, $T_C$=125 °C | | | 1<br>100 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{GS}$ = ± 25 V, $V_{DS}$ = 0 | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 5.5 A | | 0.338 | 0.374 | Ω |

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 816 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 23 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.6 | - | pF |
| $C_{o(er)}$ (1) | Equivalent output capacitance energy related | $V_{GS}$ = 0, $V_{DS}$ = 0 to 520 V | - | 21 | - | pF |
| $C_{o(tr)}$ (2) | Equivalent output capacitance time related | | - | 70 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 5 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 5.5 A, $V_{GS}$ = 10 V (see *Figure 15*) | - | 22 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 5.5 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 11 | - | nC |

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$
2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(v)}$ | Voltage delay time | $V_{DD}$ = 400 V, $I_D$ = 6 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 16* and *19*) | - | 30 | - | ns |
| $t_{r(v)}$ | Voltage rise time | | - | 8 | - | ns |
| $t_{f(i)}$ | Current fall time | | - | 11 | - | ns |
| $t_{c(off)}$ | Crossing time | | - | 12.5 | - | ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 10 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 40 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 11 A, $V_{GS}$ = 0 | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 11 A, di/dt = 100 A/µs $V_{DD}$ = 100 V (see *Figure 16*) | - | 247 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 2.4 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 19.5 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 11 A, di/dt = 100 A/µs $V_{DD}$ = 100 V, $T_j$ = 150 °C (see *Figure 16*) | - | 312 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 3 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 19 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

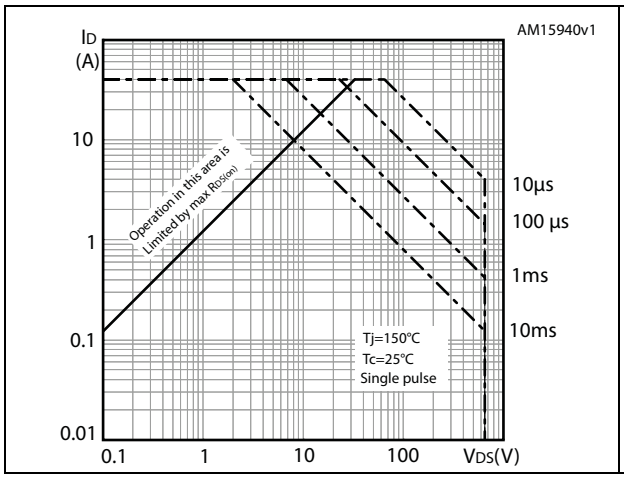



**Figure 3. Thermal impedance**

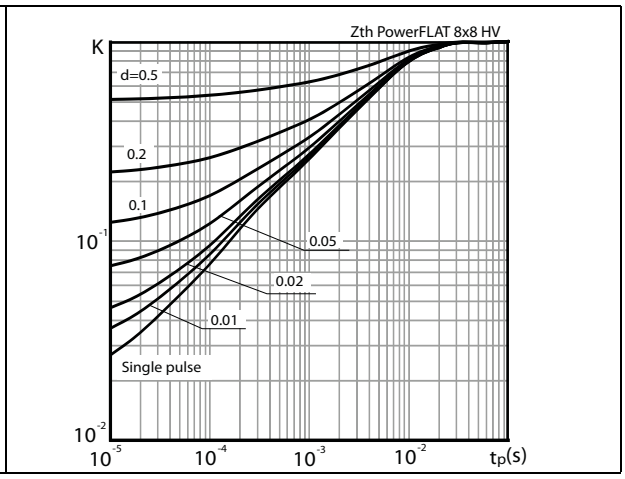



**Figure 4. Output characteristics**

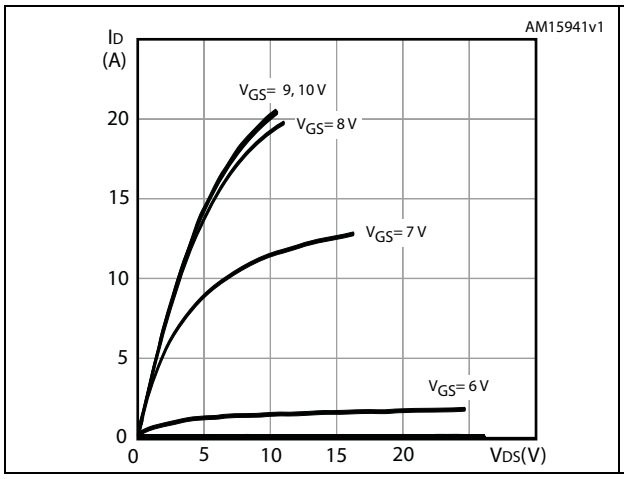



**Figure 5. Transfer characteristics**

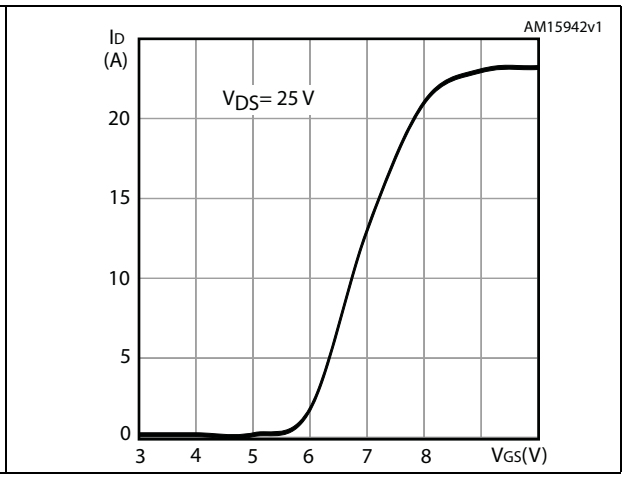



**Figure 6. Gate charge vs gate-source voltage**

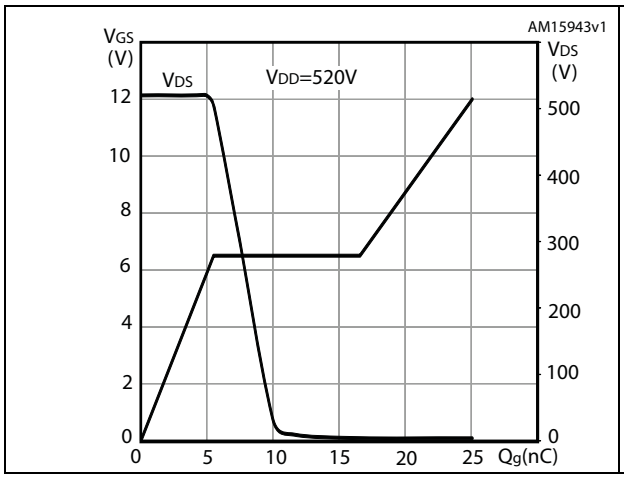



**Figure 7. Static drain-source on-resistance**

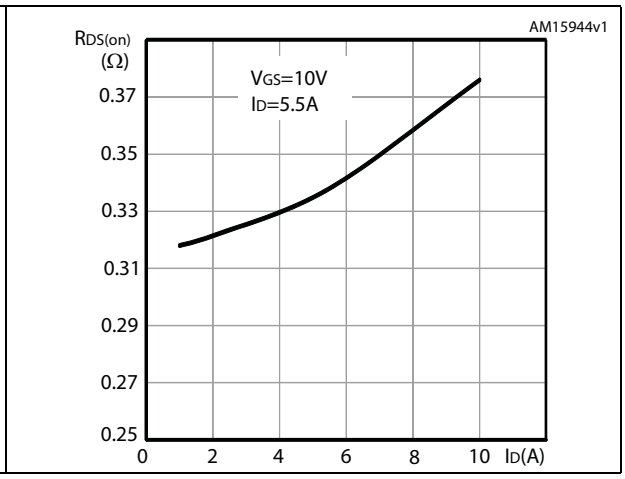


**Figure 8. Capacitance variations**

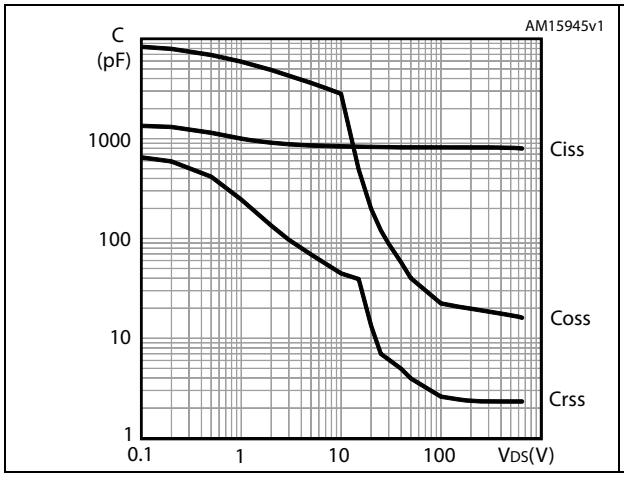



**Figure 9. Normalized $V_{DS}$ vs temperature**

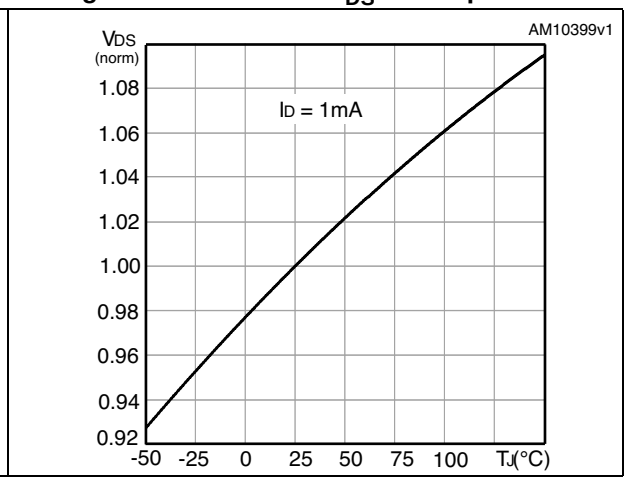



**Figure 10. Normalized gate threshold voltage vs temperature**

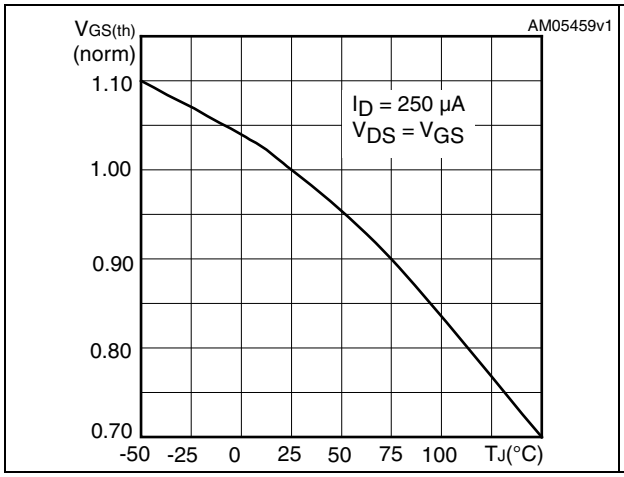



**Figure 11. Normalized on-resistance vs temperature**

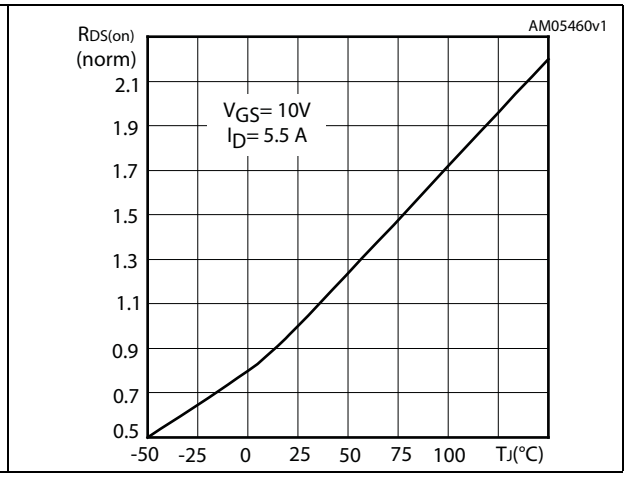



**Figure 12. Source-drain diode forward characteristics**

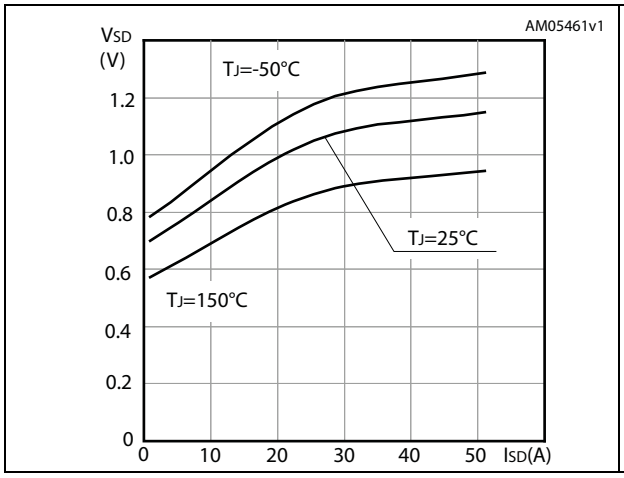
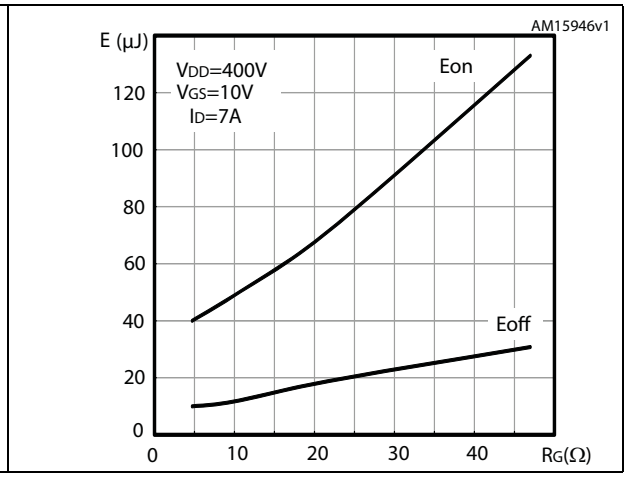



**Figure 13. Switching losses vs gate resistance(1)**




1. Eon including reverse recovery of a SiC diode

# 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**

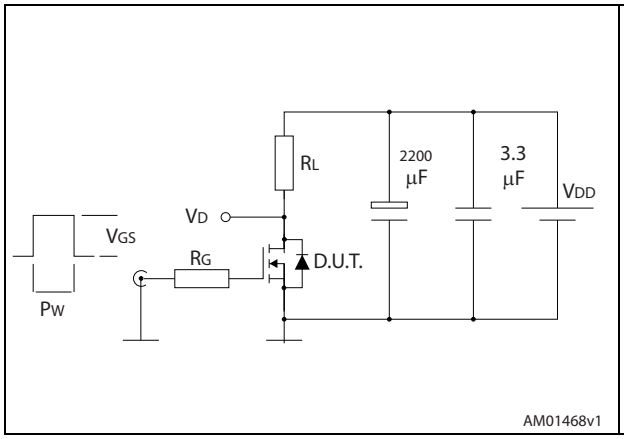



**Figure 15. Gate charge test circuit**

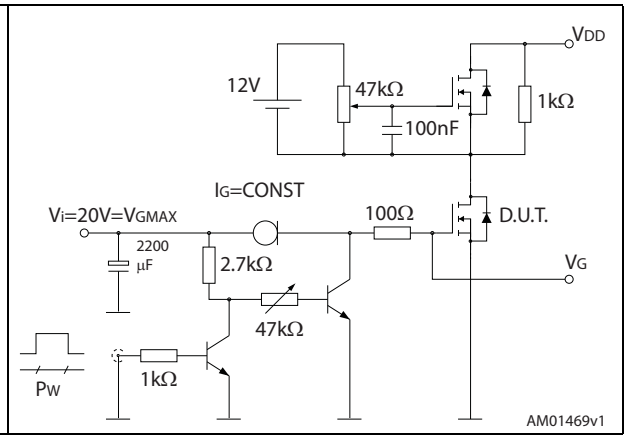



**Figure 16. Test circuit for inductive load switching and diode recovery times**

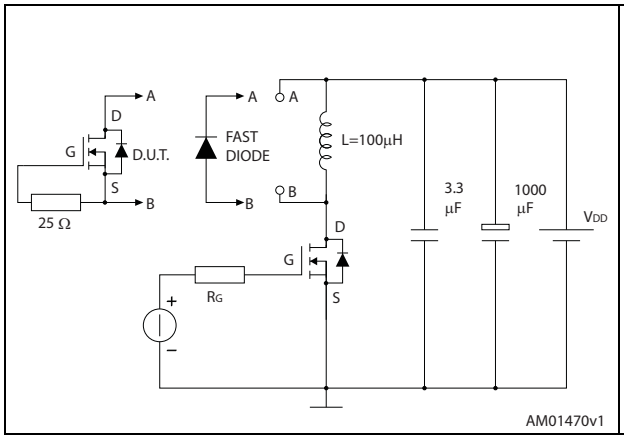



**Figure 17. Unclamped inductive load test circuit**

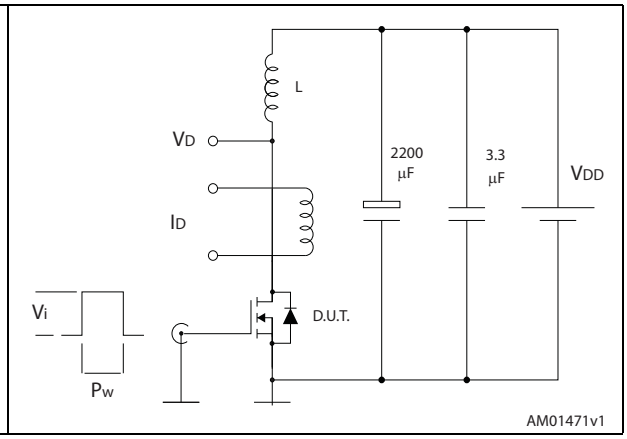



**Figure 18. Unclamped inductive waveform**

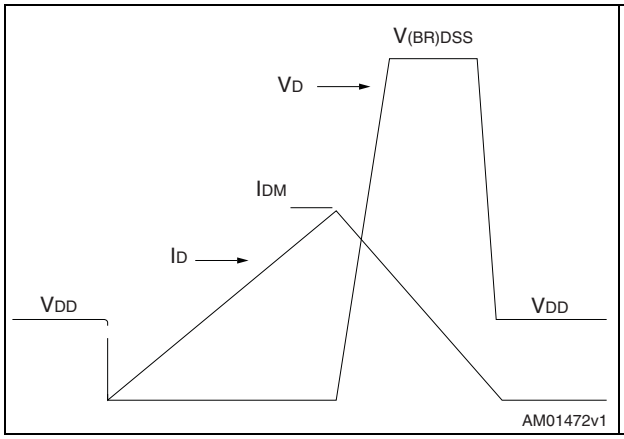
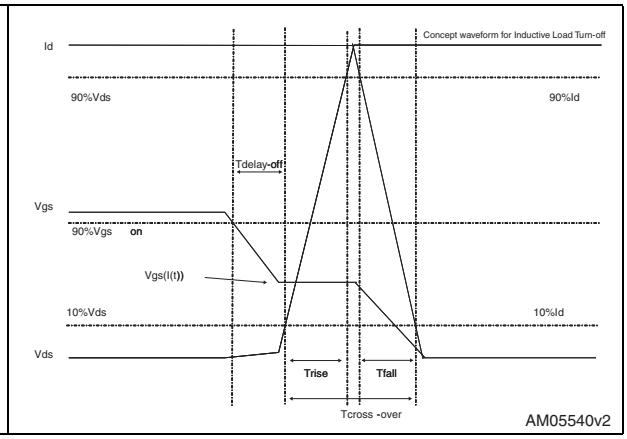



**Figure 19. Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.95 | 1.00 | 1.05 |
| D | | 8.00 | |
| E | | 8.00 | |
| D2 | 7.05 | 7.20 | 7.30 |
| E2 | 4.15 | 4.30 | 4.40 |
| e | | 2.00 | |
| L | 0.40 | 0.50 | 0.60 |

**Figure 20. PowerFLAT™ 8x8 HV drawing mechanical data**

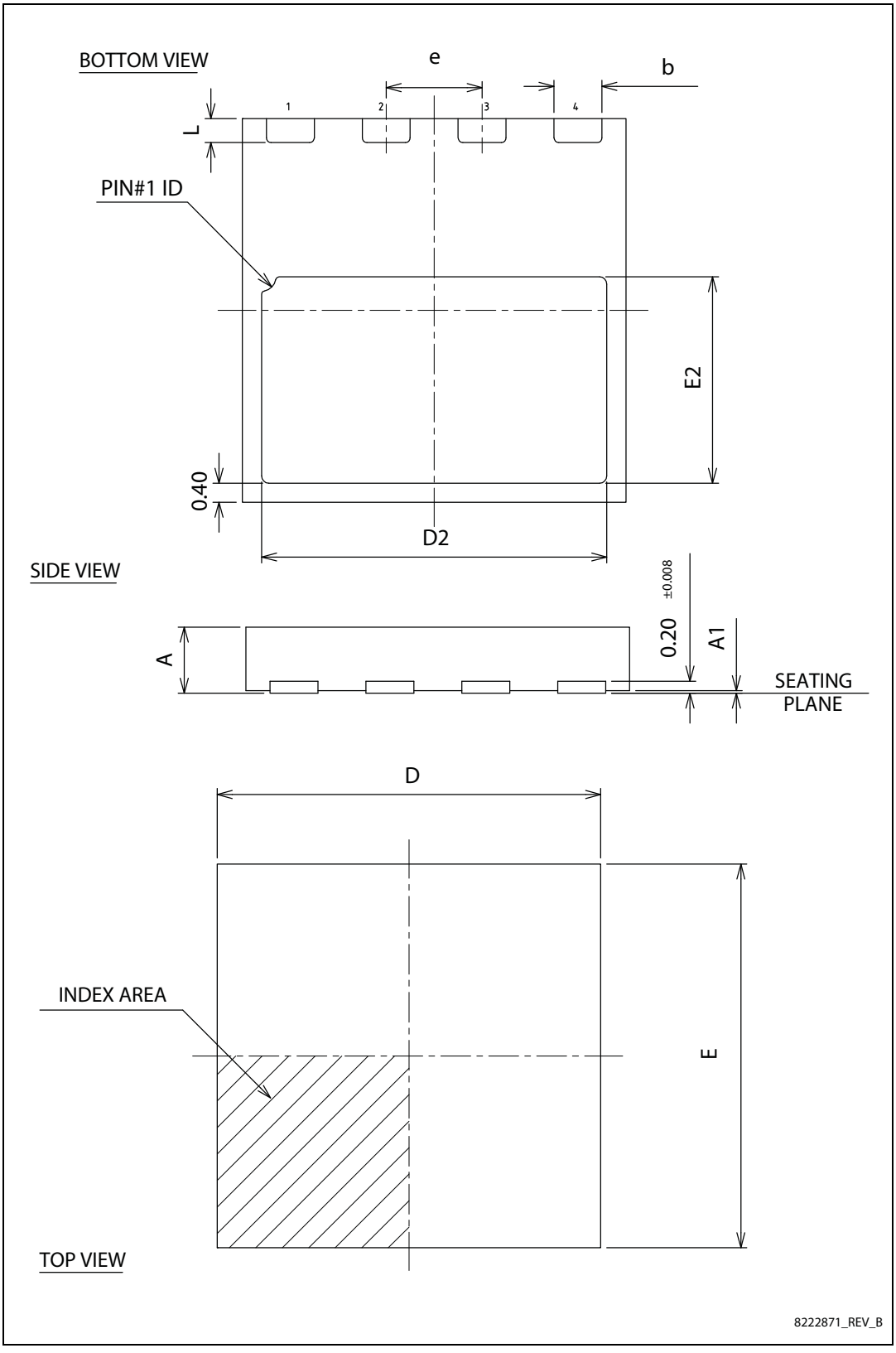
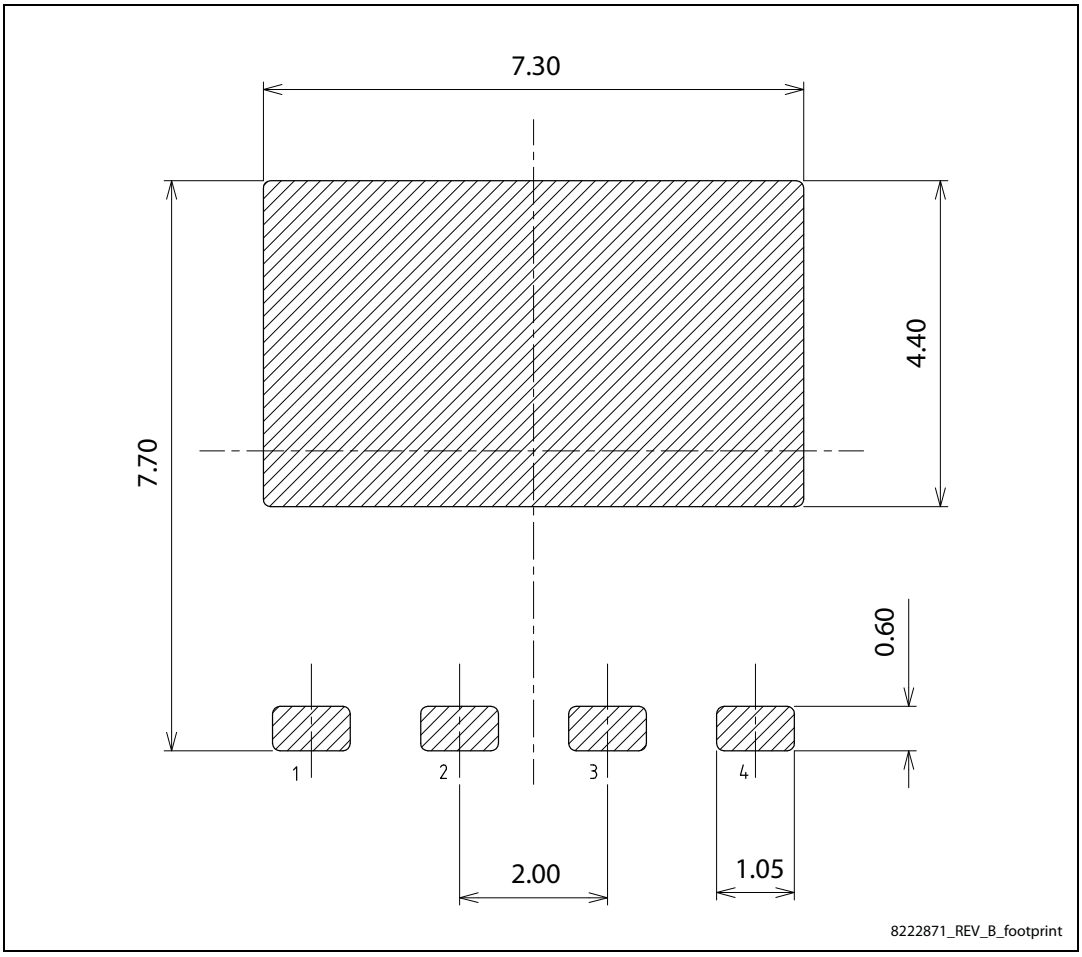


**Figure 21. PowerFLAT™ 8x8 HV recommended footprint (dimension in millimeters)**



# 5 Packaging mechanical data

**Figure 22. PowerFLAT™ 8x8 HV tape (dimension in millimeters)**

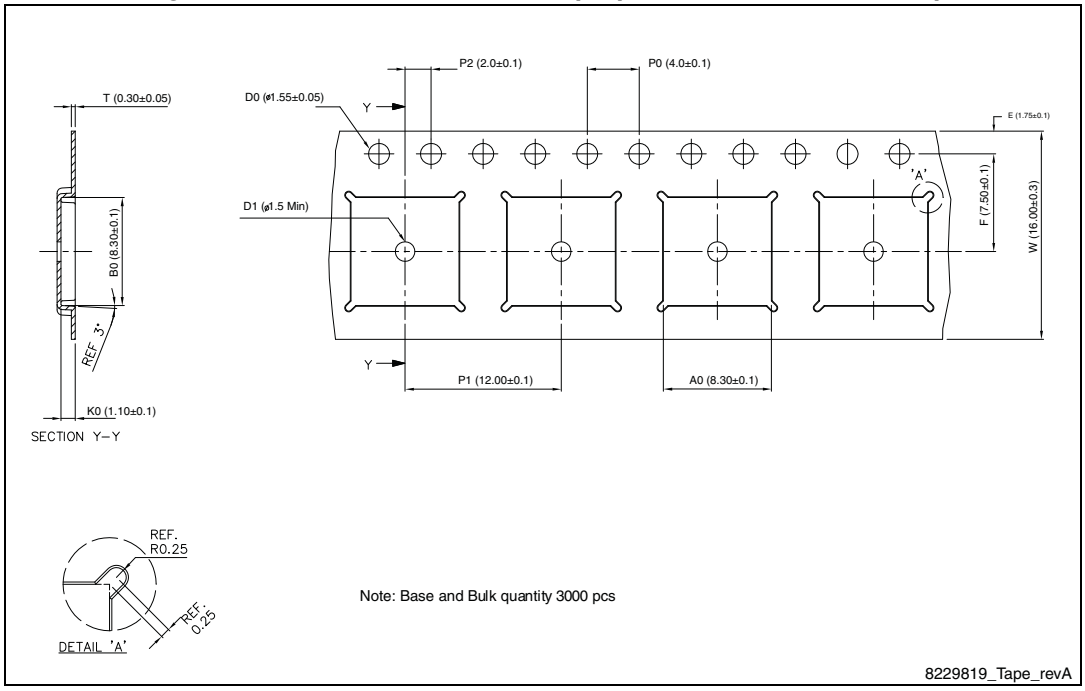



**Figure 23. PowerFLAT™ 8x8 HV package orientation in carrier tape**

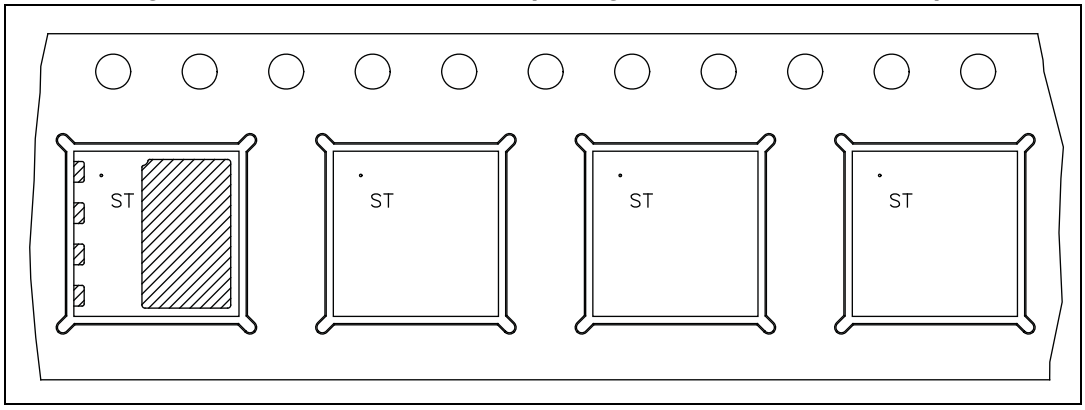
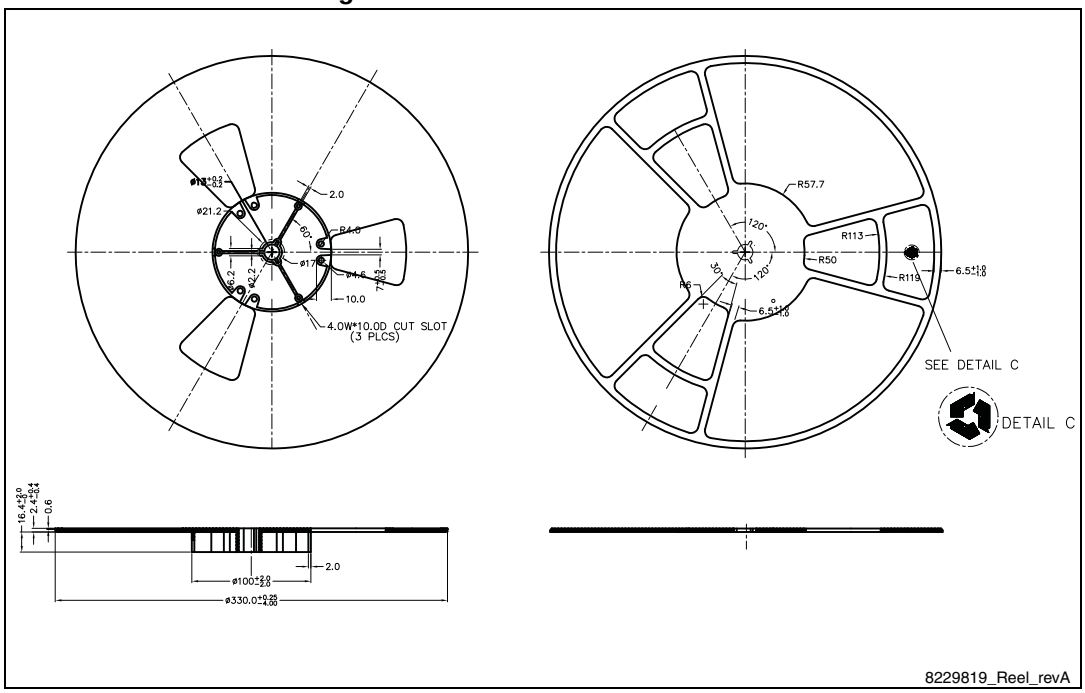


**Figure 24. PowerFLAT™ 8x8 HV reel**



# 6 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 05-Apr-2012 | 1 | First release. |
| 09-Jul-2013 | 2 | – Modified: note *1* and *Figure 1* in first page<br>– Modified: $I_D$ value at $T_C$=100 °C, $T_{amb}$=25 °C, $T_{amb}$=100 °C, $P_{TOT}$ and $E_{AS}$ values in *Table 2*<br>– Modified: $R_{thj\text{-}case}$ value in *Table 3*, the entire typical values in table *Table 5*, *6* and *7*<br>– Inserted: *Section 2.1: Electrical characteristics (curves)*<br>– Modified: *Figure 15*, *16* and *17*<br>– Minor text changes |
| 17-Jul-2013 | 3 | – Minor text changes<br>– Modified: *Table 6*<br>– Updated: *Section 4: Package mechanical data* |

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