LTM2895 100MHz Isolated DAC SPI Serial Interface and LTC2642-16

DESCRIPTION

Demonstration circuit DC2589A shows an LTM®2895 isolating and interfacing an LTC®2642-16. The LTM2895 is a high speed SPI isolator for interfacing DACs with a full complement of control signals. The LTC2642-16 is a bipolar 16-bit unbuffered voltage output DAC. Low noise isolated power is delivered to the isolated side with a LT®3999 push pull driver and isolation transformer.

The DC2589A demonstrates the DC and AC operation of the LTC2642-16 without performance degradation when isolated with the LTM2895. The serial peripheral interface (SPI) runs at a maximum 100MHz SCK frequency. The LTM2895 is configurable with many DACs with SPI clock frequencies up to 100MHz.

The DC2589A connects to either the DC590 or DC2026 for control with QuikEval™.

Design files for this circuit board are available at http://www.linear.com/demo/DC2589A

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Range	VCC-GND	4.75		5.25	V
	Analog Signal Output Range (AOUT)				±5	V
	Analog Output Frequency	Default sine wave, f_{CLK} = 100MHz, Sample Rate Divisor = 1		2.33		kHz
	User Waveform Buffer				4096	Samples
f_{CLK}	Clock Frequency (CLK IN)		50		100	MHz
	Internal Clock Frequency	No f_{CLK} input	50	80	100	MHz
V_{IORM}	Maximum Working Insulation Voltage	GND to GND2	500			V_{RMS}

DC2589A CONNECTION DIAGRAM

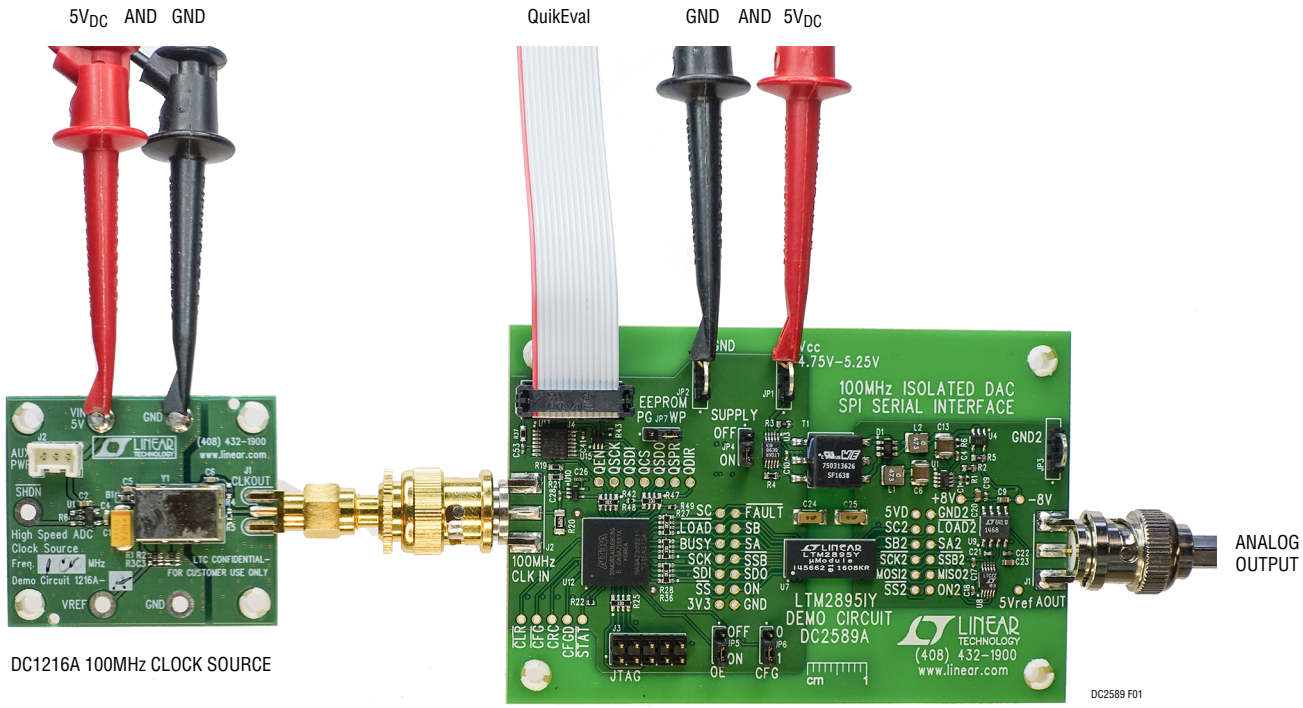

Figure 1. DC2589A Setup

DC2589A JUMPERS

JP1: VCC, 5V Power Supply input connection.

JP2: GND, Power Supply return connection.

JP3: GND2, Isolated Ground connection.

JP4: Supply Enable, enables or disables onboard DC/DC converter, default ON.

JP5: OE, Output Enable for U12. When OE is ON, U12 drives the signals to U7 for use with the DC590, or DC2026 or standalone operation. When OE is OFF, the signals to U7 are medium or high impedance from U12 and so the interface signals can be driven externally from the test points. Default is ON.

JP6: CFG, Default 1.

JP7: EEPROM is for factory use only, default is WP.

STANDALONE QUICK START PROCEDURE

1. To use the DC2589A, it is necessary to apply 5V and ground to the VCC and GND terminals of the DC2589A.
2. An external clock such as the DC1216 is suggested on 100MHz CLK IN/J2 to provide accurate waveform generation.
3. Make sure JP4 is in the ON position.
4. Make sure JP5 is in the ON position.
5. Measure the sine wave output at AOUT/J1.

DC590/DC2026 QUICK START PROCEDURE

1. To use the DC590/DC2026 with the DC2589A, it is necessary to apply 5V and ground to the VCC and GND terminals of the DC2589A.
2. Connect the DC590/DC2026 to a host PC with a standard USB A/B cable.
3. Connect the DC2589A's QuikEval connector J4 to a DC590/DC2026 USB serial controller using the supplied 14-conductor ribbon cable.
4. An external clock such as the DC1216 is suggested on J2 to provide accurate frequency generation.
5. Run the QuikEval software (quikeval.exe version K109 or later), which is available from www.linear.com/designtools/software. The correct control panel will be loaded automatically.
6. Make sure that the ON radio buttons for the LTM2895 and Output are selected.
   a. The *LTM2895* radio button controls the state of the LTM2895's ON pin which enables or disables the LTM2895.
   b. The *Output* radio button stops or starts the FPGA data writing to the DAC. When OFF is selected, the FPGA writes the mid-scale value to the DAC once and then stops writing further data.
7. Select the desired output waveform from the Output Selection.
   a. *Sine Wave* will generate the pre-programmed sine wave.
   b. *Square Wave* will generate a square wave with the high and low levels as indicated. The format for the values is selected by the radio buttons to the right.
   c. *DC Level* will generate a constant output as indicated. The format for the values is selected by the radio buttons to the right.
   d. *Load Waveform* will load a text file containing an arbitrary waveform pattern which will be generated in a looping manner. See the User Waveform Data File Format subsection for more details on the file format. Once a waveform is loaded, the User Waveform radio button will select the waveform.
8. The sample rate may be reduced by entering an integer number between 1 and 256. See the FPGA subsection for the sample rate calculation.

DC590/DC2026 QUICK START PROCEDURE

9. The status of the DC2589A is reported by the indicators in the lower right.

   a. *Isolator ON* indicates the status of the LTM2895 ON pin.

   b. *Isolator Fault* latches when the $\overline{\text{FAULT}}$ pin on the LTM2895 goes low. This is cleared with the button to the right.

   c. *FPGA Output Enable* reports the status of JP5. When the outputs are disabled, the FPGA connections to the LTM2895 are medium or high impedance, allowing the LTM2895 to be externally driven.

   d. *FPGA Image CFG* reports the status of JP6 which is for future use.

   e. *Loop Back Fault* latches if there is a mismatch between the MOSI data transmitted and the MISO data received across the LTM2895. This is cleared with the button to the right.

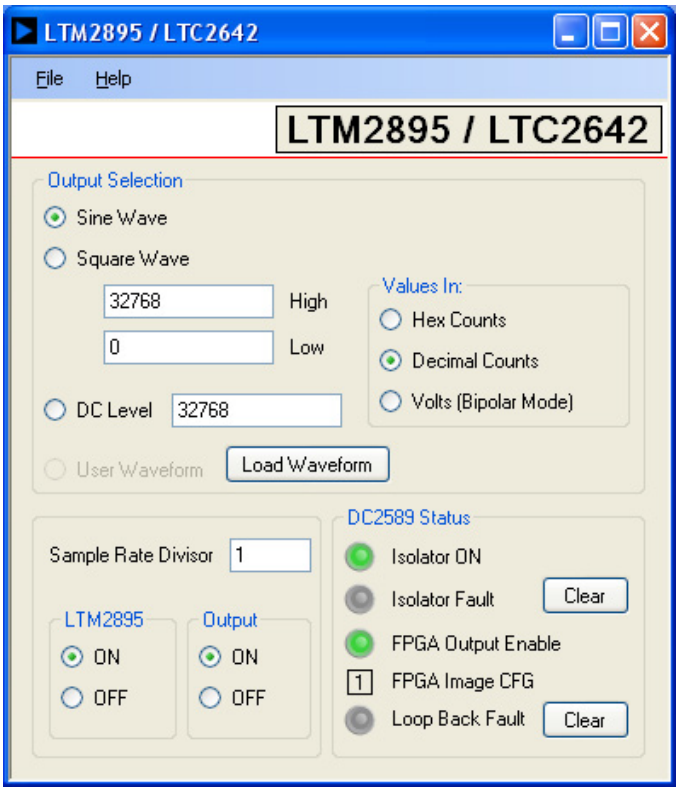

Figure 2. QuikEval Image

DC2589A FEATURES

DC Power

The DC2589A requires +5VDC and draws approximately 180mA. This current is split between the isolated side and the logic side. The isolated side load is powered through the DC/DC power converter and consists of the isolated side of the LTM2895, the LTC2642-16 DAC and the LT1468 output buffer. The logic side load is supplied by a LT1763 3.3V LDO and primarily consists of the FPGA, the clock input buffer and the LTM2895's logic side.

The isolated power supply may be disabled to allow the use of an external positive supply by moving jumper JP4 to the OFF position. An external supply may be connected between either the +8V or +5VD nodes and GND2. For the +8V node, use a 5.5V to 15V supply. For the +5VD node, use a 3V to 5V supply. Do not externally supply the –8V or 5VRef nodes.

Clock Source

You may provide a low jitter $2.5V_{P-P}$ 50MHz to 100MHz sine or square wave to the clock input J2. The clock input is AC coupled so the DC level of the clock signal is not important.

A generator such as the DC1216 High Speed ADC Clock Source is recommended.

If a clock signal is not present, the DC2589A's FPGA will internally generate a nominally 80MHz clock to produce an output waveform; however, the timing of the internally generated clock may vary between 50MHz and 100MHz.

When using the internal FPGA clock and observing the output spectrum, side-lobes will be present at about –60dB below the fundamental due to the FPGA clock's frequency drift. Using a lower jitter clock will significantly reduce the side-lobes.

Analog Output

The DC2589A's analog output, J1, is connected to the output of the LT1468 which buffers the DAC output with a full-scale range of ±5V. This output is suitable for driving a low capacitance, high impedance load. An external amplifier will be required if driving a 50Ω load.

FPGA

Upon power up, the DC2589A's FPGA configures the LTM2895 for operation with the LTC2642-16 with a 50MHz SPI clock with a 16-bit word length.

The FPGA automatically selects between the external clock and the internally generated clock as described in Clock Source.

The DC2589A's FPGA contains two waveform buffers in addition to a constant register which holds the data that is sent via SPI through the LTM2895 to the LTC2642-16 DAC.

When the output is enabled, the waveform buffers continuously are written out in a looping manner. The constant register is only written when it changes. When the output is disabled, the FPGA writes a single value to set the output to 0V.

The waveform buffers are written out with the sample rate which is a function of the clock frequency and a sample rate divisor:

$$f_{SAMPLE} = \frac{f_{CLK}}{42 \bullet \text{Sample Rate Divisor}}$$

The sample rate divisor is 1 by default, but may be changed by the QuikEval interface to any value between 1 and 256.

The serial data sent across the LTM2895 is looped back from the isolated side, read by the FPGA and compared against what was previously sent. If a mismatch occurs, the FPGA sets a loopback data mismatch error flag. This flag may be read and/or cleared via the QuikEval interface.

DC2589A FEATURES

The FPGA will latch any LTM2895 $\overline{\text{FAULT}}$ outputs with the Isolator Fault flag which may be read and/or cleared via the QuikEval interface.

The first waveform buffer contains a pre-programmed sine wave consisting of 1020 x 16-bit samples. The second buffer is for user downloaded waveforms and consists of 4096 x 16-bit samples. The constant register holds a single 16-bit word.

By default, the FPGA endlessly loops through the data contained within the sine-wave waveform buffer at the maximum sample rate. Using the QuikEval interface, the sample rate and the output source can be changed, started and/or stopped as desired.

User Waveform Data File Format

The user waveform data which is downloaded using the QuikEval interface consists of a text file with numeric strings containing the decimal sample values (0 to 65535), one value per line. An optional blank line will indicate the end of data. Any values following the 1st blank line will be ignored. The file must contain at least 1 sample and no more than 4096 samples. If there are fewer than 4096 samples, the DC2589A will automatically loop back at the end of the data.

An example data file consisting of 10 sample points forming a ramp from negative to positive full scale would be

0
7282
14563
21845
29127
36408
43690
50972
58253
65535

LTM2895 Digital Interface

The demo board has unpopulated header placeholders with 0.100 inch centers on either side of the LTM2895. The headers provide access to all signals and power supplies of the LTM2895.

All interface signals between the FPGA (U12) and the logic interface of the LTM2895 (U7) are exposed. An external interface may control the LTM2895 by setting the OE jumper JP5 OFF. When JP5 is OFF, all signals from the FPGA to the LTM2895 will be medium or high impedance as follows:

FPGA Pin	STATE	FPGA Pin	STATE
SA	High-Z	ON	Pull-Up
SB	High-Z	SCK	Pull-Up
SC	High-Z	SDI	Pull-Up
$\overline{\text{SSB}}$	Pull-Up	$\overline{\text{LOAD}}$	Pull-Up
$\overline{\text{SS}}$	Pull-Up		

Change the position of JP5 when the DC2589A is off.

The isolated side MISO/MOSI signals are connected in a loop-back configuration by R50.

DC2589A FEATURES

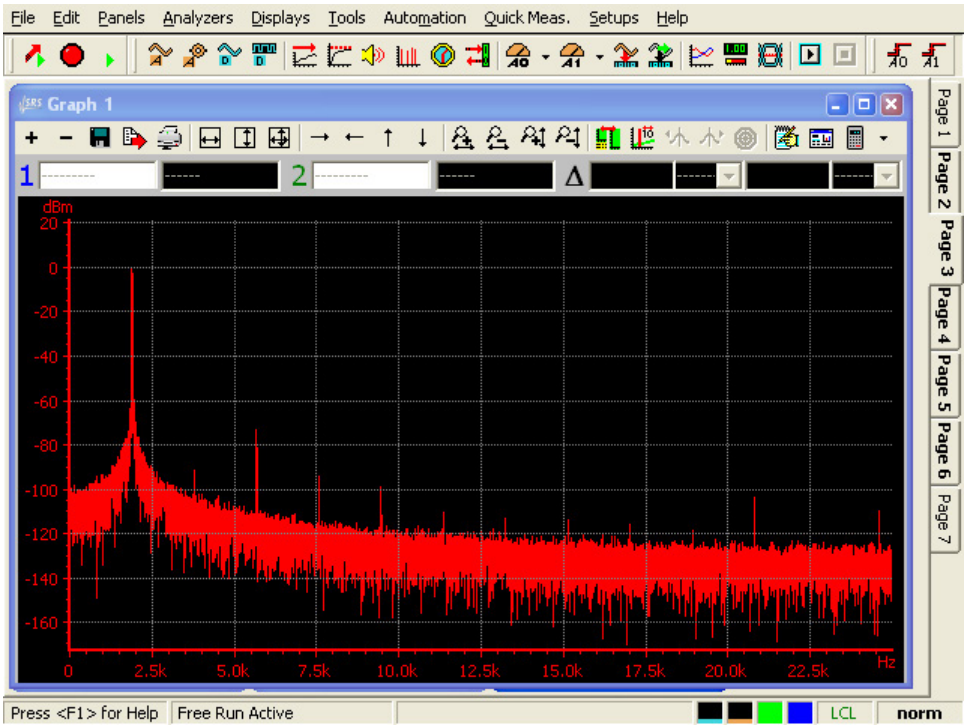

Figure 3. SR1 Audio Analyzer Display Showing Sine Wave Output Spectrum with FPGA Clock Source

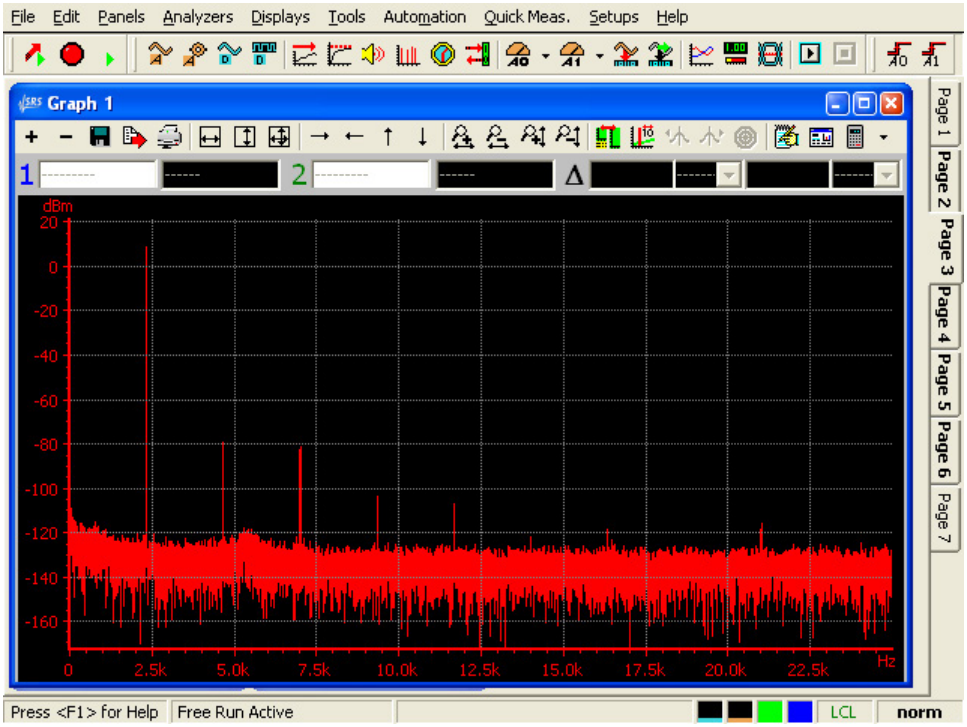

Figure 4. SR1 Audio Analyzer Display Showing Sine Wave Output Spectrum with DC1216A Clock Source

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Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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