AT91EB42 Evaluation Board

User Guide

Table of Contents

Section 1

Overview

1.1 Scope

The AT91EB42 Evaluation Board enables real-time code development and evaluation. It supports the AT91M42800A.

This user guide focuses on the AT91EB42 Evaluation Board as an evaluation and demonstration platform.

- Section 1 provides an overview.
- Section 2 describes how to set up the evaluation board.
- Section 3 details the on-board software.
- Section 4 contains a description of the circuit board.
- Section 5 and Section 6 are two appendixes covering configuration straps and schematics, including pin connectors.

1.2 Deliverables

The evaluation board is delivered with a DB9 plug-to-DB9 socket straight-through serial cable to connect the target evaluation board to a PC. A bare power lead with a 2.1 mm jack on one end for connection to a bench power supply is also delivered.

The evaluation board is also delivered with a CD-ROM that contains an evaluation version of the software development toolkit, the documentation that outlines the AT91 microcontroller family and the AT91 C Library.

The evaluation board is capable of supporting different kinds of debugging systems, using an ICE interface or the on-board Angel™ Debug Monitor.

1.3 The AT91EB42 Evaluation Board

The board consists of an AT91M42800A together with several peripherals:

- Two serial ports
- Reset push-button
- An indicator that memorizes a reset event
- Four user-defined push-buttons
- Eight LEDs
- A 256K bytes 16-bit SRAM (upgradeable to 1M byte)

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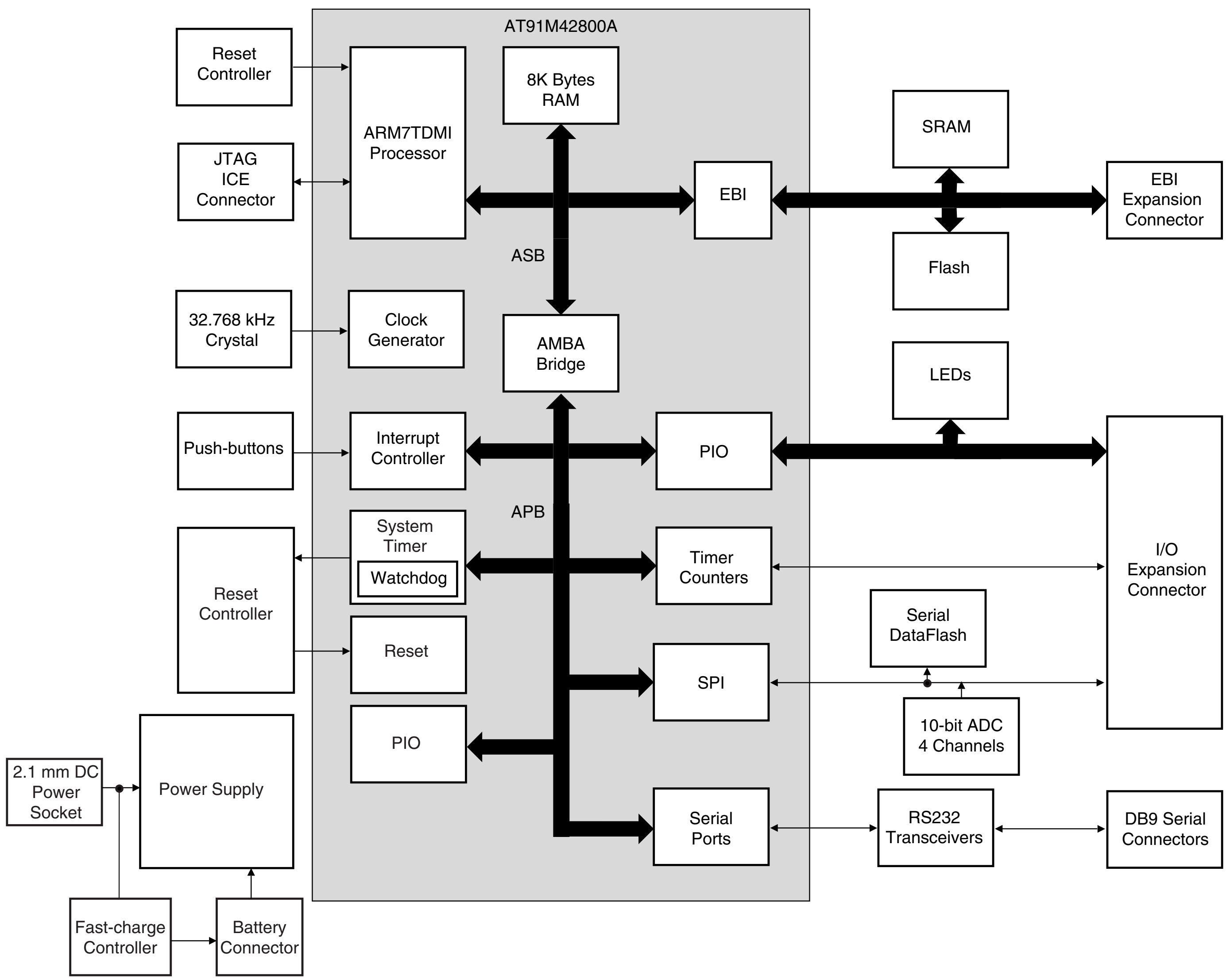
- A 2M bytes 16-bit Flash (of which 1M byte is available for user software)
- A 4M bytes Serial DataFlash
- An analog-to-digital converter with SPI access
- 2 x 32-pin EBI expansion connectors
- 2 x 32-pin I/O expansion connectors
- 20-pin JTAG interface connector

If required, user-defined peripherals can also be added to the board. See Section 5 for details.

Figure 1-1. AT91EB42 Evaluation Board Block Diagram



Section 2

Setting Up the AT91EB42 Evaluation Board

2.1 Electrostatic Warning

The AT91EB42 Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

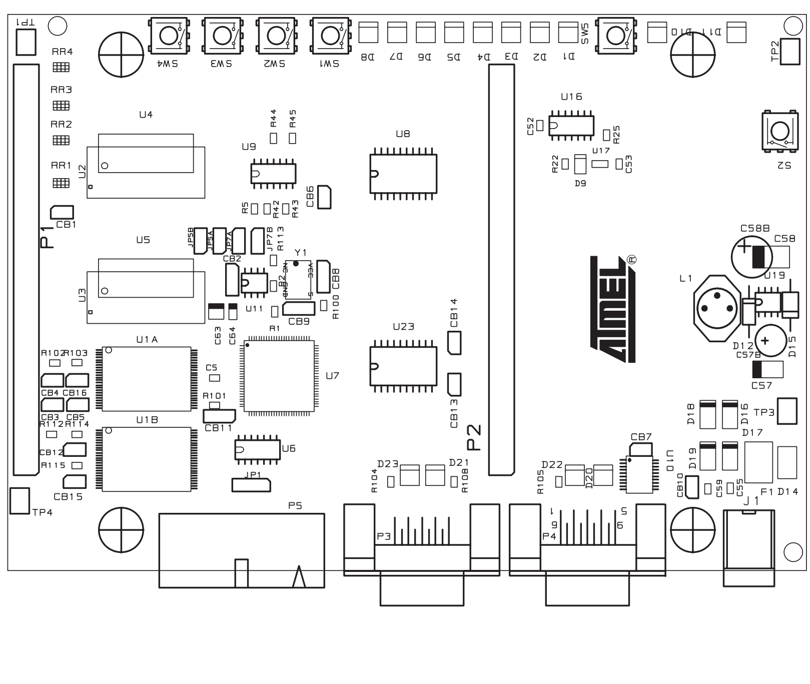
In order to set up the AT91EB42 Evaluation Board, the following requirements are needed:

- The AT91EB42 Evaluation Board itself
- The DC power supply capable of supplying 7V to 12V at 1A (not supplied)

2.3 Layout

Figure 2-1 shows the layout of the AT91EB42 Evaluation Board.

Figure 2-1. Layout of the AT91EB42 Evaluation Board



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2.4 Jumper Settings

JP1 is used to boot standard or user programs. For standard operations, set it in the STD position.

JP8 is used to select the core power supply of the AT91M42800A. Operations at 2V are not supported on the current silicon.

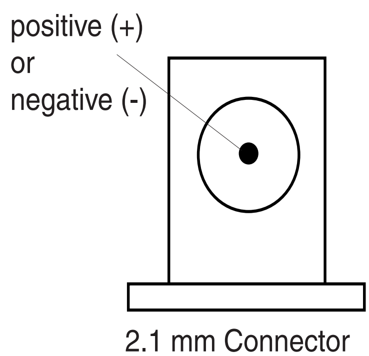
For more information about jumpers and other straps, see Section 5.

2.5 Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (J1) shown in Figure 2-2. The polarity of the power supply is not critical. The minimum voltage required is 7V.

A battery is supplied on the AT91EB42. It supplies all on-board devices in the same way that the external DC power operates. A battery fast-charge controller is provided on-board with a fast-charge indicator (D28), as shown in Figure 2-1.

Figure 2-2. 2.1 mm Socket



The board has a voltage regulator providing +3.3V. The regulator allows the input voltage to range from 7V to 12V. When you switch the power on, the red LED marked POWER lights up. If it does not, switch off and check the power supply connections.

2.6 Measuring Current Consumption on the AT91M42800A

The board is designed to generate the power for the AT91 product, and only the AT91 product, through the jumpers JP5 (V_{DDIO}) and JP8 (V_{DDCORE}). This feature enables measurements of the consumption of the AT91 product to be made.

See Section 5 for further details.

2.7 Testing the AT91EB42 Evaluation Board

To test the AT91EB42 Evaluation Board, perform the following procedure:

1. Hold down the SW1 button and power-up the board, or generate a reset and wait for the light sequence on each LED to complete. All the LEDs light.
2. Release the SW1 button. The LEDs D1 to D8 light up in sequential order. If all the LEDs light up twice, this indicates an error.

The LEDs represent the following test functions:

- D1 for the internal SRAM
- D2 for the external SRAM
- D3 for the external Flash
- D4 reserved
- D5 for the SPI DataFlash®
- D6 reserved
- D7 for the USART
- D8 for ADC with SPI access

During a complete test cycle, each LED flashes once to inform the user that the corresponding function has been successfully tested. If an error is detected, all the LEDs will light up twice. After a complete test cycle, the embedded self-test software called Functional Test Software (FTS) restarts a new cycle.

Section 3

The On-board Software

3.1 AT91EB42 Evaluation Board

The AT91EB42 Evaluation Board embeds an AT49BV162A Flash memory device programmed with default software. Only the lowest 8 x 8 KB sectors are used. The remaining sectors are user definable, and can be programmed using one of the Flash downloader “Flash_16x4” solutions offered in the AT91 Library.

When delivered, the Flash memory device contains:

- the Boot Software Program
- the Functional Test Software (FTS)
- the Flash Uploader
- the power-down function
- the Angel Debug Monitor
- a default user boot with a default application (LED Swing Application)

The Boot Software Program and Functional Test Software (FTS) are in sectors 0 and 1 of the Flash. These sectors are not locked in order to provide an easy on-board upgrade. The user must avoid overwriting these sectors.

3.2 Boot Software Program

The Boot Software Program configures the AT91M42800A, and thus controls the memory and other board components.

The Boot Software Program is started at reset if JP1 is in the STD position. If JP1 is in the USER position, the AT91M42800A boots from address 0x01100000 in the Flash, which must have a user-defined boot.

The Boot Software Program first initializes the master clock frequency at 32.768 MHz. The EBI then executes the REMAP procedure and checks the state of the buttons as described below.

- When the SW1 button is pressed:
  - All the LEDs light up together.
  - The D1 LED remains lit when SW1 is released.
  - The Functional Test Software (FTS) is started.

- When the SW2 button is pressed:
  - Reserved
- When the SW3 button is pressed:
  - All the LEDs light up together.
  - The D3 LED remains lit when SW3 is released.
  - The Flash uploader is activated.
- When the SW4 button is pressed:
  - All the LEDs light up together.
  - The D4 LED remains lit when SW4 is released.
  - The power-down function is activated.
- When no buttons are pressed:
  - Branch at address 0x01006000.
  - The Angel Debug Monitor starts from this address by recopying itself in external SRAM.

3.3 Programmed Default Memory Mapping

Table 3-1 defines the mapping defined by the boot program.

Table 3-1. Memory Map

Part Name	Start Address	End Address	Size	Device
U1	0x01000000	0x011FFFFF	2M Bytes	Flash AT49BV162A
U2 - U3	0x02000000	0x0203FFFF	256K Bytes	SRAM

The Boot Software Program, Functional Test Software (FTS), Flash Uploader and the power-down demonstration are in sectors 0 and 1 of the Flash device. Sectors 3 to 8 support the Angel Debug Monitor.

Sector 24 at address 0x0110 0000 can be programmed with a user application to be debugged. This sector is mapped at address 0x0100 0000 (or 0x0 after a reset) when the jumper JP1 is in the USER position.

3.4 Flash Uploader

The Flash Uploader included in the EB42 Boot Software is the same Flash Uploader factory-programmed in the Flash-based AT91 devices, the AT91FR4042 and the AT91FR40162/S. The Flash Uploader allows programming to Sector 24 of Flash through a serial port. Either of the on-chip USARTs can be used by the Flash Uploader.

To boot from the application downloaded in Sector 24, the downloading address must be 0x01100000. The boot starts the Flash Uploader if the SW3 button is pressed at reset.

The procedure is as follows:

1. Connect the Serial A or B port of the AT91EB42 Evaluation Board to a host PC Serial port using the straight serial cable provided.
2. Start the AT91Loader.exe program available in the AT91 Library on the host computer. The AT91 Loader must be configured beforehand. See the “Readme.pdf” file in folder <CDROM>\ToolBox\host_tools\Dev PC windev\AT91Loader\Doc.

3. Check JP1 is in STD position. Power-on or press RESET, holding down the SW3 button simultaneously. Wait for all LEDs to light up together and then release SW3. LED3 remains lit. If the AT91Loader is configured in automatic mode, the download starts. Wait for the download to end.
4. Put JP1 in USER position and press RESET button. The application downloaded starts.

For further details, see the application note “Crystal Oscillator and PLL Considerations for AT91M42800A and AT91M55800A”, literature number 1740A. A PLL Filter Calculator Tool is also available. See “Automatic_calculation_xls.zip”.

3.5 Power-down Demonstration

The AT91EB42 Evaluation Board is delivered with a battery unit to supply the board when the main power supply is removed. The aim of the power-down demonstration is to save the battery unit. When the power-down function is started, the main clock of the AT91M42800A is switched to the slow clock oscillator at 32.768 kHz. The processor is put in IDLE mode and all peripheral clocks are turned off. The power-down mode is indicated by LED4 flashing every 10 seconds. The boot starts the power-down demonstration if the SW4 button is pressed at reset.

The procedure is as follows:

1. Power-on or press RESET, holding down the SW4 button simultaneously.
2. Wait for all LEDs to light up and then release SW4. LED4 remains lit for 3 seconds and light off. Then LED4 flashes every 10 seconds.
3. Press SW4 or the reset button to re-start the board. When SW4 is pressed, the power-down demonstration re-configures the AT91M42800A to run at 32.768 MHz and branches to Angel.

3.6 Angel Debug Monitor

The Angel Debug Monitor is located in the Flash from 0x01006000 up to 0x01011FFF. The boot program starts it if no button is pressed at reset.

When Angel starts, it recopies itself in SRAM in order to run faster. The SRAM used by Angel is from 0x02020000 to 0x0203FFFF, i.e., the highest half part of the SRAM.

The Angel on the AT91EB42 Evaluation Board can be upgraded regardless of the version programmed on it.

Note that if the debugger is started through ICE while the Angel monitor is on, the Advanced Interrupt Controller (AIC) and the USART channel are enabled.

3.7 Programmed Default Speed

As the speed of the AT91M42800A is programmable, the Boot Software Program initializes the device to run as fast as possible, i.e., at 32.768 MHz. The Boot Software Program and the Functional Test Software are run at this speed. When Angel is started, it also runs at 32.786 MHz and the user should not modify this frequency without reprogramming the speed of the USARTs.

Section 4

Circuit Description

4.1 AT91M42800A Processor

Figure 6-1 on page 6-2 shows the AT91M42800A. The footprint is for a 144-pin TQFP package.

Strap CB20 enables the user to choose between the standard ICE debug mode and the JTAG boundary scan mode of operation.

The operating mode is defined by the state of the JTAGSEL input detected at reset.

Jumper JP5 (see Figure 6-8 on page 6-9 in Section 6, “Appendix B – Schematics”) can be removed by the user to allow measurement of the consumption of the whole microcontroller (V_{DDIO} and V_{DDCORE}). Jumper JP8 can be removed to measure the core microcontroller consumption (V_{DDCORE}).

4.2 Expansion Connectors and JTAG Interface

The two expansion connectors, I/O expansion connector and EBI expansion connector, and the JTAG interface are described below.

The I/O and EBI expansion connectors’ pinout and position are compatible with other AT91 evaluation boards (except the I/O expansion connector pinout and position of the EB40) so that users can connect their prototype daughter boards to any of these evaluation boards.

4.2.1 I/O Expansion Connector

The I/O expansion connector makes the general-purpose I/O (GPIO) lines, VCC3V3 and Ground, available to the user. Configuration straps CB2, CB3, CB4, CB11, CB13, CB14, CB15, CB17, CB18 and CB19 are used to select between the I/O lines being used by the evaluation board or by the user via the I/O expansion connector.

4.2.2 EBI Expansion Connector

The schematic (see Figure 6-4 on page 6-5 in Section 6, “Appendix B – Schematics”) also shows the bus expansion connector. The 32 x 2 connector allows the user to access the data bus, all control bus signals and oscillator output. VCC3V3 and ground are also available on this connector.

Configuration strap CB1, when open, allows the user to connect the EBI expansion connector to the MPI expansion connector of an AT91EB63 evaluation board without any conflict.

4.2.3 JTAG Interface

An ARM®-standard 20-pin box header (P5) is provided to enable connection of an ICE interface to the JTAG inputs on the AT91. This allows code to be developed on the board without using system resources such as memory and serial ports.

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4.3 Memories

The schematic (see Figure 6-3 on page 6-4 in Section 6, "Appendix B – Schematics") shows one AT49BV162A 2M bytes 16-bit Flash, one AT45DB321 4M bytes serial DataFlash, one AT24C512 64K bytes EEPROM, one AT25256 32K Bytes EEPROM and two 128K/512K x 8 SRAM devices.

Note: The AT24C512 64K byte EEPROM and the AT25256 32K byte EEPROM are not mounted.

4.4 Analog-to-digital Converter

An on-board 4-channel, 10-bit ADC device (TLV1504 by Texas Instruments) is featured on the AT91EB42. This device is interfaced to the AT91M42800A via the SPIA peripheral and embeds its voltage reference equal to 2V. Four channels are used on the AT91EB42 for the following measurements:

- Channel 0 is used to measure the temperature near the 32.768 kHz crystal.
- Channel 1 is dedicated to supervise the External Power Supply.
- Channel 2 is dedicated to supervise the Battery Power Supply.
- Channel 3 is dedicated to supervise the V_{DDCORE}.

Each ADC channel is fitted on the I/O extension connector and can be used in other applications. For this reason, each ADC input can be taken away from its function by its appropriate jumper.

4.5 Power and Crystal Quartz

The AT91M42800A master clock is derived from a 32.768 kHz crystal. The on-chip low-power oscillator together with two PLL-based frequency multipliers and the prescaler results in a programmable master clock between 500 Hz and 33 MHz. A temperature sensor has been placed near the 32.768 kHz crystal and the analog signal output has been fitted to Channel 0 of the on-board ADC.

Two sets of components for the PLL filters are fitted by default on the board (see Figure 6-6 on page 6-7 in Section 6, "Appendix B – Schematics"). They are calculated to provide a 16.77 MHz (PLLA: multiplier factor of 512 and settling time of 600 µs) or a 32.768 MHz (PLLB: multiplier factor of 1000 and settling time of 6 ms) master clock frequency.

For further details, see the application note "Crystal Oscillator and PLL Considerations for AT91M42800A and AT91M55800A", literature number 1740A. A PLL Filter Calculator Tool is also available. See "Automatic_calculation_xls.zip".

The voltage regulator provides 3.3V to the board and will light the red POWER LED (D11) when operating.

Power can be applied via the 2.1 mm connector to the regulator in either polarity because of the diode-rectifying circuit. Another regulator allows the user to power the AT91M42800A core with 3.3V or 1.8V by means of the JP8 jumper.

All functions can be supplied by the on-board battery. A connector permits the user to disconnect the battery. The type of battery and connection to be used are shown in Section 6 of this user guide. This type of battery will ensure the power supply of the board for approximately one hour. A battery fast-charge controller is provided on-board to charge it and maintains the full charge. The user is warned while the fast-charge is started via the on-board indicator (D28) or a logical signal on I/O port PB18.

4.6 Push-buttons, LEDs, Reset and Serial Interfaces

The IRQ0, TIOA0, PB6 and PB21 switches are debounced and buffered.

A supervisory circuit has been included in the design to detect and consequently reset the board when the 3.3V supply voltage drops below 3.0V. Note that this voltage can be changed depending on the board production series. The supervisory circuit also provides a debounced reset signal. This device can also generate the reset signal in case of watchdog timeout as the pin NWDOVF of the AT91M42800A is connected to its input $\overline{\text{MR}}$.

The assertion of this reset signal will light up the red RESET LED (D10). By pressing the CLEAR RESET push-button (S1), the LED can be turned off.

Another supervisory circuit initializes separately the microcontroller-embedded JTAG/ICE interface when the 3.3V supply voltage drops below 3.0V. Note that this voltage can be changed, depending on the board production series. These separated reset lines allow the user to reset the board without resetting the JTAG/ICE interface while debugging.

The schematic (see Figure 6-5 on page 6-6 in Section 6, “Appendix B – Schematics”) also shows eight general-purpose LEDs connected to Port B PIO pins (PB8 to PB15).

Two 9-way D-type connectors (P3/4) are provided for serial port connection.

Serial Port A (P3) is used primarily for host PC communication and is a DB9 female connector. TXD and RXD are swapped so that a straight-through cable can be used. CTS and RTS are connected together, as are DCD, DSR and DTR.

Serial Port B (P4) is a DB9 male connector with TXD and RXD obeying the standard RS-232 pinout. Apart from TXD, RXD and ground, the other pins are not connected.

LEDs are connected to the TX and RX signals of both serial ports and show activity on these serial links.

A MAX3223 device (U10) and associated bulk storage capacitors provide RS-232 level conversion.

4.7 Layout Drawing

The layout diagram (see Figure 6-1 on page 6-2 in Section 6, “Appendix B – Schematics”) shows an approximate floor plan for the board. This has been designed to give the lowest board area, while still providing access to all test points, jumpers and switches on the board.

The board is provided with four mounting holes, one at each corner, into which feet are attached. The board has two signal layers and two power planes.

Section 5

Appendix A – Configuration Straps

5.1 Functional Pin Assignment

The following table provides a list of each peripheral used on the AT91EB42 Evaluation Board.

Table 5-1. Functional Pin Assignment

Pin Designation	Function Used on the AT91EB42
NCS0	Chip Select signal for the Flash Memory (AT49BV162A)
NCS1	Chip Select signal for the Static RAMs
PB7/TIOA0	General I/O input line for the User Interface Push-button (SW1)
PA0/IRQ0	General I/O input line for the User Interface Push-button (SW2)
PB6/TCLK0	General I/O input line for the User Interface Push-button (SW3)
PB21/TCLK5	General I/O input line for the User Interface Push-button (SW4)
PB8/TIOB0	General I/O output line for the User Interface Light Indicator (Led D1)
PB9/TCLK1	General I/O output line for the User Interface Light Indicator (Led D2)
PB10/TIOA1	General I/O output line for the User Interface Light Indicator (Led D3)
PB11/TIOB1	General I/O output line for the User Interface Light Indicator (Led D4)
PB12/TCLK2	General I/O output line for the User Interface Light Indicator (Led D5)
PB13/TIOA2	General I/O output line for the User Interface Light Indicator (Led D6)
PB14/TIOB2	General I/O output line for the User Interface Light Indicator (Led D7)
PB15/TCLK3	General I/O output line for the User Interface Light Indicator (Led D8)
PA6/TXD0	To the RS232 Transceiver device and dedicated for the Serial A socket
PA7/RXD0	To the RS232 Transceiver device and dedicated for the Serial A socket
PA9/TXD1/NTRI	To the RS232 Transceiver device and dedicated for the Serial B socket
PA10/RXD1	To the RS232 Transceiver device and dedicated for the Serial B socket
PB18/TCLK4	General I/O input line to detect the fast-charge mode for the battery
PB16/TIOA3	General I/O output line to generate SCL signal dedicated for a two wire bus access

Table 5-1. Functional Pin Assignment (Continued)

Pin Designation	Function Used on the AT91EB42
PB17/TIOB3	General I/O input/output line to generate SDA signal dedicated for a two wire bus access
PA13/MOSIA	To generate SPI bus Access to the DataFlash, EEPROM and ADC devices
PA12/MISOA	To generate SPI bus Access to the DataFlash, EEPROM and ADC devices
PA11/SPCKA	To generate SPI bus Access to the DataFlash, EEPROM and ADC devices
PA14/NPCSA0/NSSA	Chip Select signal for the SPI device: DataFlash
PA15/NPCSA1	Chip Select signal for the SPI device: EEPROM
PA16/NPCSA2	Chip Select signal for the SPI device: ADC
PA3/IRQ3	Interrupt line from the ADC device

5.2 Configuration Straps (CB1 - 23, JP1 - 8)

By adding the I/O and EBI expansion connectors, users can connect their own peripherals to the evaluation board. These peripherals may require more I/O lines than available while the board is in its default state. Extra I/O lines can be made available by disabling some of the on-board peripherals or features. This is done using the configuration straps detailed below. Some of these straps present a default wire (notified by the default mention) that must be cut before soldering the strap.

CB1	On-board PB5/A23/CS4 Signal
Closed(1)	AT91 PB5/A23/CS4 signal is connected to the EBI expansion connector (P1-B21).
Open	AT91 PB5/A23/CS4 signal is not connected to the EBI expansion connector (P1-B21). This authorizes users to connect the EBI expansion connector of this board to the MPI expansion connector of an AT91EB63 Evaluation Board without conflicting problems.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB3	On-board IRQ3 Signal
Closed(1)	AT91 IRQ3 signal is connected to the external ADC (U20 pin 4).
Open	AT91 IRQ3 signal is not connected to the external ADC (U20 pin 4). This authorizes the user to use this signal for other applications via the I/O Expansion connector (P2 - A8).

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB4	ADC Chip Select Line
Closed[1]	ADC (U20) control lines enabled.
Open	ADC (U20) control lines disabled. This authorizes users to connect the corresponding chip select line to their own resources via the I/O expansion connector.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB5	Standard Power Supply Supervisory Enabling
Closed[1]	Standard power supply is supervised by the ADC (U20) channel 1 via a resistor bridge. The ratio is set to 0.1013 so that the standard power supply can be supervised up to 15V.
Open	Standard power supply is not connected to the ADC (U20) channel 1. This allows the user to connect the corresponding ADC channel to their own resources via the I/O expansion connector.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB6	VDDCORE Voltage Monitoring
Closed[1]	The ADC channel 3 is connected at the V_{DDCORE} power supply. This allows the user to tune the frequency clock according to the core voltage.
Open	The ADC channel 3 is not connected and it is available on the I/O expansion connector for user application.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB7	Battery Power Supply Supervisory Enabling
Closed[1]	Battery power supply is supervised by the ADC (U20) channel 2 via a resistor bridge. The ratio is set to 0.24 so that the battery voltage range can be supervised (5.5V to 6.2V).
Open	Battery power supply is not connected to the ADC (U20) channel 2. This authorizes the user to connect the corresponding ADC channel to their own resources via the I/O expansion connector.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB8	Ambient Temperature Monitoring
Closed[1]	The ADC channel 0 is connected to a temperature sensor near the 32.768 kHz crystal. This allows the user to evaluate the frequency drift according to the ambient temperature.
Open	The ADC channel 0 is not connected and it is available on the I/O expansion connector for the user application.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB9	On-board Boot Chip Select
Closed[1]	AT91 NCS0 select signal is connected to the Flash memory.
Open	AT91 NCS0 select signal is not connected to the Flash memory. This authorizes the user to connect the corresponding select signal to their own resources via the EBI expansion connector.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB10	Flash Reset
Closed[1]	The on-board reset signal is connected to the Flash NRESET input.
Open	The on-board reset signal is not connected to the Flash NRESET input.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB12	Boot Mode Strap Configuration
Open[1]	BMS AT91 input pin is set for the microcontroller to boot on an external 16-bit memory at reset.
Closed	BMS AT91 input pin is set for the microcontroller to boot on an external 8-bit memory at reset.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB13, CB14	Two-wire Interface EEPROM Enabling
Closed[1]	EEPROM communication enabled.
Open	EEPROM communication disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB15	Serial DataFlash Enabling
Closed[1]	AT91 NPCSA0 select signal is connected to the serial DataFlash memory.
Open	AT91 NPCSA0 select signal is not connected to the serial DataFlash memory. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB16	Control Line for the Internal Oscillator
Closed	Disables the internal low frequency oscillator.
Open[1]	Enables the internal oscillator.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB17	**SPI EEPROM Enabling**
Closed[1]	EEPROM communication enabled.
Open	EEPROM communication disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB18	**R(eturn) TCK ICE Signal Synchronization**
1 - 2[1]	The TCK and RTCK ICE signals are not synchronized with MCKO.
2 - 3	The TCK signal from the JTAG interface can be synchronized with the MCKO signal and returns to the JTAG interface (RTCK).

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB19	**PB18 End of Fast Charge Signal**
Closed[1]	AT91 PB18 signal is connected to the battery charger (U16), NFASTCHG output pin.
Open	AT91 PB18 signal is not connected to the battery charger (U16), NFASTCHG output pin. This authorizes users to connect the corresponding signal to their own resources via the I/O expansion connector.

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB20	**JTAGSEL**
1 - 2[1]	AT91 standard ICE debug feature enabled
2 - 3	IEEE 1149.1 JTAG boundary scan feature enabled

Note: 1. Hardwired default position: To cancel this default configuration, the user should cut the wire on the board.

CB21, CB22, CB23	**Charger Device (U16): Programming the Battery Number of Cells**		
Number of Cells	**CB21**	**CB22**	**CB23**
1	Open	Closed	Closed
2	Open	Open	Closed
4	Closed	Open	Closed
5[1]	Open	Closed	Open
6	Open	Open	Open
8	Closed	Open	Open

JP1	User or Standard Boot Selection
2 - 3	The first half part of the Flash memory is accessible at its base address.
1 - 2	The second half part of the Flash memory is accessible at its base address. This authorizes users to download their own application software in this part and to boot on it.

JP2	Push Button Enabling
Open	SW1-4 inputs to the AT91 are valid.
Closed	SW1-4 inputs to the AT91 are not valid. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

JP3	User or Standard Boot Selection
Open	The RS-232 transceivers are enabled.
Closed	The RS-232 transceivers are disabled. This authorizes users to connect the corresponding PIO to their own resources via the I/O expansion connector.

JP4	PME Function (Protect Mode Enable)
Closed	The AT91M42800A is in Protect Mode.
Open	This is the default mode on the AT91EB42. The AT91M42800A internal registers are accessible in all processor modes.

JP8	Core Power Supply Selection
2 - 3	The AT91 core is powered by 3.3V power supply.
1 - 2	Not supported on the current microcontroller revision.

5.3 Power Consumption Measurement Strap (JP5)

The JP5 strap enables connection of an ammeter to measure the AT91M42800A global consumption (V_{DDCORE} and V_{DDIO}) when V_{DDCORE} power supply is derived from V_{DDIO} (JP8 in 3V3 position). Core consumption can be measured by connecting another ammeter between JP8 1 - 2 or 2 - 3, depending on the power supply used to power the core.

5.4 Ground Links (JP6)

The JP6 strap allows the user to connect the electrical and mechanical grounds.

5.5 Increasing Memory Size

The AT91EB42 Evaluation Board is supplied with two 128K x 8 SRAM memories. If, however, the user needs more than 256K bytes of memory, the devices can be replaced with two 512K x 8 3.3V 10/15 ns SRAMs, giving a total of 1024K bytes. The following references for the 512K x 8 SRAM are available.

Manufacturer	Reference
Samsung	KM68V4002BJ-15 in 36-SOJ-400 package
IDT	71V424-15 in 36-pin 400-mil SOJ package (SO36-1)

Section 6

Appendix B – Schematics

6.1 Schematics

The following schematics are appended:

- Figure 6-1 – PCB Layout
- Figure 6-2 – AT91EB42 Blocks Overview
- Figure 6-3 – EBI Memories
- Figure 6-4 – I/O and EBI Expansion Connectors
- Figure 6-5 – Push-buttons, LEDs and Serial Interface
- Figure 6-6 – AT91M42800A
- Figure 6-7 – Reset and JTAG Interface
- Figure 6-8 – Power Supply and Battery Charger
- Figure 6-9 – SPI Memories, Two-wire Interface Memories and SPI ADC

The pin connectors are indicated on the schematics:

- P1 = EBI Expansion Connector (Figure 6-4)
- P2 = I/O Expansion Connector (Figure 6-4)
- P3 = Serial A (Figure 6-5)
- P4 = Serial B (Figure 6-5)
- P5 = JTAG Interface (Figure 6-7)

Figure 6-1. PCB Layout

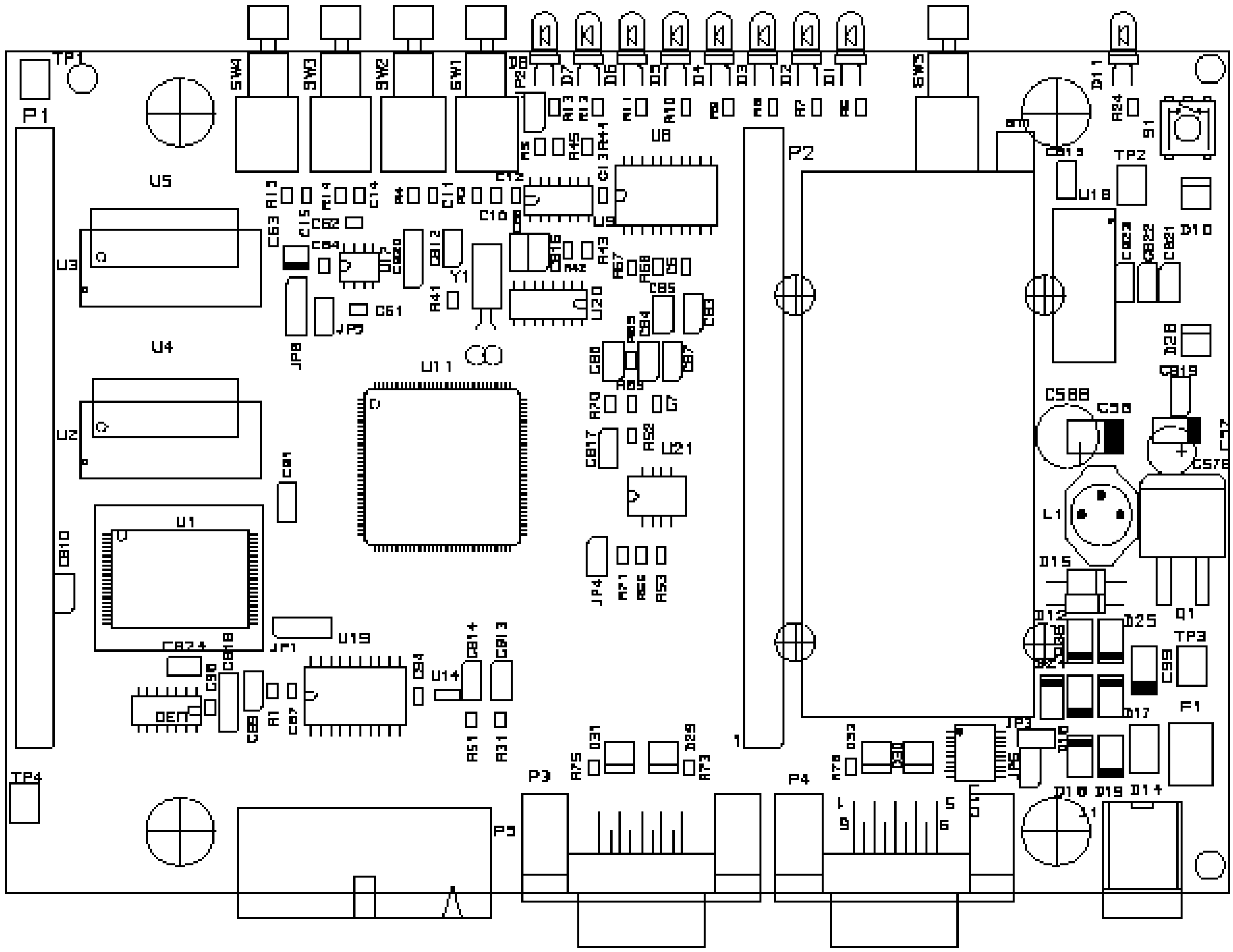


Figure 6-2. AT91EB42 Blocks Overview

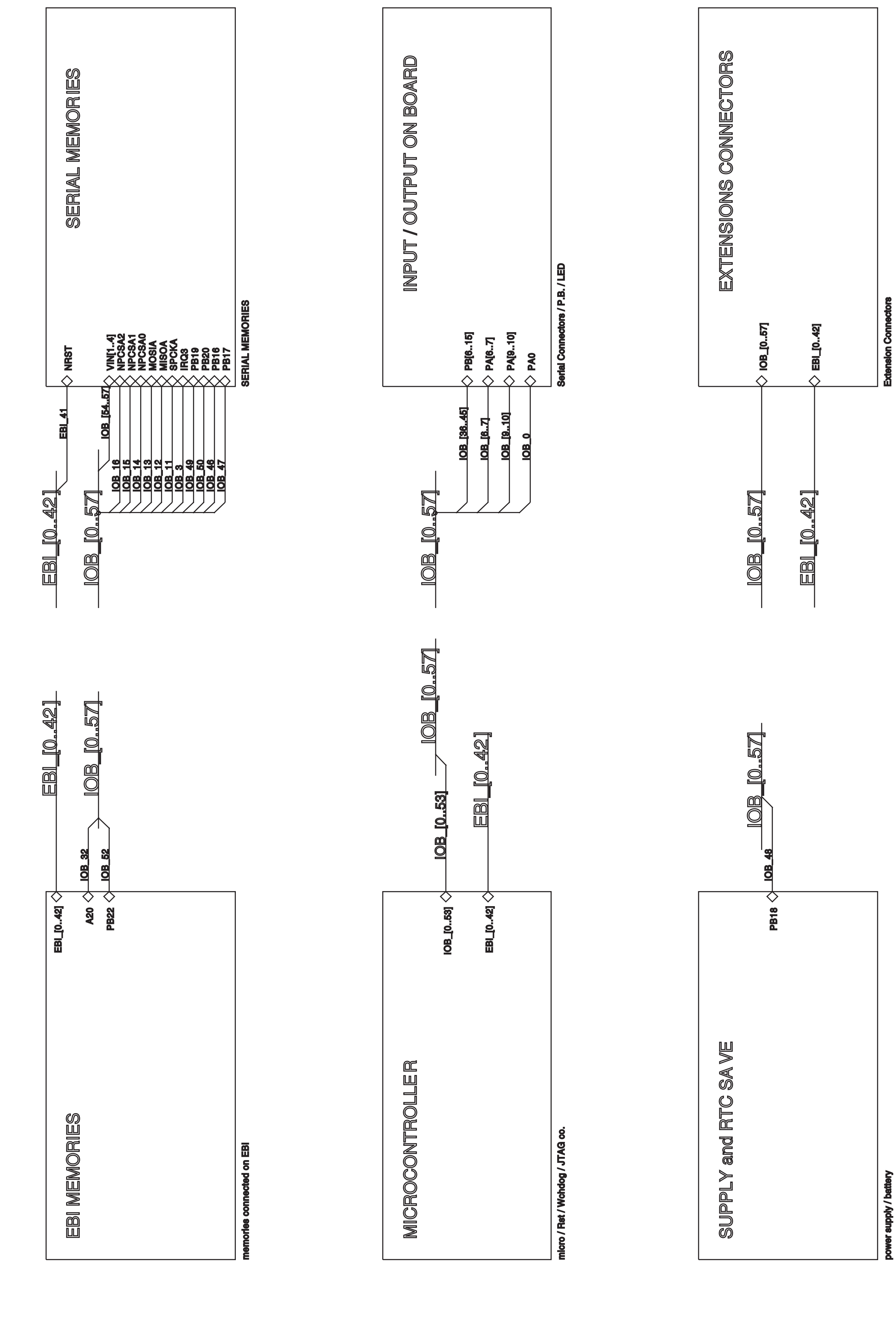


Figure 6-3. EBI Memories

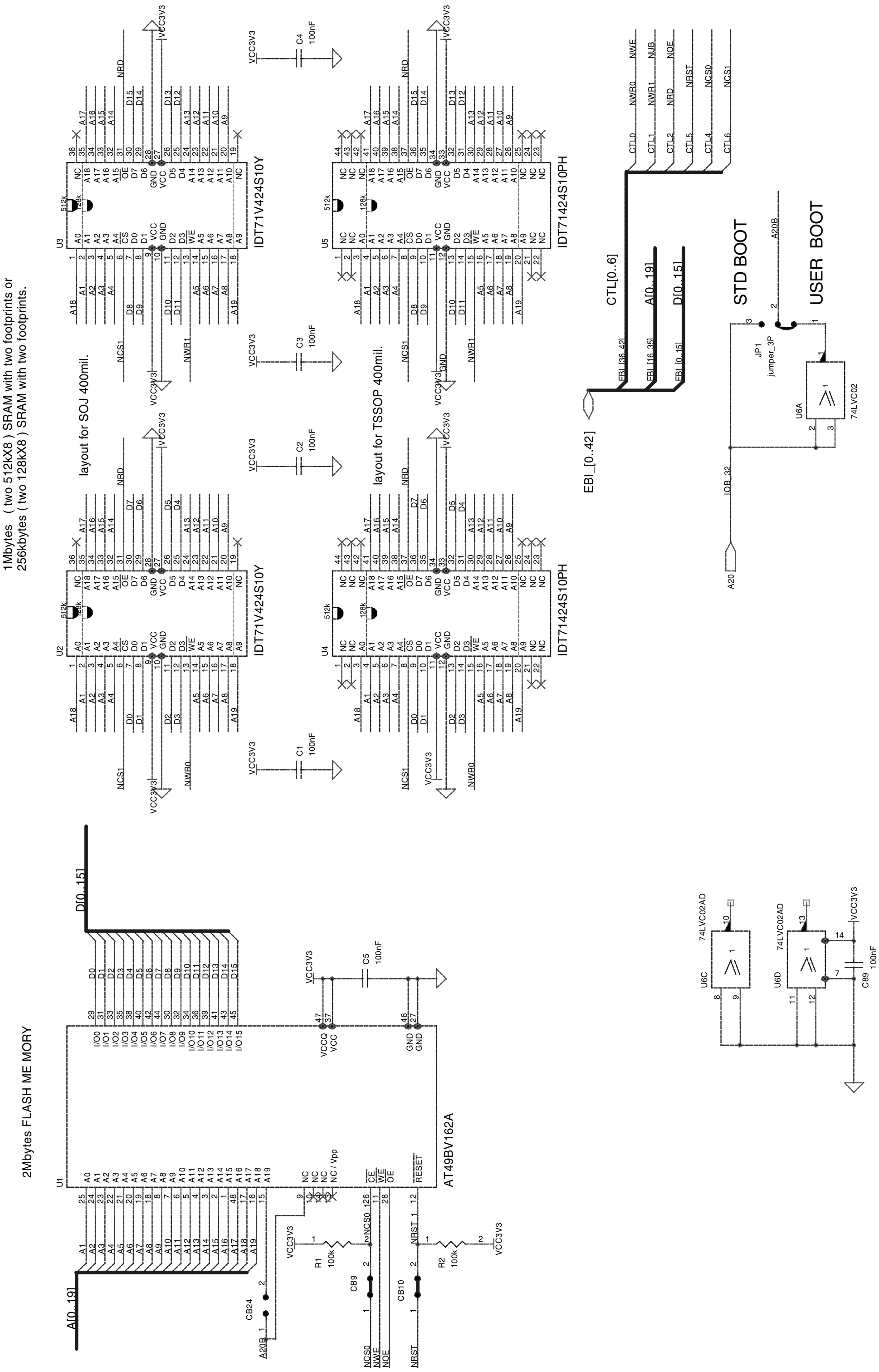


Figure 6-4. I/O and EBI Expansion Connectors

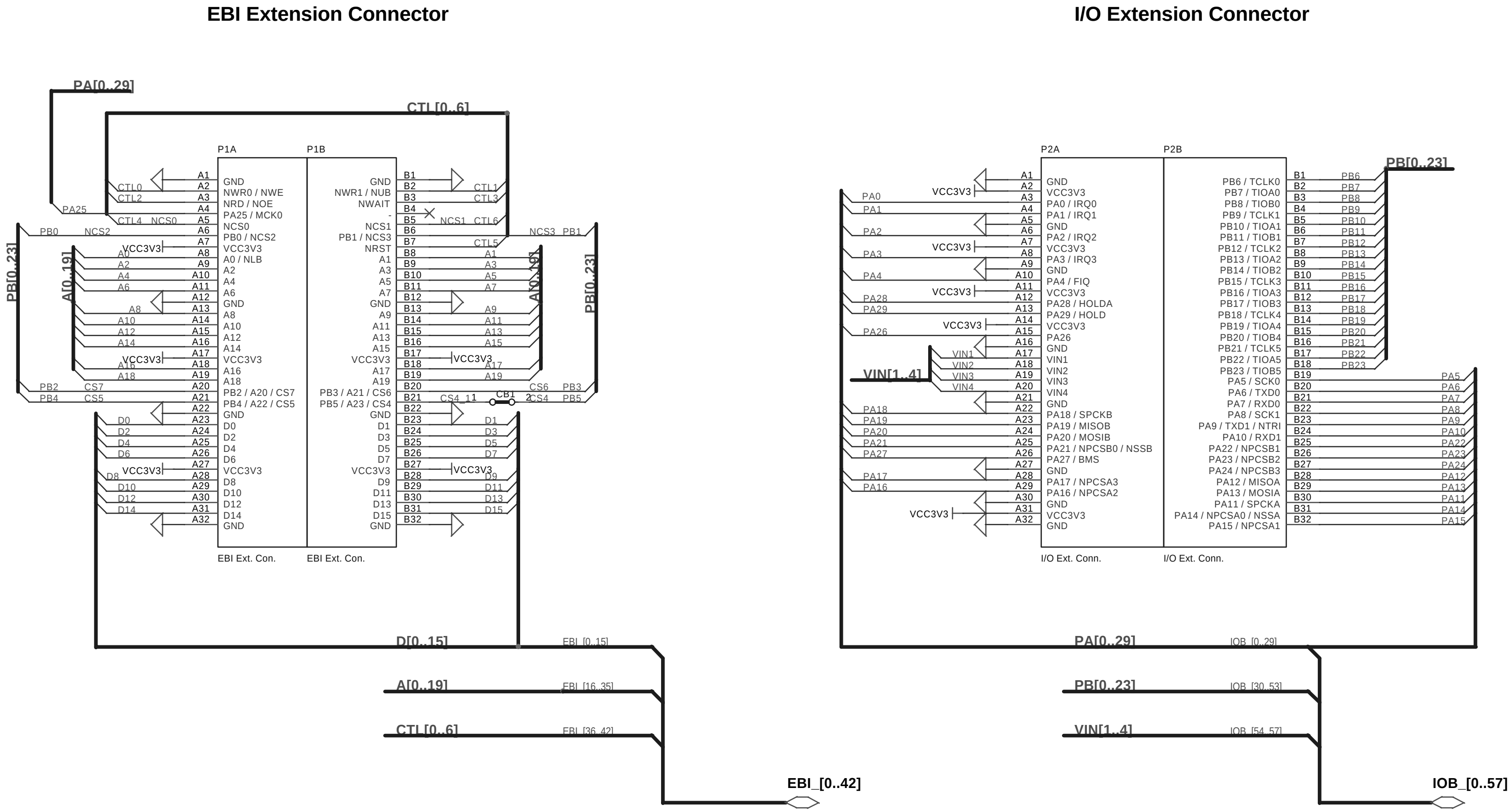


Figure 6-5. Push-buttons, LEDs and Serial Interface

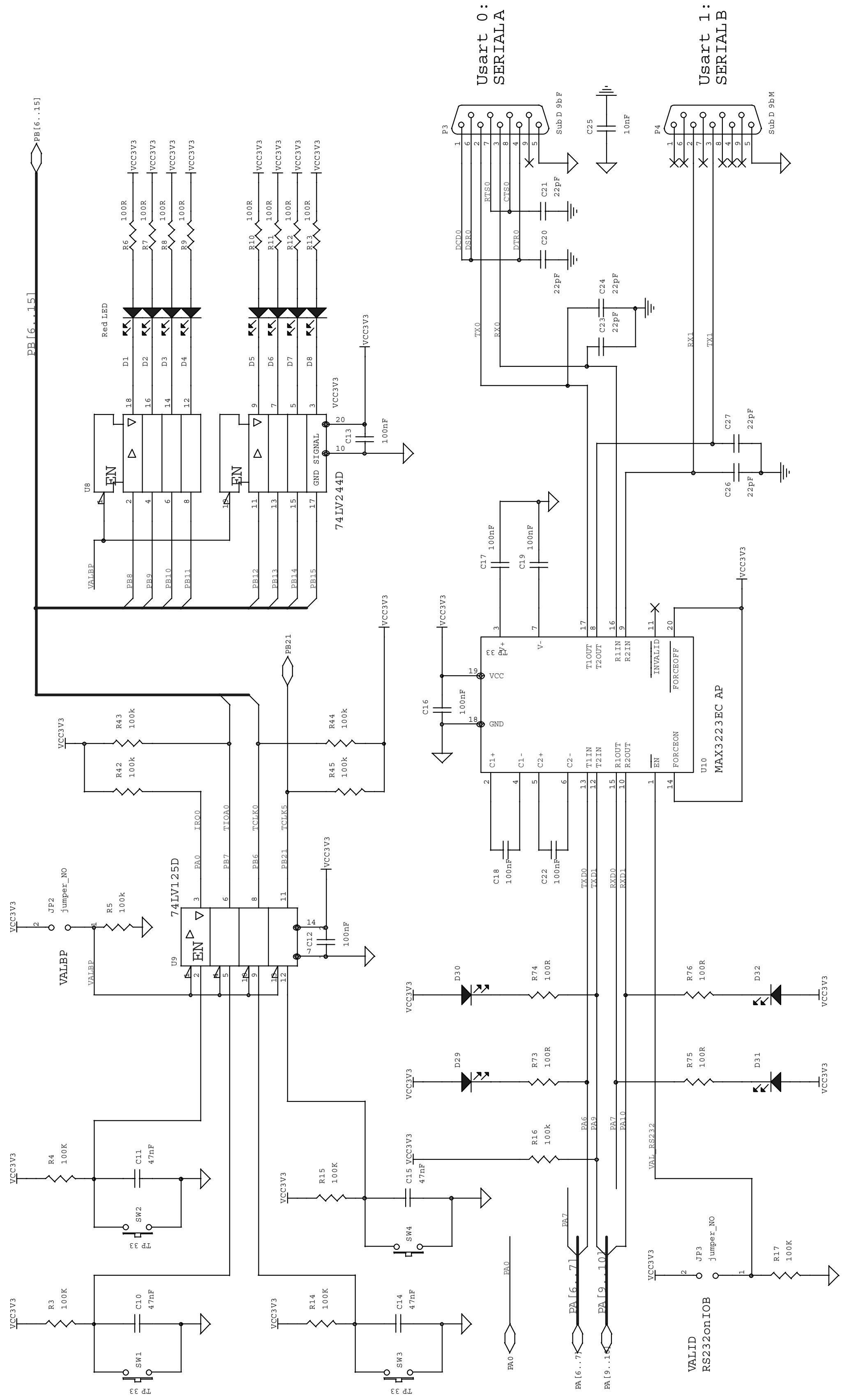


Figure 6-6. AT91M42800A

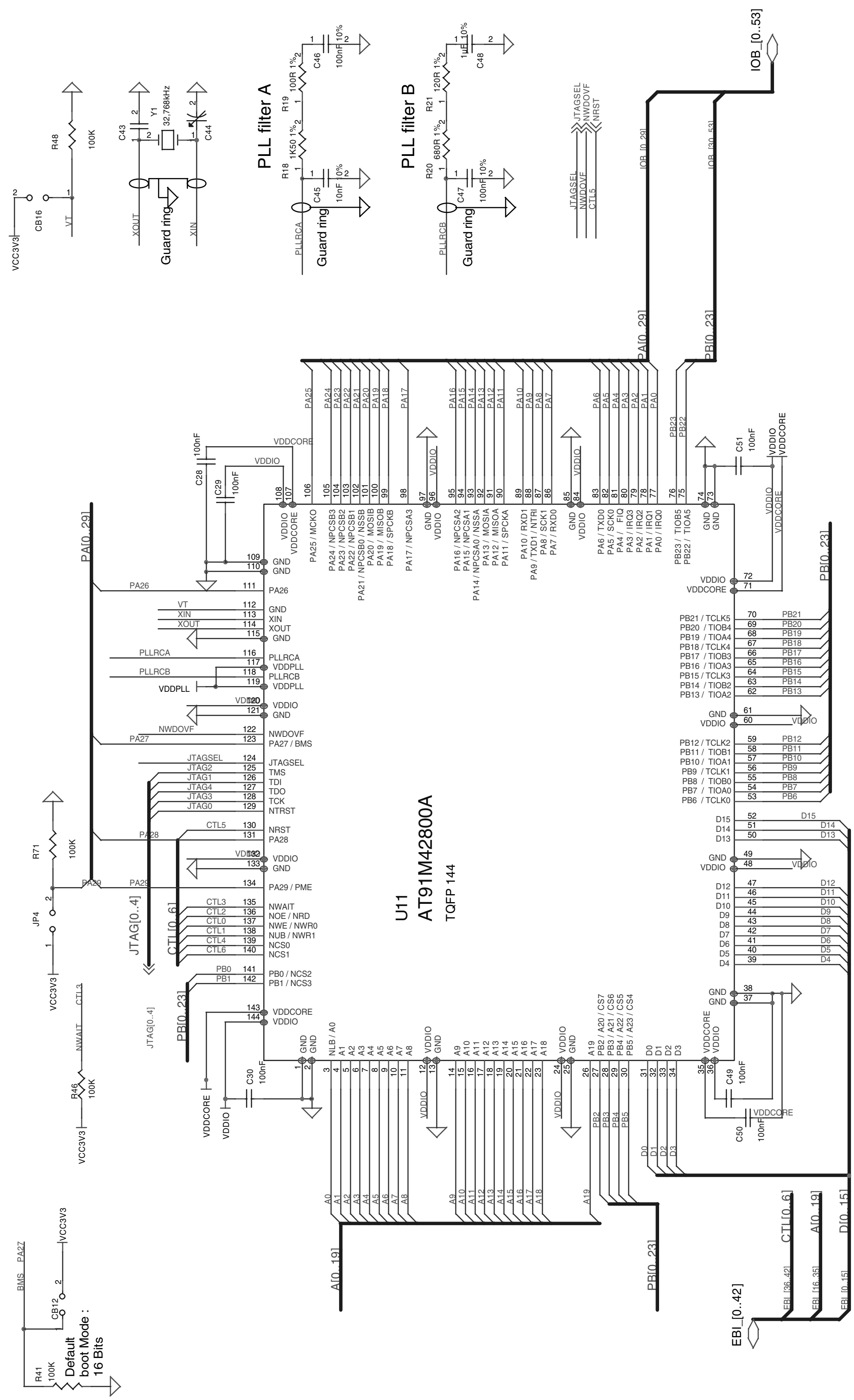


Figure 6-7. Reset and JTAG Interface

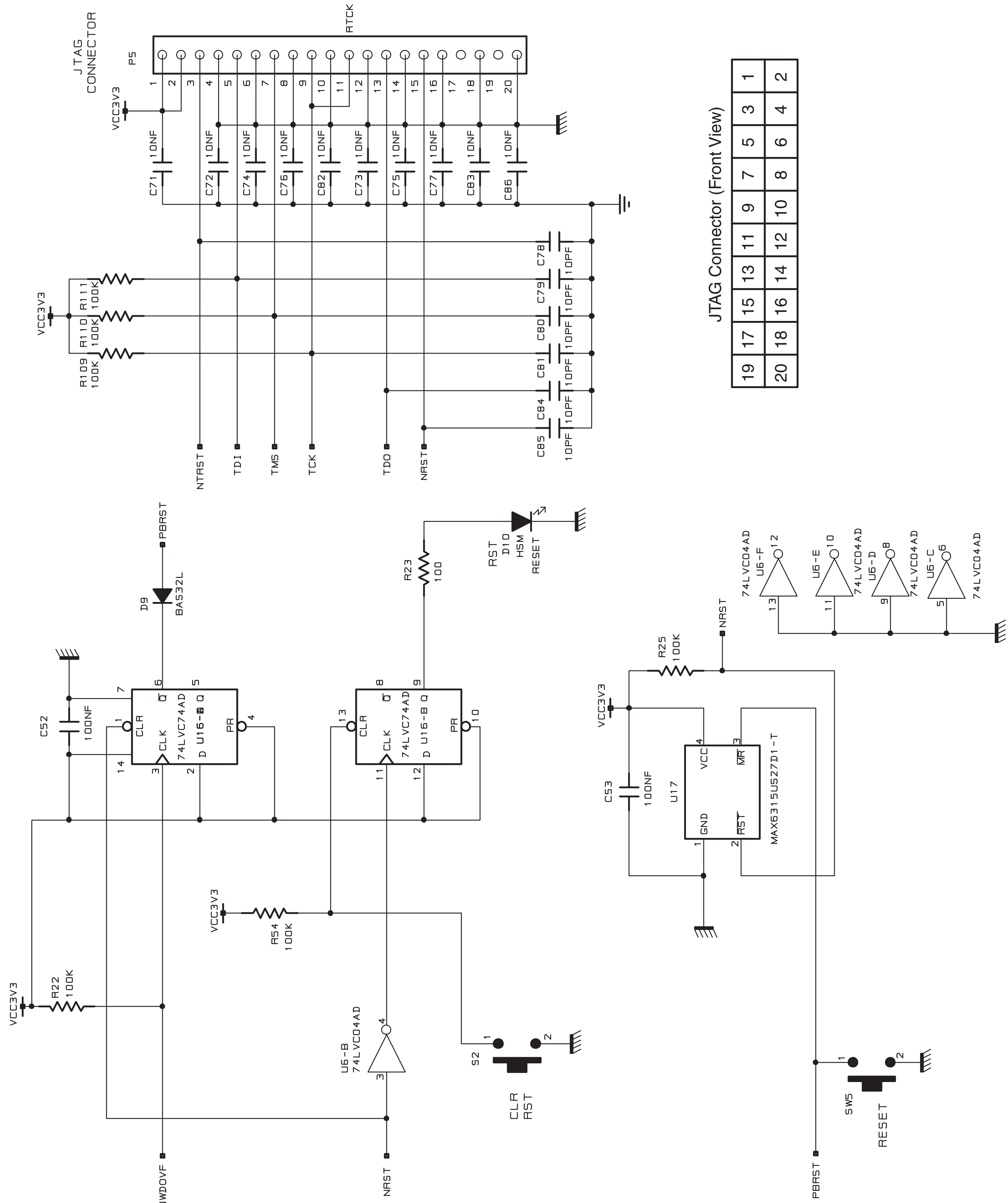


Figure 6-8. Power Supply and Battery Charger

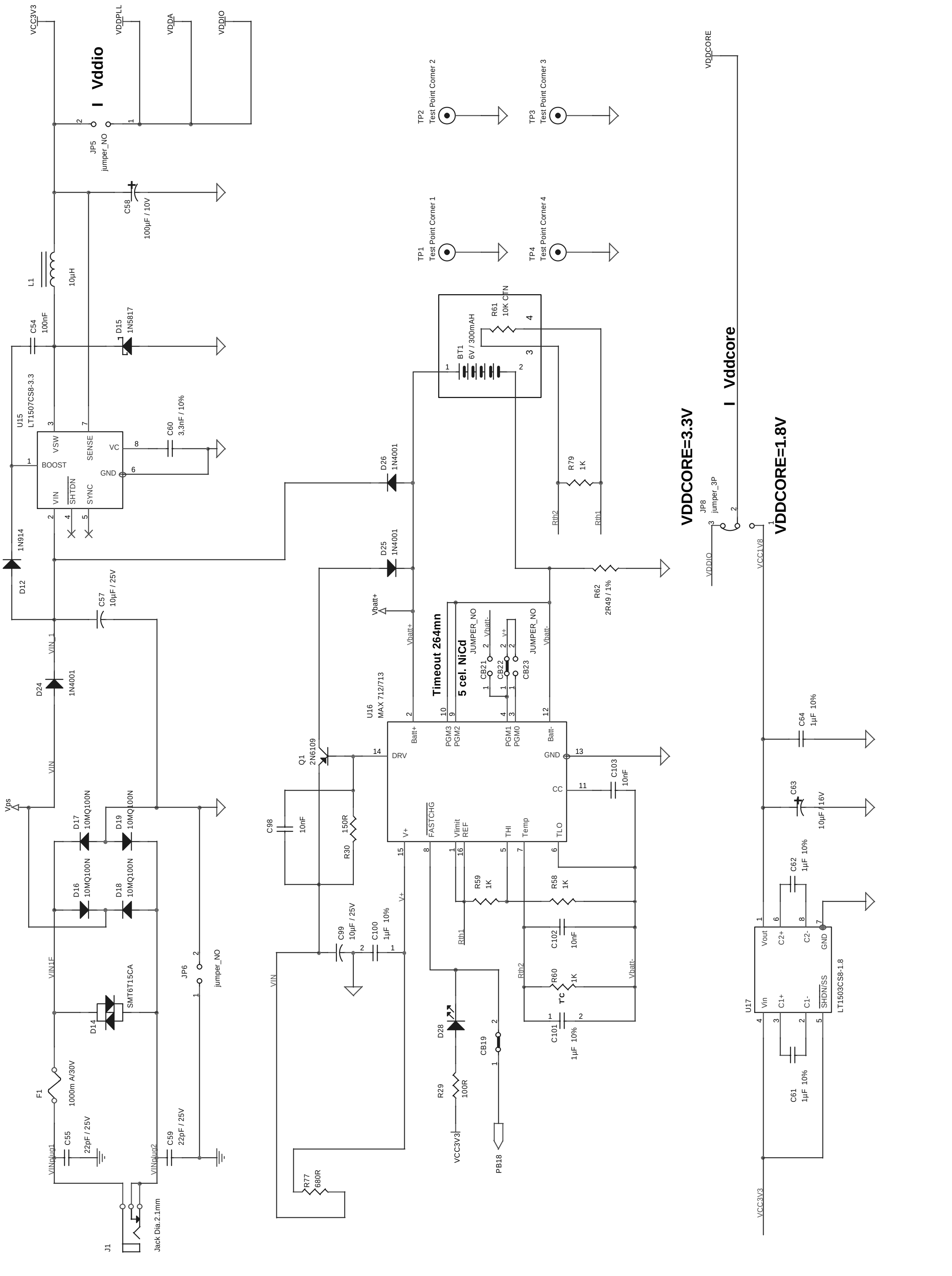
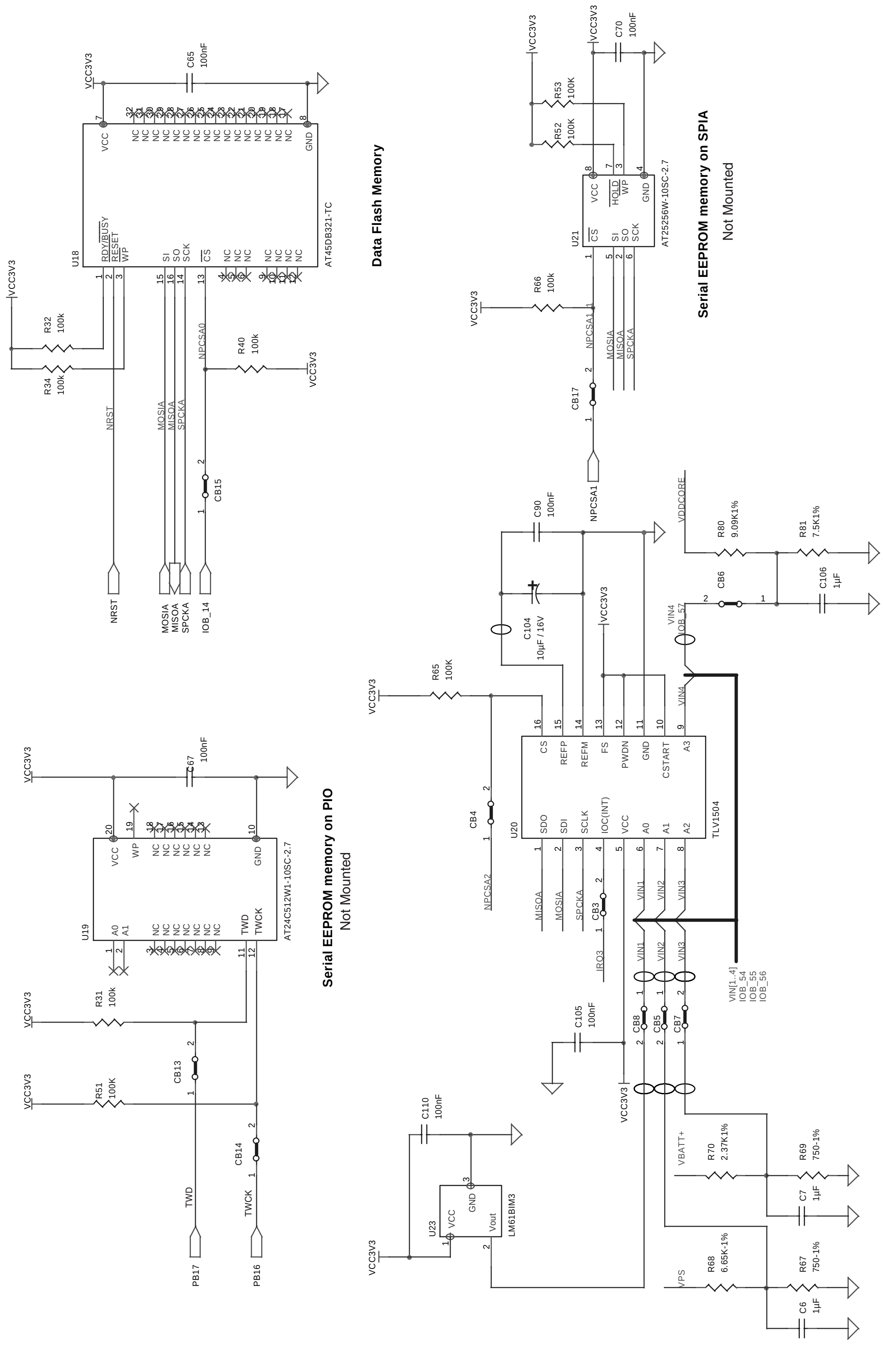


Figure 6-9. SPI Memories, Two-wire Interface Memories and SPI ADC



Section 7

Appendix C – Bill of Materials

Figure 7-1. Bill of Materials for AT91EB42

Item	Qty.	Reference	Part	Designation	Manufacturer
1	1	BT1	6V battery	NiCd pack battery 6V – 300 mAh	Saft
2	2	JP1, JP8	3-point jumper	Jumper	
3	2	JP4, JP5	2-point	Jumper	
4		CB24(*)	2-point strap	Soft-soldering jumper	
5	30	C1, C2, C3, C4, C5, C12, C13, C16, C17, C18, C19, C22, C28, C29, C30, C49, C50, C51, C52, C53, C54, C65, C67, C70, C89, C90, C94, C96, C105, C110	100 nF	Ceramic Y5 10V	AVX
6	3	C6, C7, C106	1 µF	Ceramic Y5V 10V	AVX
7	4	C10, C11, C14, C15	47 nF	Ceramic X7R 10V	AVX
8	5	C20, C21, C23, C24, C26, C27	22 pF	Ceramic NPO 10V	AVX
9	14	C25, C71, C72, C73, C74, C75, C76, C77, C82, C83, C86, C98, C102, C103	10 nF	Ceramic X7R 16V	AVX
10	7	C43, C78, C79, C80, C81, C84, C85	10 pF	Ceramic NPO 10V 5%	AVX
11	1	C44	4 - 25 pF	Varicap. serie TZBX4	MURATA
12	1	C45	10 nF	CeramicX7R 10V 10%	AVX
13	2	C46, C47	100 nF	CeramicX7R 10V 10%	AVX
14	3	C48, C100, C101	1 µF	CeramicX7R 10V 10%	AVX
15	2	C55, C59	22 pF	CeramicX7R 25V	AVX
16	2	C57, C99	10 µF	Tantalum (TPS ou OS-CON) 25V ESR < 0.5Ω	AVX
18	1	C58	100 µF	Tantalum (TPS ou 593D) 10V ESR < 0.5Ω	AVX
20	1	C60	3.3 nF	Ceramic X7R/25V/10%	SIEMENS
21	3	C61, C62, C64	1 µF	CeramicX7R 10V 10%	AVX
22	2	C104, C63	10 µF	Tantalum 16V 10% TAJ	AVX
23	9	D1, D2, D3, D4, D5, D6, D7, D8, D11	Red LED	Red LED H.R. 3mm T1 7mcd 60°	HP

Figure 7-1. Bill of Materials for AT91EB42 (Continued)

Item	Qty.	Reference	Part	Designation	Manufacturer
24	2	D10, D28	Red LED	Red CMS LED	HP
25	2	D30, D29	Orange LED	SMT Orange LED	HP
26	2	D32, D31	Green LED	SMT Green LED	HP
27	1	D12	1N914	Diode	Fairchild
28	1	D14	SMT6T15CA	Transil 12.8V/600W/VBRmin. 14.3V	ST
29	1	D15	1N5817	Schottky 1A/0.45V	ST
30	7	D16, D17, D18, D19, D24, D25, D26	10MQ100N	Rectifier diode 0.62V/0.77A	I.R.
31	1	F1	1000 mA/30V	Fuse rarm 1000 mA/30V	Polyswitch
32	1	J1	Jack diam. 2.1mm	Jack socket diam. 2.1 mm	LUMBERG
33	1	L1	10 µH	Self 10 µH @ 1A and 500 kHz	COILCRAFT
34	1	P3	Sub D 9b F	Sub D 9b F, female socket, right angle, mechanical strength, locking	ETEC
35	1	P4	Sub D 9b M	Sub D 9b M, male socket, right angle, mechanical strength, locking	ETEC
36	1	P5	HE10 2x10	HE10 2 x 10, low-profile	T&B
37	1	Q1	MJD45H11	Transistor PNP	MOTOROLA
38	29	R1, R2, R3, R4, R5, R14, R15, R16, R17, R25, R27, R31, R32, R34, R40, R41, R42, R43, R44, R45, R46, R48, R51, R52, R53, R65, R66, R71, R78	100K	Resistors @ 5%	Vishay
39	15	R6, R7, R8, R9, R10, R11, R12, R13, R23, R24, R29, R73, R74, R75, R76	100R	Resistor @ 5%	Vishay
40	1	R18	1K50 1%	Resistor @ 1%, 125 mW	Vishay
41	1	R19	100R 1%	Resistor @ 1%, 125 mW	Vishay
42	1	R20	680R 1%	Resistor @ 1%, 125 mW	Vishay
43	1	R21	120R 1%	Resistor @ 1%, 125 mW	Vishay
44	1	R30	150R	Resistor @ 1%, 125 mW	Vishay
45	1	R58	10K	Resistor @ 1%, 125 mW	Vishay
46	1	R59, R60, R79	1k	Resistor @ 1%, 125 mW	Vishay
47	1	R61	10K CTN	Therm. CTN 10k @ 25°C, B = 3730°K	SIEMENS
48	4	R62d, R62c, R62b, R62a (****)	10R	Resistor 0.25W 5% RC01	
49	1	R67	7.5K1%	Resistor @ 1%, 125 mW	Vishay
50	1	R68	66.5K1%	Resistor @ 1%, 125 mW	Vishay
51	1	R69	31.6K1%	Resistor @ 1%, 125 mW	Vishay
52	1	R70	100K1%	Resistor @ 1%, 125 mW	Vishay
53	1	R77 (****)	6R8	Resistor @ 1%, 125 mW	Vishay
54	1	R80	90.9K1%	Resistor @ 1%, 125 mW	Vishay
55	1	R81	75K1%	Resistor @ 1%, 125 mW	Vishay
56	4	SW1, SW2, SW3, SW4	TP 33	Push-button with black cap	APEM

Figure 7-1. Bill of Materials for AT91EB42 (Continued)

Item	Qty.	Reference	Part	Designation	Manufacturer
57	1	SW5	TP 33	Push-button with red cap	APEM
58	1	S1	B.P.	SMT Push-button	J.RENAUD
59	4	TP1, TP2, TP3, TP4	Test Point Corner	SMT Test point	
60	1	U1(1)	AT49BV162A-70TI	2-Mbyte x 16-bit Flash	Atmel
61	2	U3, U2(2)	IDT71V424S10Y	Static memory: 128K x 8 - 15 ns/36-pin 400 mil SOJ	IDT
62	2	U5, U4(2)	IDT71424S10PH	Static memory: 128K x 8 - 15 ns/44-pin TSOP Type II	IDT
63	1	U6	74LVC02AD	QUAD 2-INPUT NOR Gate	TI Philips
64	1	U8	74LV244D	Buffer	TI Philips
65	1	U9	74LV125D	Tri-state buffer	TI Philips
66	1	U10	MAX3223ECAP	Driver RS232 + ESD “E”	MAXIM
67	1	U11	AT91M42800A	32-bit Arm/Thumb Microcontroller	Atmel
68	1	U12	74LVC74AD	D flip-flop (LVC Serial)	TI Philips
69	2	U13, U14	MAX6315US30D4-T	Circuit LVD-reset	Maxim
70	1	U15	LT1507CS8-3.3	Voltage Regulator DC/DC	Linear Technology
71	1	U16	MAX 712/713	NiCd/NiMH Battery Fast-charge Controllers	MAXIM
72	1	U17	LTC 1503CS8-2	Voltage Regulator DC/DC	Linear Technology
73	1	U18(3)	AT45DB321-TC	Serial DataFlash	Atmel
75	1	U20	TLV1504	4 analog-to-digital converter with SPI protocol (D package)	TI
77	1	U23	LM61BIM3	2.7V, SOT-23 Temperature Sensor	NS
78	1	U30	74LCX74	D flip-flop (LCX serie)	TI Philips
79	1	Y1	32,768kHz	Crystal 32.768 kHz/50 ppm	MICRO CRYSTAL
80	2	P1, P2	2 x 32 male	HE10 Header 2.54 mm	FCI
81	4	R62d, R62c, R62b, R62a	14R7	Resistor 0.25W 5% RC01	
82	1	R77	680	Resistor 0.25W 5% RC01	Vishay
83	2	P1, P2	2 x 32-point, male	HE13 Header 2.54 mm	FCI
84	4	R62d, R62c, R62b, R62a	14R7	Resistor 0.25W 5% RC01	
85	1	Socket to be bonded to BT1(4)	4-point socket, male	2.54 mm pitch KK® vertical friction lock header, series 6410/7395	Molex
86	1	Connector to supply battery(1)	4-point connector, female	2.54 mm pitch KK crimp terminal housing, series 6471	Molex

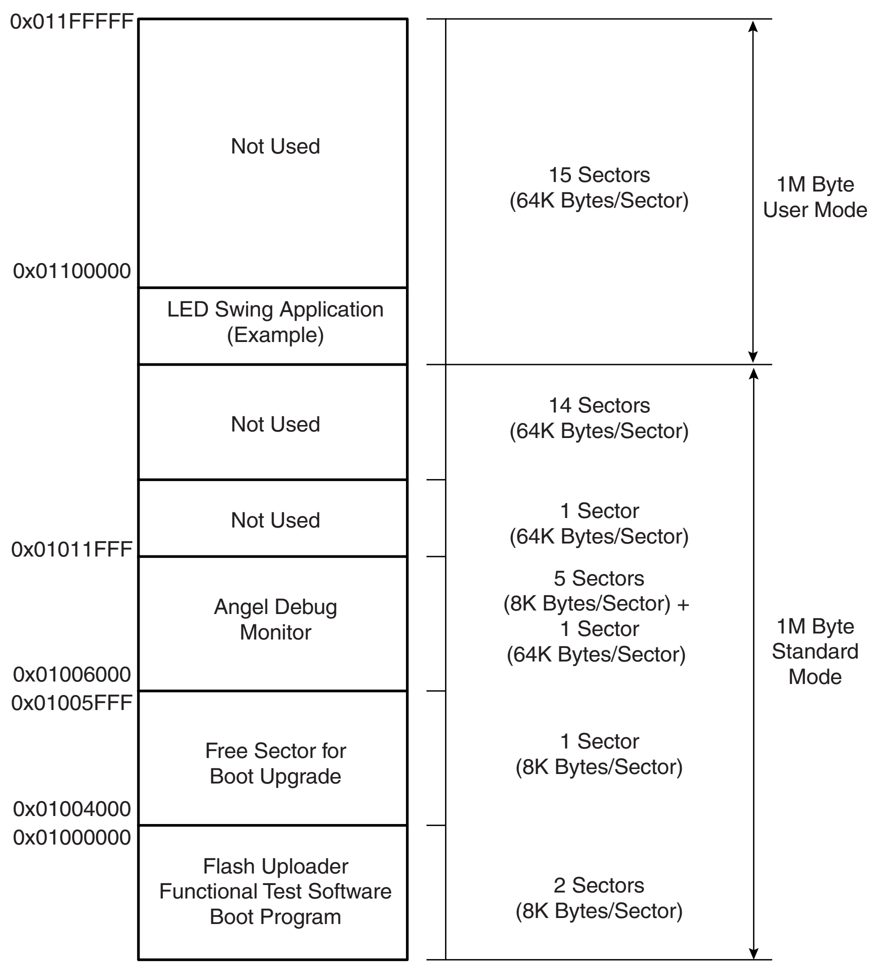
Notes:
1. The AT91EB42 board is equipped with SRAM U2/U3 or U4/U5. The difference is in the type of case used. The selection is made based on availability.
2. U18 is wired according to availability.
3. Cannot be seen in Figure 6-1.

Section 8

Appendix D – Flash Memory Mapping

Figure 8-1 shows the embedded software mapping after the remap. It describes the location of the different programs in the AT49BV162A Flash memory and the division into sectors.

Figure 8-1. EB42 Flash Memory Software Mapping



Rev. 1708C–ATARM–12-May-05

Document Details

Title	AT91EB42 Evaluation Board User Guide
Literature Number	1708

Revision History

Version C	**Publication Date**: 12-May-05
Revisions since last issue	
All pages	Removed all references to SRAM Downloader Removed all references to two-wire interface Changed all occurrences of AT49B1604(A) or AT49BV1614(A) or AT49BV16x4 to AT49BV162A.
Section 1.3	Removed references to: 64K bytes of EEPROM with two-wire access 32K bytes of SPI EEPROM
Fig.1-1	Removed the 2 "SERIAL EEPROM" boxes
Section 2.7	Changed - D4 for the EEPROM with two-wire access to D4 reserved - D6 for the SPI EEPROM to D6 reserved
Section 3.2	Replaced the description of "When SW2 button is pressed" by Reserved
Section 3.4	Removed
Section 3.5	Replaced AT91F40816 and AT91FR4081 by AT91FR4042 and AT91FR40162/S
Section 4.3	Added note: The AT24C512 64K byte EEPROM and the AT25256 32K byte EEPROM are not mounted.
Appendix A	Removed the table describing CB24
Figure 6-3	EBI Memories Changed AT49BV16X4-90TC to AT49BV162A for U1 part.
Figure 6-9	Changed figure names into SPI and TWI Memories. For U19 & U21 part: Add note NOT MOUNTED
Table 7-1	Removed items 74 & 76 Item 60 / "Part" Column --> changed to AT49BV162A-70TI

Figure 8-1	Updated with new memory sizes

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