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NO RECOMMENDED REPLACEMENT
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12MHz Rail-to-Rail Input-Output Operational Amplifier

EL5120T

The EL5120T is a high voltage rail-to-rail input-output amplifier with low power consumption. The EL5120T is a single amplifier that exhibits beyond the rail input capability, rail-to-rail output capability, and is unity gain stable.

The operating voltage range is from 4.5V to 19V. It can be configured for single or dual supply operation, and typically consumes only 750µA. The EL5120T has an output short circuit capability of ±200mA and a continuous output current capability of ±70mA.

The EL5120T features a slew rate of 12V/µs. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 12MHz (-3dB). This enables the amplifier to offer maximum dynamic range at any supply voltage. These features make the EL5120T an ideal amplifier solution for use in TFT-LCD panels as a V_{COM} or static gamma buffer, and in high speed filtering and signal conditioning applications. Other applications include battery power and portable devices, especially where low power consumption is important.

The EL5120T is available in small 5 Ld TSOT package. It features a standard operational amplifier pinout. The device operates over an ambient temperature range of -40°C to +125°C.

Features

- 750µA supply current
- 12MHz (-3dB) bandwidth
- 4.5V to 19V maximum supply voltage range
- 12V/µs slew rate
- ±70mA continuous output current
- ±200mA output short circuit current
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- Built-in thermal protection
- -40°C to +125°C ambient temperature range
- Pb-free (RoHS compliant)

Applications

- TFT-LCD panel - tablet, monitor, notebook
  - V_{COM} amplifier, static gamma buffer, panel repair
- Electronic notebooks, games
- Touch-screen displays
- Personal communication devices, digital assistants (PDA)
- Portable instrumentation
- Sampling ADC amplifiers
- Wireless LANs
- Office automation
- Active filters
- ADC/DAC buffer

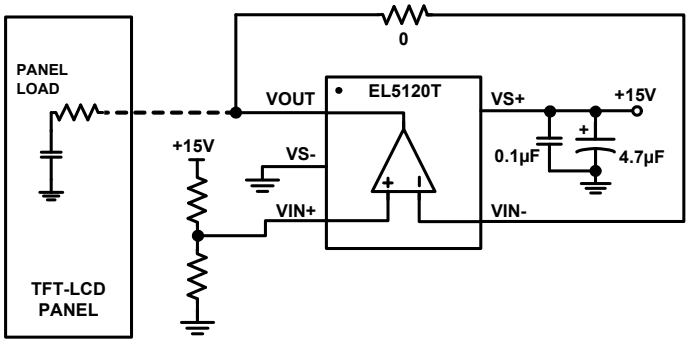


FIGURE 1. TYPICAL TFT-LCD V_{COM} APPLICATION

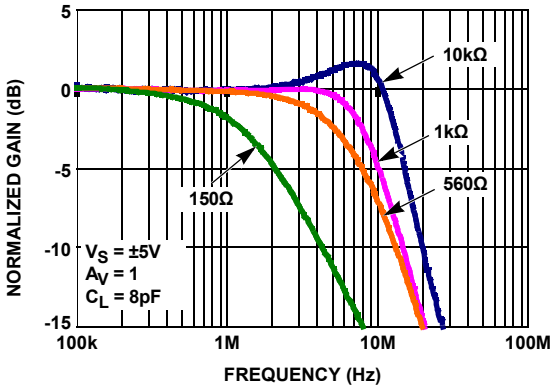
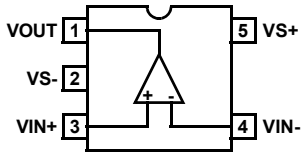


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS R_L

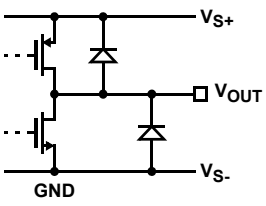
Pin Configuration

EL5120T
(5 LD TSOT)
TOP VIEW

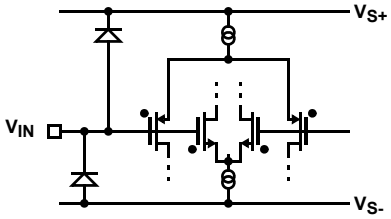


Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	VOUT	Amplifier output	(Reference “CIRCUIT 1”)
2	VS-	Negative power supply	
3	VIN+	Amplifier non-inverting input	(Reference “CIRCUIT 2”)
4	VIN-	Amplifier inverting input	(Reference “CIRCUIT 2”)
5	VS+	Positive power supply	



CIRCUIT 1



CIRCUIT 2

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
EL5120TIWTZ-T7 (Note 1)	BESA	5 Ld TSOT	MDP0049

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for EL5120T. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . . . +19.8V
Input Voltage Range (V_{IN+}, V_{IN-}) . . . . . V_S- - 0.5V, V_S+ + 0.5V
Input Differential Voltage (V_{IN+} - V_{IN-}) . . . . . (V_S+ + 0.5V)-(V_S- - 0.5V)
Maximum Continuous Output Current . . . . . ±70mA
ESD Rating
Human Body Model (Tested per JESD22-A114) 4000V
Machine Model (Tested per JESD22-A115) 300V
Charged Device Model (Tested per JESD22-C101) 2000V
Latch Up (Tested per JESD78; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld TSOT (Notes 4, 5)	215	290

Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +125°C
Maximum Junction Temperature . . . . . +150°C
Power Dissipation . . . . . See Figures 30 and 31

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 10kΩ to 0V, T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		5	18	mV
TCV_{OS}	Average Offset Voltage Drift (Note 6)			5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -5.5V to +5.5V	50	75		dB
A_{VOL}	Open Loop Gain	-4.5V ≤ V_{OUT} ≤ +4.5V	75	105		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.94	-4.85	V
V_{OH}	Output Swing High	I_L = +5mA	4.85	4.94		V
I_{SC}	Short Circuit Current	V_{CM} = 0V, Source: V_{OUT} short to V_S-, Sink: V_{OUT} short to V_S+		±200		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
(V_S+) - (V_S-)	Supply Voltage Range		4.5		19	V
I_S	Supply Current	V_{CM} = 0V, No load		750	950	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from ±2.25V to ±9.5V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 7)	-4.0V ≤ V_{OUT} ≤ +4.0V, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (Note 8)	A_V = +1, V_{OUT} = 2V step, R_L = 10kΩ, C_L = 8pF		500		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 8pF		12		MHz

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $R_L = 10k\Omega$ to 0V, $T_A = +25°C$, unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
GBWP	Gain-Bandwidth Product	$A_V = -50$, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, $C_L = 8pF$		8		MHz
PM	Phase Margin	$A_V = -50$, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, $C_L = 8pF$		50		°

Electrical Specifications $V_S+ = +5V$, $V_S- = 0V$, $R_L = 10k\Omega$ to 2.5V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		5	18	mV
TCV_{OS}	Average Offset Voltage Drift (Note 6)			5		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -0.5V to +5.5V	45	70		dB
A_{VOL}	Open Loop Gain	$0.5V \leq V_{OUx} \leq +4.5V$	75	105		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -2.5mA$		30	150	mV
V_{OH}	Output Swing High	$I_L = +2.5mA$	4.85	4.97		V
I_{SC}	Short Circuit Current	$V_{CM} = 2.5V$, Source: V_{OUT} short to V_S-, Sink: V_{OUT} short to V_S+		±125		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
$(V_S+) - (V_S-)$	Supply Voltage Range		4.5		19	V
I_S	Supply Current	$V_{CM} = 2.5V$, No load		750	950	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 7)	$1V \leq V_{OUT} \leq 4V$, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (Note 8)	$A_V = +1$, $V_{OUT} = 2V$ step, $R_L = 10k\Omega$, $C_L = 8pF$		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 8pF$		12		MHz
GBWP	Gain-Bandwidth Product	$A_V = -50$, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, $C_L = 8pF$		8		MHz
PM	Phase Margin	$A_V = -50$, $R_F = 5k\Omega$, $R_G = 100\Omega$ $R_L = 10k\Omega$, $C_L = 8pF$		50		°

Electrical Specifications

$V_S+ = +18V$, $V_S- = 0V$, $R_L = 10k\Omega$ to 9V, $T_A = +25°C$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 9V		6	18	mV
TCV_{OS}	Average Offset Voltage Drift (Note 6)			6		µV/°C
I_B	Input Bias Current	V_{CM} = 9V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+18.5	V
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -0.5V to +18.5V	53	78		dB
A_{VOL}	Open Loop Gain	$0.5V \le V_{OUT} \le 17.5V$	75	90		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -9mA		120	150	mV
V_{OH}	Output Swing High	I_L = +9mA	17.85	17.88		V
I_{SC}	Short Circuit Current	V_{CM} = 9V, Source: V_{OUT} short to V_S-, Sink: V_{OUT} short to V_S+		±200		mA
I_{OUT}	Output Current			±70		mA
POWER SUPPLY PERFORMANCE						
$(V_S+) - (V_S-)$	Supply Voltage Range		4.5		19	V
I_S	Supply Current	V_{CM} = 9V, No load		900	1100	µA
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 7)	$1V \le V_{OUT} \le 17V$, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (Note 8)	A_V = +1, V_{OUT} = 2V step, $R_L = 10k\Omega$, C_L = 8pF		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, C_L = 8pF		12		MHz
GBWP	Gain-Bandwidth Product	A_V = -50, $R_F = 5k\Omega$, $R_G = 100\Omega$, $R_L = 10k\Omega$, C_L = 8pF		8		MHz
PM	Phase Margin	A_V = -50, $R_F = 5k\Omega$, $R_G = 100\Omega$, $R_L = 10k\Omega$, C_L = 8pF		50		°

NOTES:

6. Measured over -40°C to +85°C ambient operating temperature range. See the typical TCV_{OS} production distribution shown in the "Typical Performance Curves" on page 6.
7. Typical slew rate is an average of the slew rates measured on the rising (20% to 80%) and the falling (80% to 20%) edges of the output signal.
8. Settling time measured as the time from when the output level crosses the final value on rising/falling edge to when the output level settles within a ±0.1% error band. The range of the error band is determined by: Final Value(V)±[Full Scale(V)*0.1%]
9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

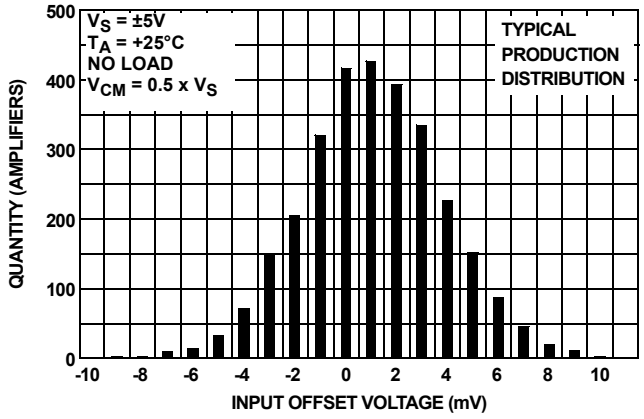


FIGURE 3. INPUT OFFSET VOLTAGE DISTRIBUTION

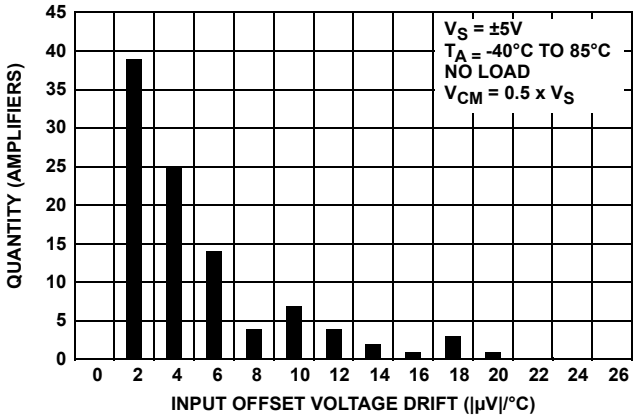


FIGURE 4. INPUT OFFSET VOLTAGE DRIFT (TSOT)

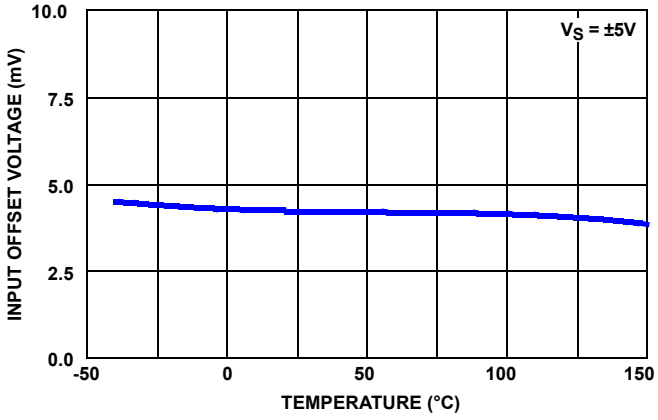


FIGURE 5. INPUT OFFSET VOLTAGE vs TEMPERATURE

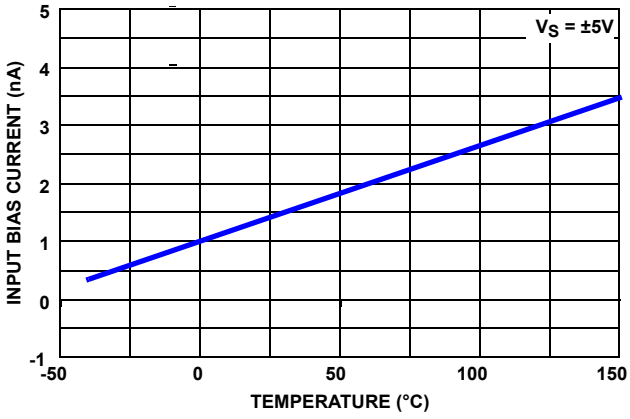


FIGURE 6. INPUT BIAS CURRENT vs TEMPERATURE

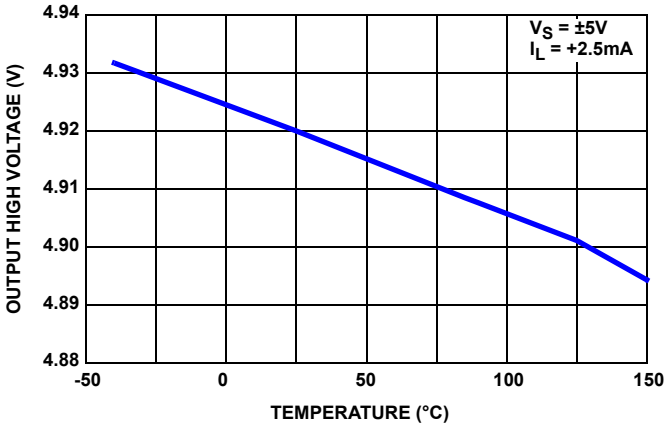


FIGURE 7. OUTPUT HIGH VOLTAGE vs TEMPERATURE

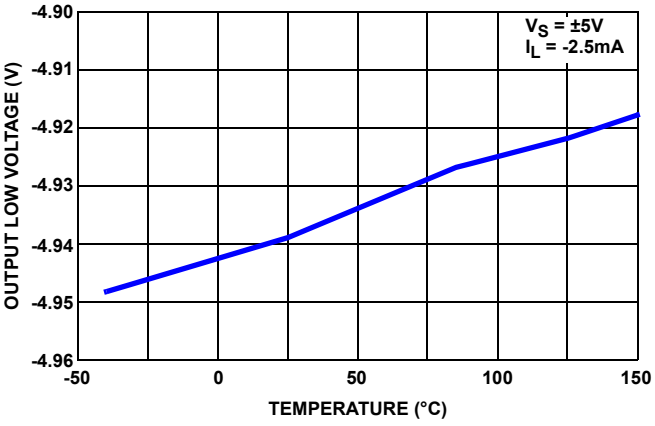


FIGURE 8. OUTPUT LOW VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

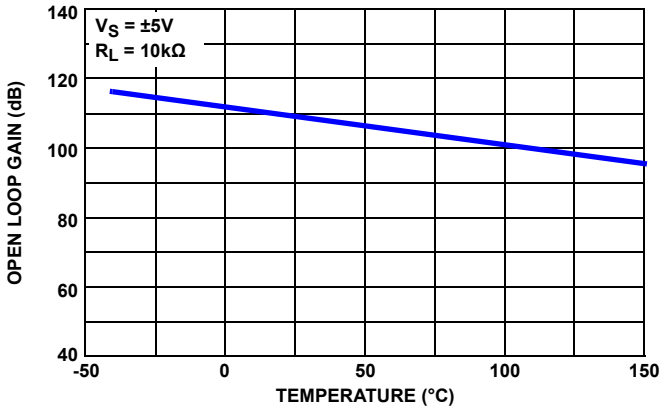


FIGURE 9. OPEN-LOOP GAIN vs TEMPERATURE

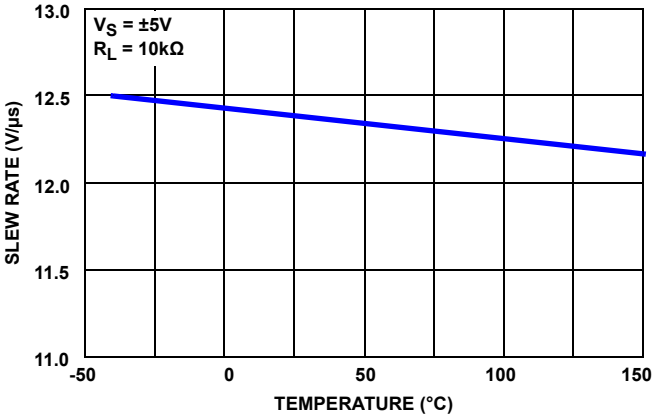


FIGURE 10. SLEW RATE vs TEMPERATURE

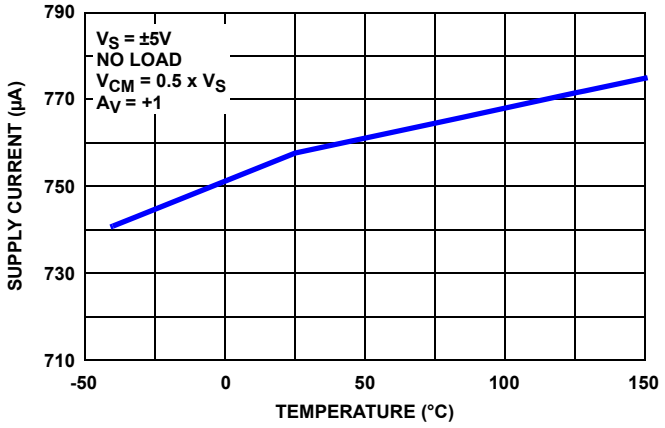


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

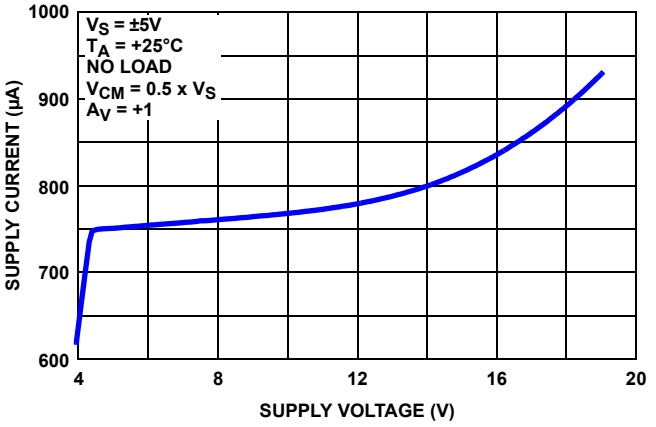


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

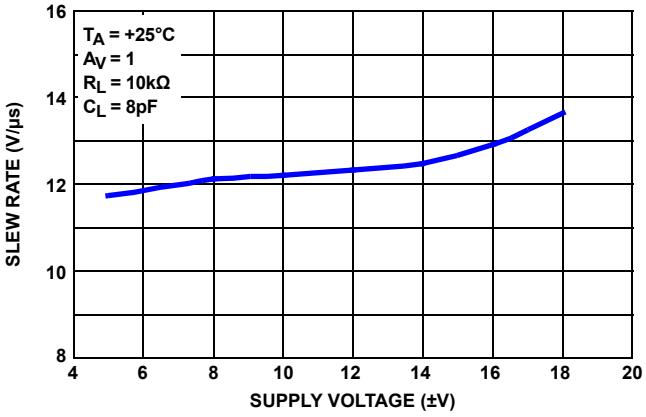


FIGURE 13. SLEW RATE vs SUPPLY VOLTAGE

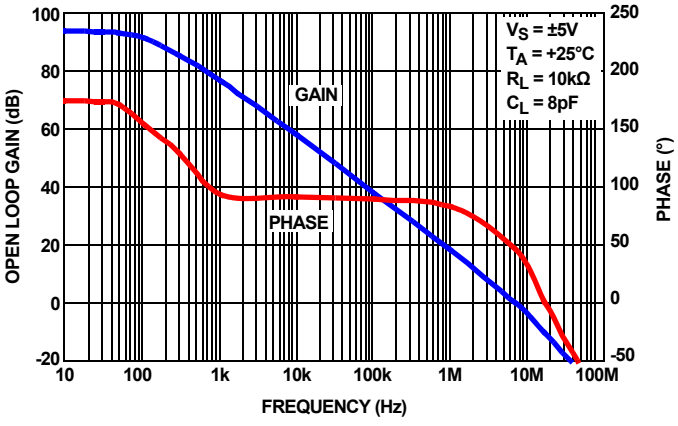


FIGURE 14. OPEN LOOP GAIN AND PHASE vs FREQUENCY

Typical Performance Curves (Continued)

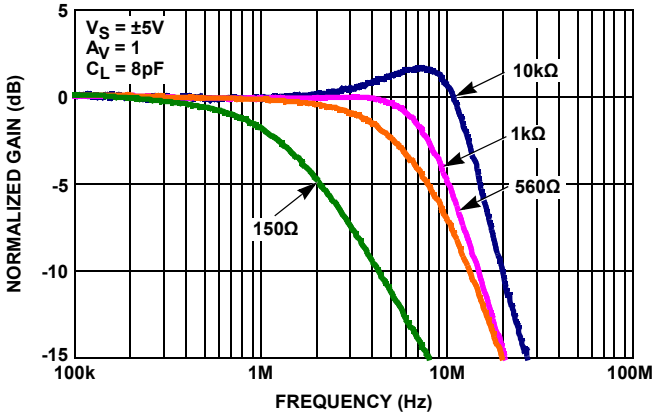


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS R_L

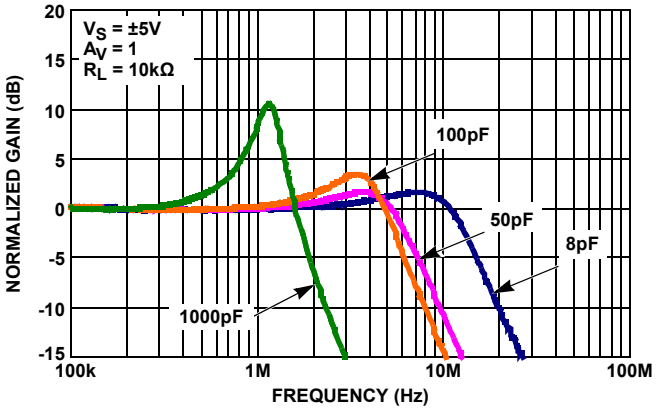


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS C_L

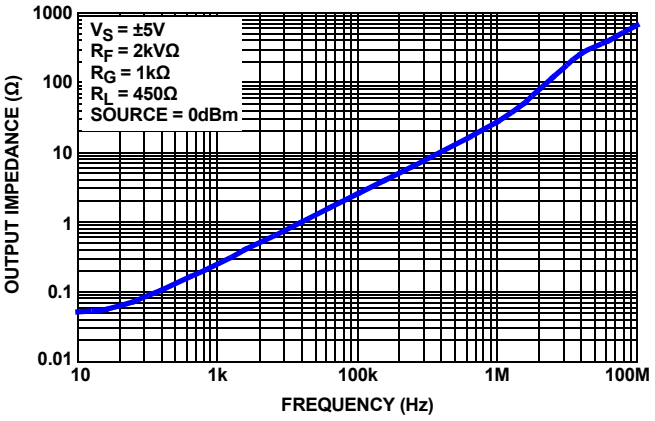


FIGURE 17. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

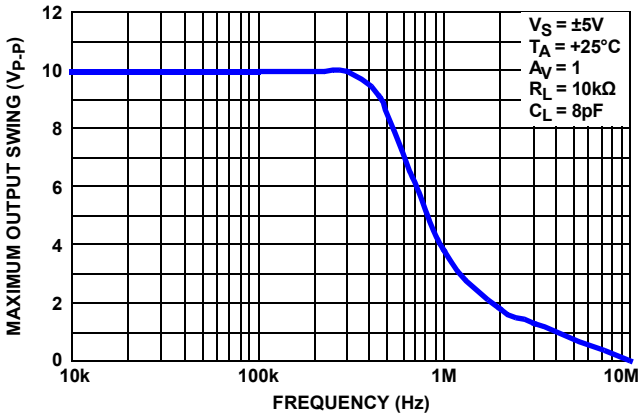


FIGURE 18. MAXIMUM OUTPUT SWING vs FREQUENCY

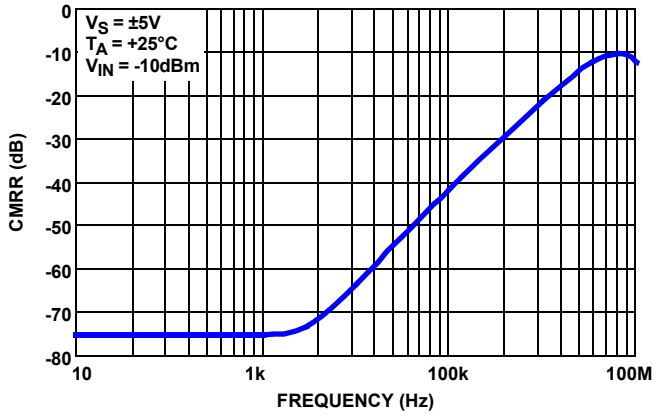


FIGURE 19. CMRR vs FREQUENCY

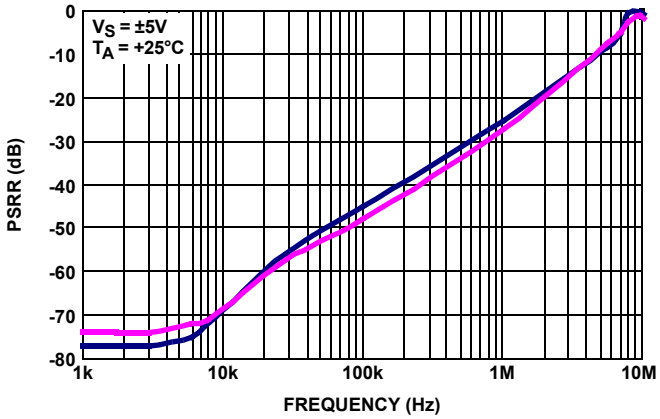


FIGURE 20. PSRR vs FREQUENCY

Typical Performance Curves (Continued)

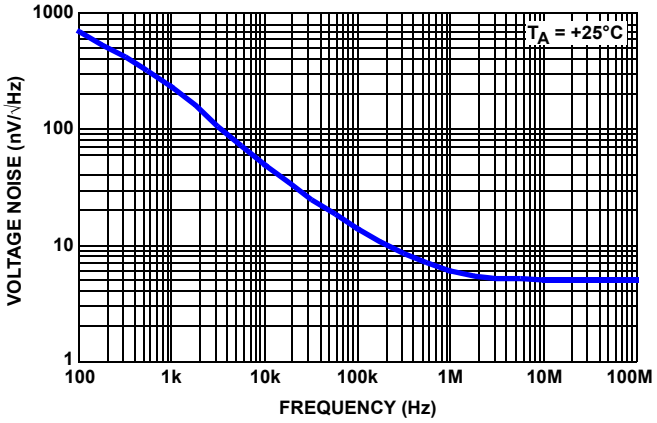


FIGURE 21. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

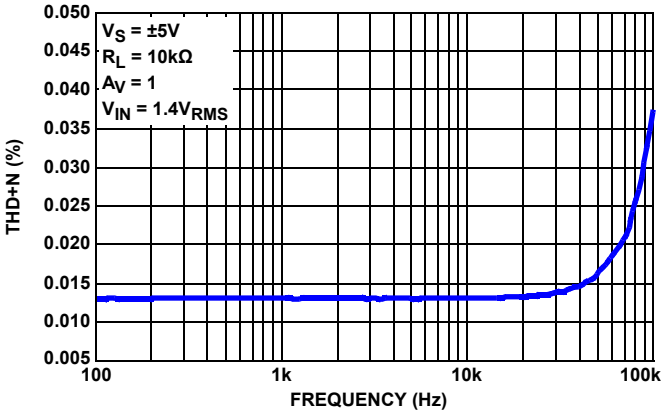


FIGURE 22. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

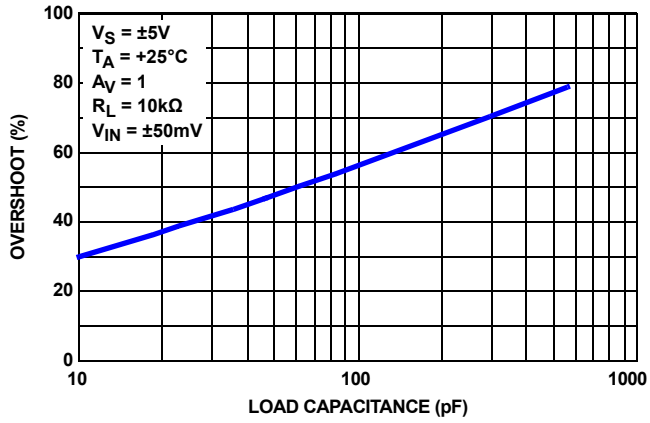


FIGURE 23. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE

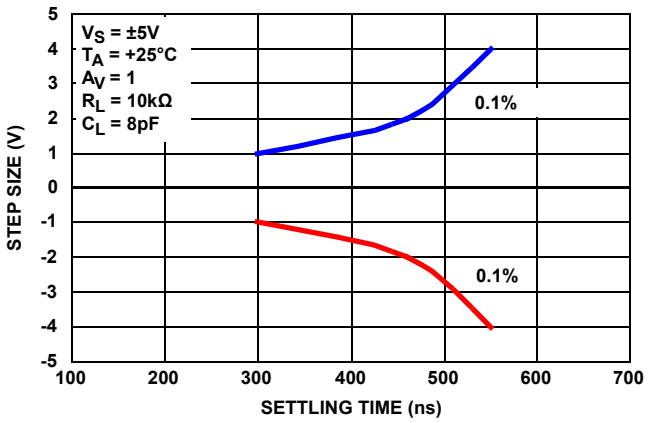


FIGURE 24. STEP SIZE vs SETTLING TIME

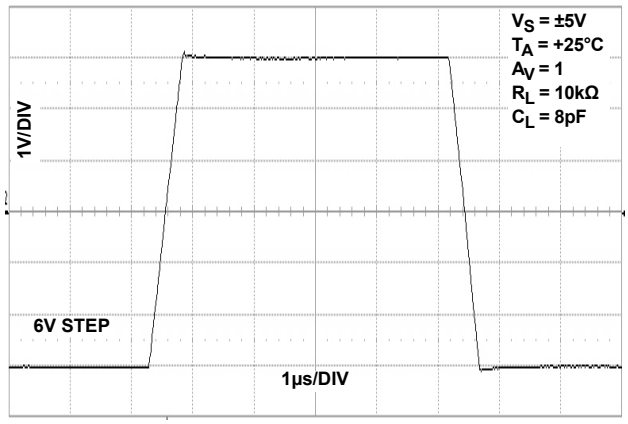


FIGURE 25. LARGE SIGNAL TRANSIENT RESPONSE

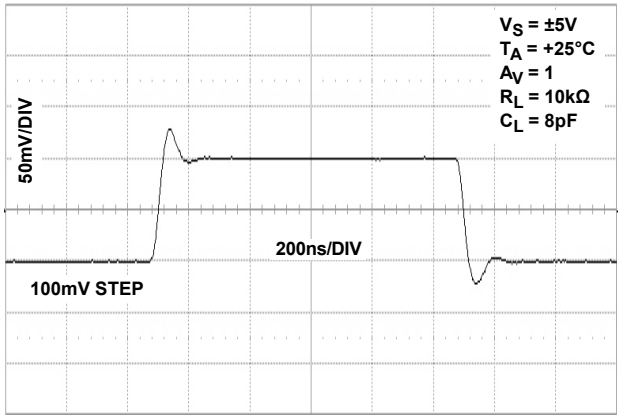


FIGURE 26. SMALL SIGNAL TRANSIENT RESPONSE

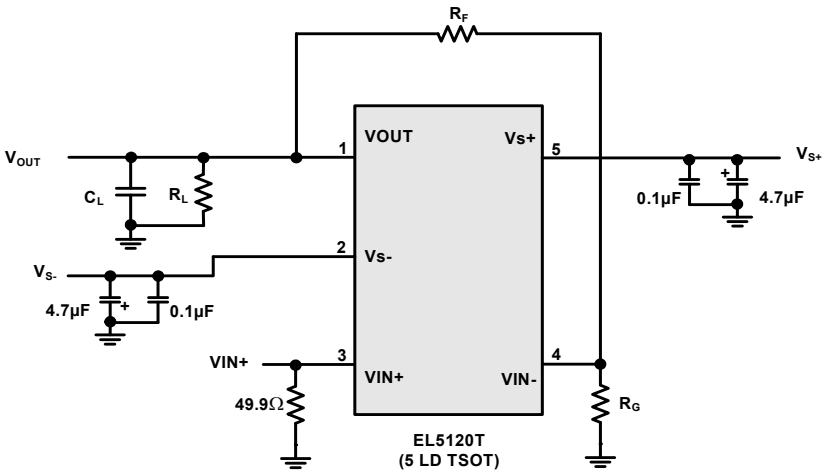


FIGURE 27. BASIC TEST CIRCUIT

Applications Information

Product Description

The EL5120T is a high voltage rail-to-rail input-output amplifier with low power consumption. The EL5120T is a single amplifier which exhibits beyond the rail input capability, rail-to-rail output capability, and is unity gain stable.

The EL5120T features a slew rate of 12V/µs. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 12MHz (-3dB). This enables the amplifier to offer maximum dynamic range at any supply voltage.

Operating Voltage, Input and Output Capability

The EL5120T can operate on a single supply or dual supply configuration. The EL5120T operating voltage ranges from a minimum of 4.5V to a maximum of 19V. This range allows for a standard 5V (or ±2.5V) supply voltage to dip to -10%, or a standard 18V (or ±9V) to rise by +5.5% without affecting performance or reliability.

The input common-mode voltage range of the EL5120T extends 500mV beyond the supply rails. Also, the EL5120T is immune to phase reversal. However, if the common mode input voltage exceeds the supply voltage by more than 0.5V, electrostatic protection diodes in the input stage of the device begin to conduct. Even though phase reversal will not occur, to maintain optimal reliability it is suggested to avoid input overvoltage conditions. Figure 28 shows the input voltage driven 500mV beyond the supply rails and the device output swinging between the supply rails.

The EL5120T output typically swings to within 50mV of positive and negative supply rails with load currents of ±5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 29 shows the input and output waveforms for the device in a unity-gain configuration. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid and the output voltage is approximately $9.9V_{P-P}$.

Refer to the “Electrical Specifications” table beginning on page 3 for specific device parameters. Parameter variations with operating voltage, loading and/or temperature are shown in the “Typical Performance Curves” beginning on page 6.

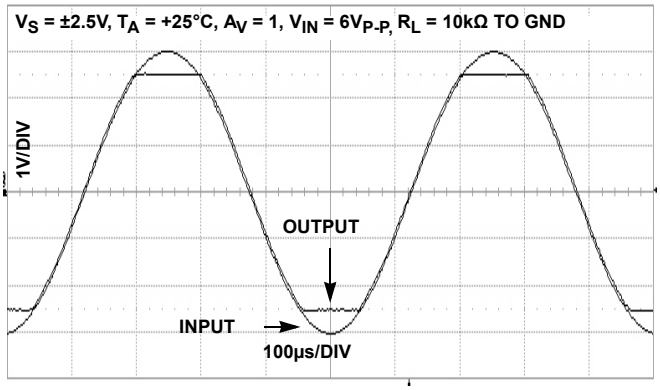


FIGURE 28. OPERATION WITH BEYOND-THE-RAILS INPUT

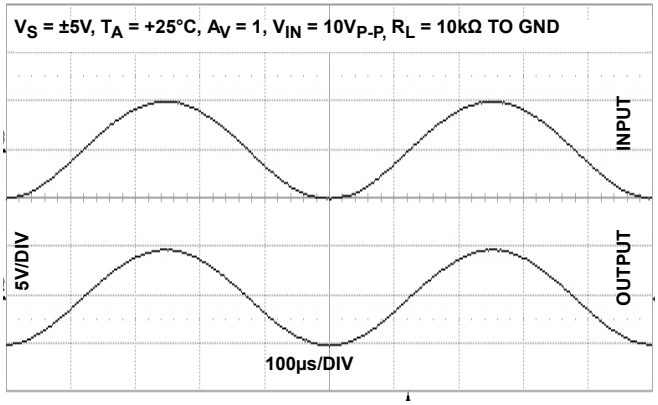


FIGURE 29. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Output Current

The EL5120T is capable of output short circuit currents of 200mA (source and sink), and the device has built-in protection circuitry, which limits the output current to ±200mA (typical).

To maintain maximum reliability, the continuous output current should never exceed ±70mA. This ±70mA limit is determined by the characteristics of the internal metal interconnects. Also, see “Power Dissipation” on page 12 for detailed information on ensuring proper device operation and reliability for temperature and load conditions.

Thermal Shutdown

The EL5120T has a built-in thermal protection, which ensures safe operation and prevents internal damage to the device due to overheating. When the die temperature reaches +165°C (typical), the device automatically shuts OFF the outputs by putting them in a high impedance state. When the die cools by +15°C (typical), the device automatically turns ON the outputs by putting them in a low impedance (normal) operating state.

Driving Capacitive Loads

Purely capacitive loads on the EL5120T should not exceed 1nF without appropriate output load isolation or amplifier compensation techniques.

As load capacitance increases, the -3dB bandwidth will decrease and peaking can occur. Depending on the application, it may be necessary to reduce peaking and to improve device stability. To improve device stability, a snubber circuit (compensation) or a series resistor (isolation) may be added to the output of the EL5120T.

A snubber is a shunt load consisting of a resistor in series with a capacitor. An optimized snubber can improve the phase margin and the stability of the EL5120T. The advantage of a snubber circuit is that it does not draw any DC load current or reduce the gain.

Another method to reduce peaking is to add a series output resistor (typically between 1Ω to 10Ω). Depending on the capacitive loading, a small value resistor may be the most appropriate choice to minimize any reduction in gain.

Power Dissipation

With the high-output drive capability of the EL5120T amplifier, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. It is important to calculate the maximum power dissipation of the EL5120T in the application. Proper load conditions will ensure that the EL5120T junction temperature stays within a safe operating region.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- Θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation allowed

The total power dissipation produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power dissipation in the IC due to the load, or:

$$P_{DMAX} = V_S \times I_{SMAX} + (V_S+ - V_{OUT}) \times I_{LOAD} \quad \text{(EQ. 2)}$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_{SMAX} + (V_{OUT} - V_S-) \times I_{LOAD} \quad \text{(EQ. 3)}$$

when sinking,

where:

- V_S = Total supply voltage ($V_S+ - V_S-$)
- V_S+ = Positive supply voltage
- V_S- = Negative supply voltage
- I_{SMAX} = Maximum supply current (I_{SMAX} = EL5120T quiescent current)
- V_{OUT} = Output voltage
- I_{LOAD} = Load current

Device overheating can be avoided by calculating the minimum resistive load condition, R_{LOAD}, resulting in the highest power dissipation. To find R_{LOAD} set the two P_{DMAX} equations equal to each other and solve for V_{OUT}/I_{LOAD}. Reference the package power dissipation curves, Figures 30 and 31, for further information.

JEDEC JESD51-3 LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD

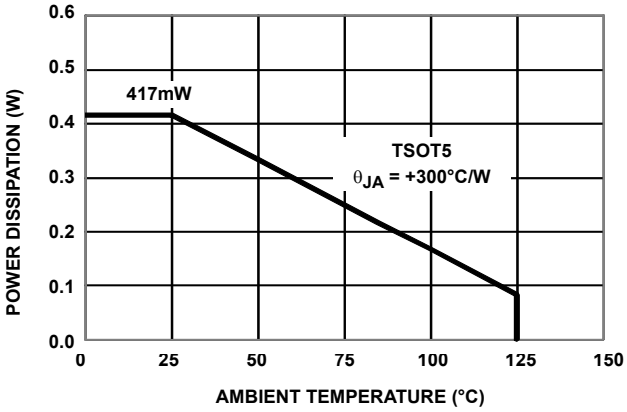


FIGURE 30. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

JEDEC JESD51-7 HIGH EFFECTIVE THERMAL CONDUCTIVITY (4-LAYER) TEST BOARD - EXPOSED DIEPAD SOLDERED TO PCB PER JESD51-5

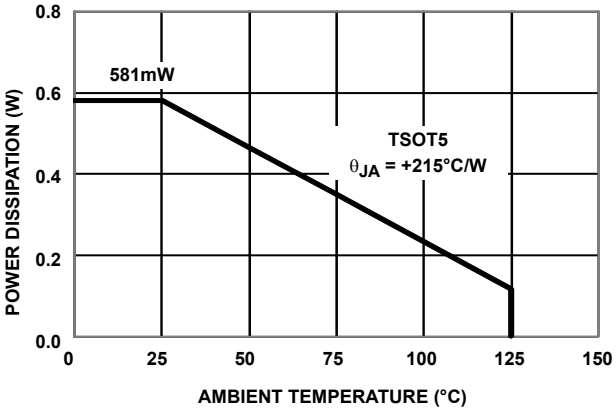


FIGURE 31. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Power Supply Bypassing and Printed Circuit Board Layout

The EL5120T can provide gain at high frequency, so good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, trace lengths should be as short as possible and the power supply pins must be well bypassed to reduce any risk of oscillation.

For normal single supply operation (the V_S- pin is connected to ground) a 4.7µF capacitor should be placed from V_S+ to ground, then a parallel 0.1µF capacitor should be connected as close to the amplifier as possible. One 4.7µF capacitor may be used for multiple devices. For dual supply operation the same capacitor combination should be placed at each supply pin to ground.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

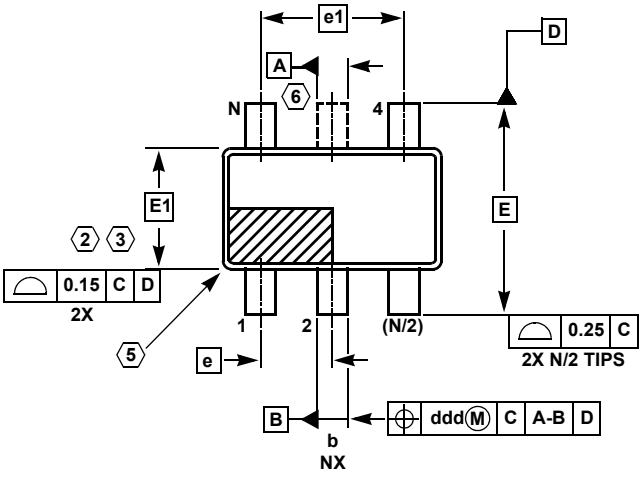
DATE	REVISION	CHANGE
September 26, 2013	FN6895.1	Features on page 1: Updated operation temperature range from " -40°C to +85°C" to "-40°C to +125°C". Thermal Information table on page 3 under Ambient operation temperature changed the temperature range from "-40°C to +85°C" to "-40°C to +125°C". Updated Figure 30, "PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE," on page 12 and Figure 31, "PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE," on page 12.
September 27, 2012	FN6895.0	Initial release.

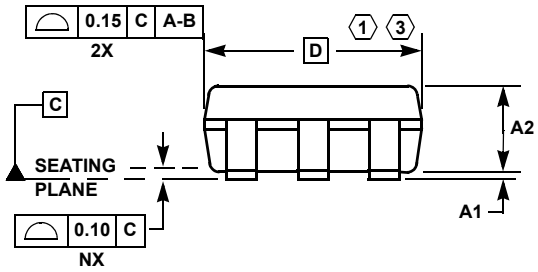
About Intersil

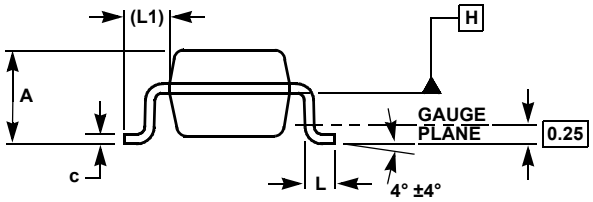
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

TSOT Package Family







MDP0049

TSOT PACKAGE FAMILY

SYMBOL	MILLIMETERS			TOLERANCE
	TSOT5	TSOT6	TSOT8	
A	1.00	1.00	1.00	Max
A1	0.05	0.05	0.05	±0.05
A2	0.87	0.87	0.87	±0.03
b	0.38	0.38	0.29	±0.07
c	0.127	0.127	0.127	+0.07/-0.007
D	2.90	2.90	2.90	Basic
E	2.80	2.80	2.80	Basic
E1	1.60	1.60	1.60	Basic
e	0.95	0.95	0.65	Basic
e1	1.90	1.90	1.95	Basic
L	0.40	0.40	0.40	±0.10
L1	0.60	0.60	0.60	Reference
ddd	0.20	0.20	0.13	-
N	5	6	8	Reference

Rev. B 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.15mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (TSOT6 AND TSOT8 only).
6. TSOT5 version has no center lead (shown as a dashed line).