19-3469; Rev 2; 4/08

EVALUATION KIT AVAILABLE

Single-Chip Global Positioning System Receiver Front-End

MAX2742

General Description

The MAX2742 complete single-chip global positioning system (GPS) RF front-end utilizes many innovative and leading-edge RF CMOS design techniques. This high-performance, state-of-the-art device consumes extremely low power and eliminates the need for costly SAW and bulky discrete IF filters. The MAX2742 incorporates a fully integrated low-noise amplifier (LNA) and mixer, IF section, digital sampler, and local oscillator synthesizer.

The intended input signal for the MAX2742 is the L1 GPS signal 1.57542GHz. This device supports high-accuracy output quantization, which delivers the best performance obtainable for the GPS receiver. The power consumption of the MAX2742 is as low as 32mW at a +2.4V supply.

The MAX2742 is available in a space-saving 48-pin TQFP package and is specified for the extended (-40°C to +85°C) temperature range.

Applications

In-Vehicle Navigation Systems (IVNS)

Location-Based Services (PDAs and Accessories)

Recreational Handheld/Walkie Talkies

Geographical Information Systems (GISs)

Telematics (Vehicle, Asset Tracking, and Inventory Management)

Emergency Roadside Assistance

Emergency Response Systems

Digital Cameras/Camcorders

Consumer Electronics

Features

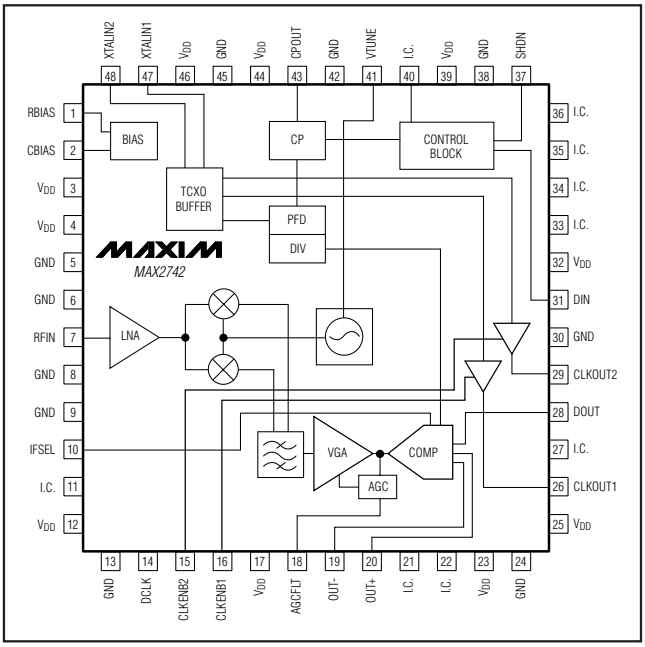
- ♦ **Complete Single-Chip GPS Front-End Receiver**
- ♦ **Single-Ended or Differential Outputs at 1.023MHz**
- ♦ **Low 4.5dB Typical Noise Figure**
- ♦ **No External IF SAW or Discrete Filters Required**
- ♦ **Very Low 32mW Power Consumption at +2.4V**
- ♦ **Wide +2.4V to +3.6V Operational Supply Voltage Range**
- ♦ **Extended -40°C to +85°C Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2742ECM	-40°C to +85°C	48 TQFP-EP*
MAX2742ECM+	-40°C to +85°C	48 TQFP-EP*

*EP = Exposed paddle.
+Denotes lead-free package.

Block Diagram/ Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +3.7V
All Other Pins to GND.....-0.3V to (V_{DD} + 0.3V)
RF LNA Input Power .....+10dBm
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP-EP (derate 12.5mW/°C above +70°C) 100mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (10s).....+300°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2742 EV kit, V_{DD} = +2.4V to +3.6V, V_{SHDN} = V_{DD}, T_A = -40°C to +85°C. Typical values are at V_{DD} = +3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.4		3.6	V
Supply Current	V_{DD} = +3.0V, T_A = +25°C (Note 1)		14	20	mA
	Shutdown mode, V_{SHDN} = 0V		10		µA
Logic-Input High Voltage		V_{DD} - 0.5			V
Logic-Input Low Voltage				0.5	V
Logic-Input Bias Current		-40		+40	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2742 EV kit, V_{DD} = +2.4V to +3.6V, V_{SHDN} = V_{DD}, T_A = -40°C to +85°C. Typical values are at V_{DD} = +3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL PERFORMANCE					
Maximum Conversion Gain	(Notes 2, 3)	91	102	117	dB
Input Frequency			1575.42		MHz
Noise Figure	Measured at quantizer input		4.5		dB
Return Loss (S11)			-15		dB
LNA/Mixer Input IP3	f_1 = 1.5MHz and f_2 = 2.0MHz above carrier frequency		-32		dBm
Output IF Frequency			1.023		MHz
OUTPUT STAGE					
Output Rise/Fall Time	Differential (VOUT+, VOUT-), C_L < 20pF		25		ns
	Single ended (DOUT), C_L < 20pF		5		
Output-Voltage-Level Low	Differential		V_{DD} - 0.9		V
	Single ended		0		
Output-Voltage-Level High	Differential		V_{DD}		V
	Single ended				

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2742 EV kit, V_{DD} = +2.4V to +3.6V, V_{SHDN} = V_{DD}, T_A = -40°C to +85°C. Typical values are at V_{DD} = +3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SYNTHESIZER					
TCXO Input Frequency	Fundamental frequency crystal		18.414		MHz
Charge-Pump Current			0.4		mA
Phase Noise	f_{OFFSET} = 10kHz offset, BW_{LOOP} = 70kHz		-71		dBc/Hz
	f_{OFFSET} = 1MHz offset, BW_{LOOP} = 70kHz		-106		
Comparison Frequency Spur	BW_{LOOP} = 70kHz		-66		dBc
VCO Turning Range	(Notes 2, 3)	148	210	277	MHz
VCO Tuning Gain	(Notes 2, 3)	139	200	305	MHz/V
IF STAGE					
IF Stage Gain	VGA set at maximum gain		77		dB
Dynamic Range IF Stage Gain			50		dB
Bandpass Filter 1dB Corner Frequency	Low-frequency corner		0.1		MHz
	High-frequency corner		3.2		
Bandpass Filter 60dB High-Side Rejection			5.0		MHz
Image Rejection			18		dB
In-Band Ripple			1		dB
AGC Loop Lock Time			1		ms

Note 1: At T_A = +25°C, min/max limits are guaranteed by production test.
Note 2: At T_A = -40°C, min/max limits are guaranteed by design and characterization.
Note 3: At T_A = +25°C and +85°C, min/max limits are guaranteed by production test.

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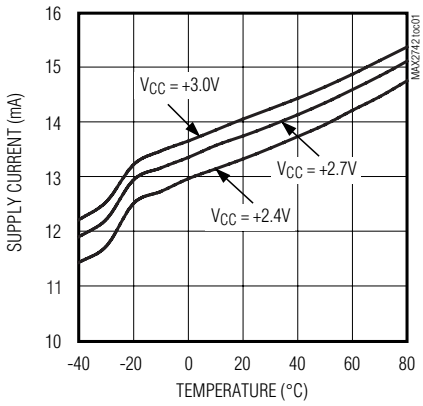
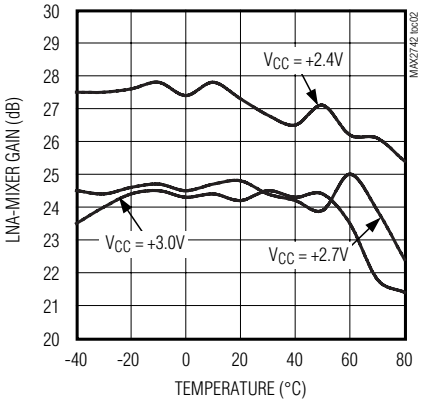
Typical Operating Characteristics

(MAX2742 EV kit, V_{DD} = +3V, and T_A = +25°C, unless otherwise noted.)

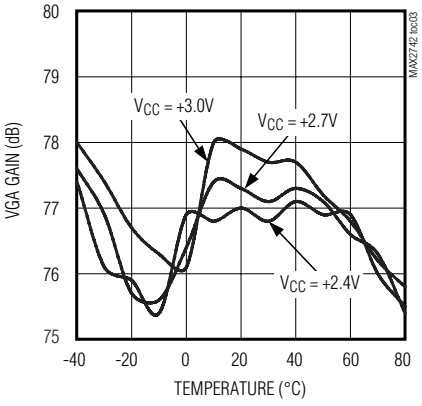
SUPPLY CURRENT vs. TEMPERATURE



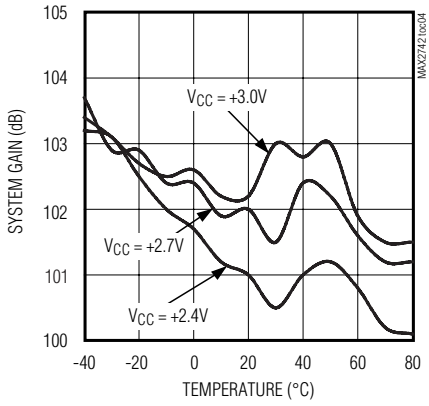
LNA/MIXER GAIN vs. TEMPERATURE



MAXIMUM IF STAGE GAIN vs. TEMPERATURE



TOTAL CONVERSION GAIN vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	RBIAS	External Bias Resistor. Connect a 100kΩ ±1% resistor in parallel with a 0.1µF capacitor in series with a 71kΩ resistor to GND.
2	CBIAS	External Bias Capacitor. Connect a 0.1µF capacitor to GND.
3, 4, 12, 17, 23, 25, 32, 39, 44, 46	V_{DD}	Supply Voltage. Bypass to GND with 100pF and 100nF capacitors as close to the pin as possible with the smaller value capacitor closer to the pin.
5, 6, 8, 9, 13, 24, 30, 38, 42, 45	GND	Ground. Connect to PC board ground plane.
7	RFIN	LNA Input. Requires external matching network.
10	IFSEL	IF Output Select. Selects output type. Drive high for single-ended output, drive low for differential output.
11, 21, 22, 27, 33–36, 40	I.C.	Internally Connected. Leave unconnected.
14	DCLK	Digital Control Clock
15	CLKENB2	Clock Output Enable 2. Drive high to enable limited-swing clock output.
16	CLKENB1	Clock Output Enable 1. Drive high to enable full-swing clock output.
18	AGCFLT	AGC External Filter
19, 20	OUT-, OUT+	Differential Comparator Outputs
26	CLKOUT1	Full-Swing Clock Output
28	DOUT	Digital Output
29	CLKOUT2	Limited-Swing Clock Output
31	DIN	Digital-Control Data Input
37	SHDN	Shutdown. Drive SHDN low to disable all device functions. Drive SHDN high for normal operation.
41	VTUNE	VCO Tuning Input. Connect directly to the loop filter output.
43	CPOUT	Charge-Pump Output. Connect directly to the loop filter input.
47, 48	XTALIN1, XTALIN2	Crystal Oscillator Input. Connect XTALIN1 and XTALIN2 together and to the TCXO output through a coupling capacitor.
—	EP	Exposed Paddle. Internally connected to GND. Connect to PC board ground plane for optimal performance.

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Detailed Description

LNA/Mixer

The RF input from the GPS antenna is fed through an LNA with a 24dB gain. The amplified signal is then fed to a mixer that downconverts the signal (1575.42MHz) to a quadrature differential IF of 1.023MHz.

IF Stage

The quadrature IF signals pass through the IF filter, which rejects the out-of-band spurs by more than 60dB and the image noise by 18dB (typ). After the image reject filter, the signal is converted from quadrature to differential. The filtered IF signal is then amplified by the AGC block, which sets the VGA output signal level to a predetermined value through the application using 50dB of dynamic range. The internal offset-cancellation mechanism generates a highpass characteristic for the IF section with a 1dB corner frequency of about 100kHz.

IF Output Selection

The sampled outputs of the GPS signal are available in a single-ended or differential format. The IFSEL pin controls the output format.

Synthesizer

An on-chip VCO provides quadrature differential LO signals to the downconverting mixer and controls the frequency. An on-board TCXO generates the reference frequency. The integrated synthesizer includes the VCO, TCXO buffer, main frequency divider, phase-frequency detector, and charge pump. It uses an off-chip PLL loop filter and TCXO. Connect the output of the TCXO to XTALIN1 and XTALIN2 through a coupling capacitor.

The main division ratio for the synthesizer is 684. With this division ratio, a low-side injection LO can be synthesized with an 18.414MHz TXCO.

Applications Information

Layout Issues

A properly designed PC board is an essential part of any RF/microwave circuit. On all high-frequency inputs and outputs, use controlled impedance lines and keep them as short as possible to minimize losses and radiation. Keeping the traces short also reduces parasitic inductance. To further reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Also, place decoupling capacitors as close to the supply pins as possible. For proper power dissipation and operation, connect the metal exposed paddle solidly to the ground plane of the PC board.

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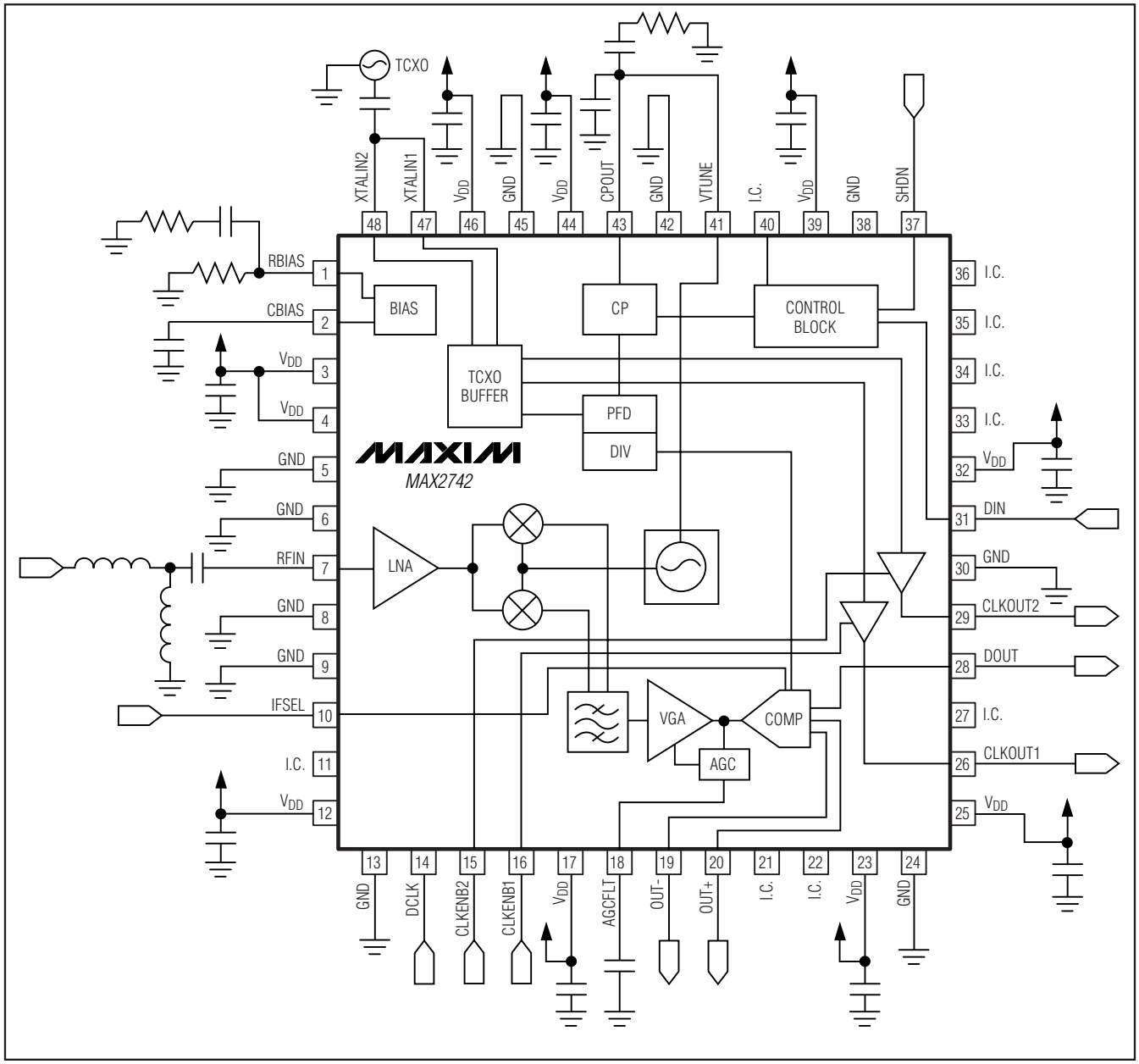
Typical Application Circuit



Chip Information

PROCESS: CMOS

TRANSISTOR COUNT: 18443

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFP-EP	C48E-8	21-0065

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	4/08	Changed *Electrical Characteristics* to include a minimum limit for a maximum conversion gain, corrected *Pin Description*	2, 3, 5, 6