TSH321

WIDE BANDWIDTH AND MOS INPUT SINGLE OPERATIONAL AMPLIFIER

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 300MHz
- GAIN OF 2 STABILITY
- SLEW RATE : 400V/µs
- VERY FAST SETTLING TIME : 60ns (0.1%)
- VERY HIGH INPUT IMPEDANCE

DESCRIPTION

The TSH321 is a wideband monolithic operational amplifier, requiring a minimum close loop gain of 2 for stability.

The TSH321 features extremely high input impedance (typically greater than $10^{12}\Omega$) allowing direct interfacing with high impedance sources.

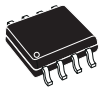
Low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The TSH321 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD883C-Class2.

ORDER CODE

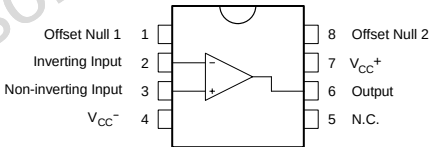
Part Number	Temperature Range	Package
		D
TSH321I	-40°C, +125°C	•

D = Small Outline Package (SO) - also available in Tape & Reel (DT)

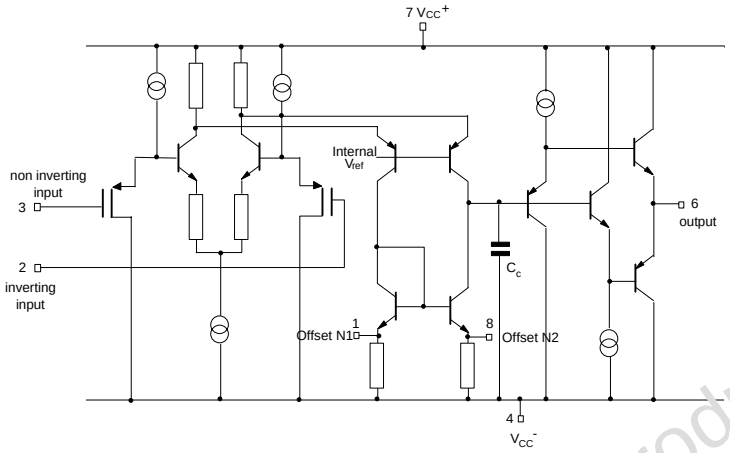


D
SO8
(Plastic Micropackage)

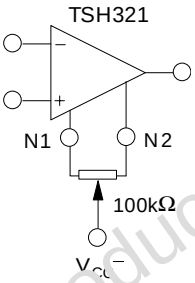
PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±7	V
V_{id}	Differential Input Voltage	±5	V
V_i	Input Voltage	±5	V
I_{in}	Current On Offset Null Pins	±20	V
T_{oper}	Operating Free-Air Temperature range	-40 to +125	°C

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±3 to ±6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC}^- to V_{CC}^+ -3	V

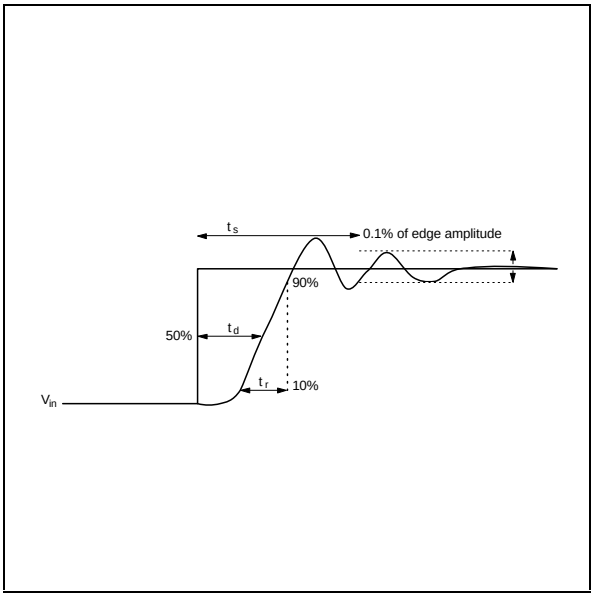
ELECTRICAL CHARACTERISTICS

V_{CC} = ±5V, T_{amb} = 25°C (unless otherwise specified)

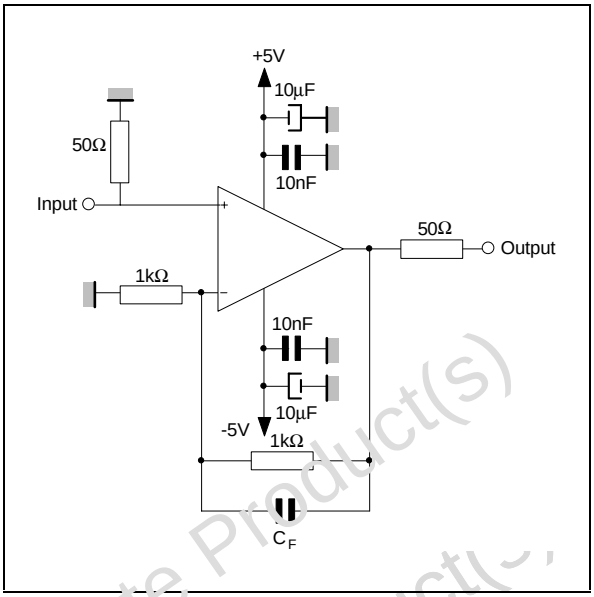
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $T_{min.} \le T_{amb} \le T_{max}$		0.5	10 12	mV
DV_{io}	Input Offset Voltage Drift $T_{min.} \le T_{amb} \le T_{max.}$		10		µV/°C
I_{ib}	Input Bias Current.		2	300	pA
I_{io}	Input Offset Current.		2	200	pA
I_{CC}	Supply Current, no load V_{CC} = ±5V V_{CC} = ±3V V_{CC} = ±6V $T_{min.} \le T_{amb} \le T_{max}$ V_{CC} = ±5V		23 21 25	30 28 40 3[illegible]	mA
Avd	Large Signal Voltage Gain Vo = ±2.5V $R_L = \infty$ R_L = 100Ω R_L = 50Ω	800 300 200	1300 850 650		V/V
V_{icm}	Input Common Mode Voltage Range	-5 to +2	5.5 to +2.5		V
CMR	Common-mode Rejection Ratio $V_{ic} = V_{icm\ min.}$	60	100		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = ±5V to ±3V	50	70		dB
V_o	Output Voltage R_L = 100Ω R_L = 50Ω R_L = 100Ω $T_{min.} \le T_{amb} \le T_{max}$ R_L = 50Ω	±3 ±2.8 ±2.9 ±2.7	+3.5 -3.7 +3.3 -3.5		V
I_o	Output Short Circuit Current Vid = ±1V, Vo = 0V	±50	±100		mA
GBP	Gain Bandwidth Product A_{VCL} = 100, R_L = 100Ω, C_L = 15pF, f = 7.5MHz		300		MHz
SR	Slew Rate V_{in} = ±1V, A_{VCL} = 2, R_L = 100Ω, C_L = 15pF	200	400		V/µs
e_n	Equivalent Input Voltage Noise R_s = 50Ω f_o = 1kHz f_o = 1k0Hz f_o = 100kHz f_o = 1MHz		20 18.2 18.1 18.2		nV/√Hz
K_{ov}	Overshoot V_{in} = ±1V, A_{VCL} = 2, R_L = 100Ω, C_L = 15pF		15		%
t_s	Settling Time 0.1% [1] V_{in} = ±1V, A_{VCL} = -1		60		ns
t_r, t_f	Rise and Fall Time (see note 1) V_{in} = ±100mV, A_{VCL} = 2		2		ns
t_d	Delay Time (see note 1) V_{in} = ±100mV, A_{VCL} = 2		2		ns
ϕm	Phase Margin A_{VM} = 2, R_L = 100Ω, C_L = 15pF		45		Degrees
THD	Total Harmonic Distortion A_{VCL} = 10, f = 1kHz, V_o = ±2.5V, no load		0.02		%
FPB	Full Power Bandwidth [2] Vo = 5Vpp, R_L = 100Ω Vo = 2Vpp, R_L = 100Ω		26 64		MHz

1. See test waveform figure
2. Full power bandwidth = $\frac{SR}{\Pi Vopp}$

TEST WAVEFORM



EVALUATION CIRCUIT



PRINTED CIRCUIT LAYOUT

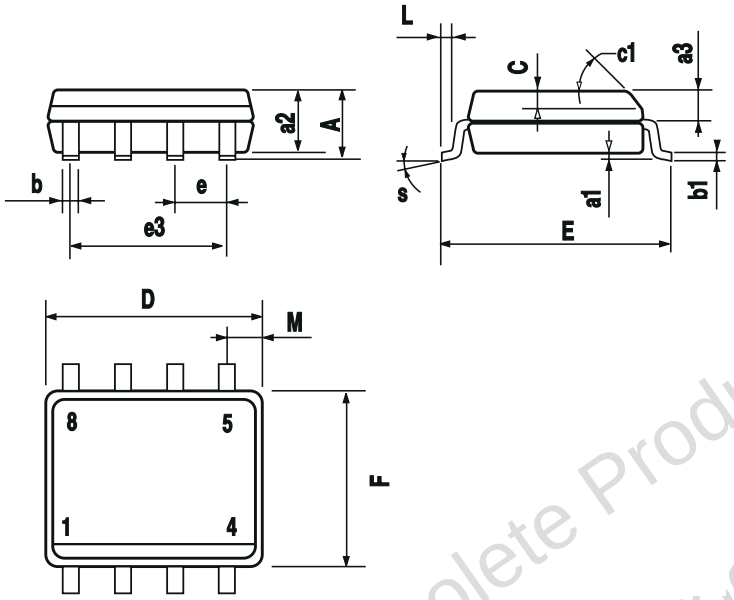
As for any high frequency device, a few rules must be observed when designing the PCB to get the best performances from this high speed op amp.

From the most to the least important points :

- Each power supply lead has to be bypassed to ground with a 10nF ceramic capacitor very close to the device and a 10µF tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitance and inductance.
- Use small resistor values to decrease time constant with parasitic capacitance.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. You can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					