19-3345; Rev 0; 8/04

EVALUATION KIT AVAILABLE

8kHz Reference Clock Synthesizer with Multiple Outputs at 35.328MHz

General Description

The MAX9486 low-cost, high-performance clock synthesizer with an 8kHz input reference clock provides six buffered LVTTL clock outputs at 35.328MHz. The clock synthesizer can be used to generate the clocks for T1, E1, T3, E3, and xDSL.

The MAX9486 has two phase-lock loops (PLLs). The first PLL uses a voltage-controlled crystal oscillator (VCXO). The second PLL is a frequency multiplier. With the two PLLs, the MAX9486 generates the output frequency at 35.328MHz. In addition, this device generates a jitter-suppressed 8kHz output that provides a better source for the reference clock relay.

The MAX9486 is available in a 24-pin TSSOP package and operates over the extended operating temperature range of -40°C to +85°C and a single +3V to +3.6V power-supply range.

Features

- **8kHz Input Reference CLK**
- **High-Jitter Rejection on the Reference CLK**
- **Synthesizer Locks to the 8kHz Reference with a ±200ppm Range**
- **Output Frequency: 35.328MHz**
- **Six Buffered LVTTL Low-Jitter Outputs**
- **One 8kHz Reference CLK Relay Output**
- **+3.3V Supply Operation**
- **24-Pin TSSOP Package**

Applications

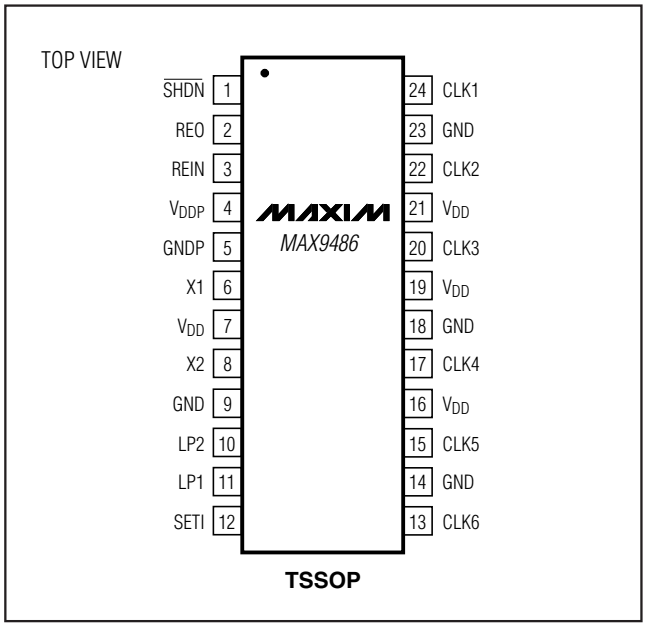
Telecom Equipment Using T1, E1, T3, E3, and ISDN Protocols

xDSL Equipment in CO with Interface to the Telecom Protocols

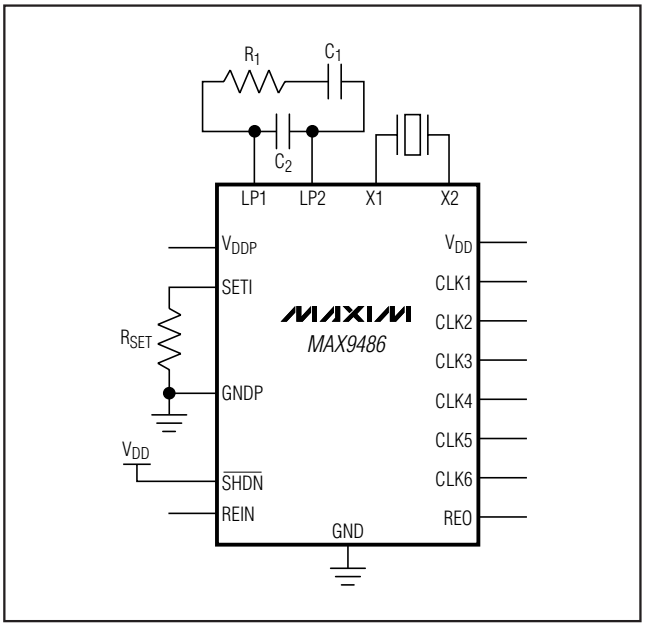
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9486EUG	-40°C to +85°C	24 TSSOP

Pin Configuration



Typical Application Circuit



8kHz Reference Clock Synthesizer with Multiple Outputs at 35.328MHz

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +4.0V
V_{DDP} to GNDP .....-0.3V to +4.0V
$\overline{SHDN}$, REO, REIN, X1, X2, CLK_ to GND ...-0.3V to (V_{DD} + 0.3V)
LP1, SETI to GNDP .....-0.3V to (V_{DD} + 0.3V)
LP2 Internally Connected to GNDP
Short-Circuit Duration of Outputs .....Continuous

Continuous Power Dissipation (T_A = +70°C)
24-Pin TSSOP (derate 12.2mW/°C above +70°C) 976mW
Operating Temperature Range .....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
ESD Rating (Human Body Model) .....±2kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DDP} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = V_{DDP} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (REIN, $\overline{SHDN}$)						
Input High Logic Level	V_{IH}		2.0			V
Input Low Logic Level	V_{IL}				0.8	V
Input-Current High Level	I_{IH}	V_{IN} = V_{DD}			20	µA
Input-Current Low Level	I_{IL}	V_{IN} = 0	-20			µA
DIGITAL OUTPUT CLOCKS (CLK1–CLK6, REO)						
Output High Logic Level	V_{OH}	I_{OH} = -4mA	V_{DD} - 0.6V			V
Output Low Logic Level	V_{OL}	I_{OL} = 4mA			0.4	V
POWER SUPPLY (V_{DD}, V_{DDP})						
Power-Supply Range	V_{DD}		3.0		3.6	V
PLL Power-Supply Range	V_{DDP}		3.0		3.6	V
Power-Supply Current	I_{DD} + I_{DDP}	(Note 2)		13	25	mA
Shutdown Supply Current	$I_{\overline{SHDN}}$			8	30	µA

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DDP} = +3.0V to +3.6V, C_L = 20pF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = V_{DDP} = +3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUT CLOCKS (CLK1–CLK6)						
Frequency Range	f_{OUT}			35.328		MHz
Clock Rise Time	T_{R1}	20% to 80% V_{DD}		1.8		ns
Clock Fall Time	T_{F1}	80% to 20% V_{DD}		1.8		ns
Duty Cycle			40	50	60	%
Period Jitter	J_{PP1}	Peak-to-peak		120		ps
Output Skew	t_S	Peak-to-peak		185		ps
REFERENCE CLOCK OUTPUT (REO)						
Frequency	f_{REF}			8		kHz
Clock Rise Time	T_{R2}			1.8		ns
Clock Fall Time	T_{F2}			1.8		ns
Duty Cycle			40	50	60	%
VCXO						
Crystal Frequency	f_{XTL}			17.664		MHz
Crystal Accuracy		Including frequency accuracy and temperature range		±25		ppm
VCXO Pulling Range		(Note 4)	-200		+200	ppm
Input Reference CLK Pulse Width	t_W	Measured at high or low states	10			ns

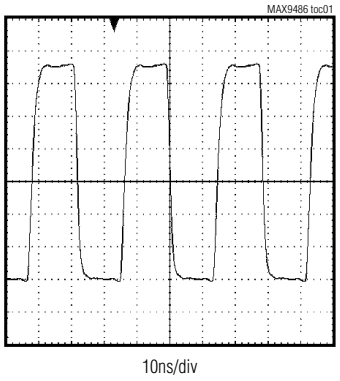
Note 1: Specifications are 100% tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.
Note 2: No load on clock outputs.
Note 3: Guaranteed by design.
Note 4: Crystal loading capacitance is 14pF.

8kHz Reference Clock Synthesizer with Multiple Outputs at 35.328MHz

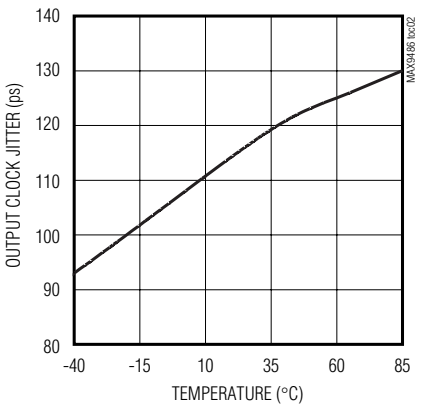
Typical Operating Characteristics

(V_{DD} = V_{DDP} = +3.3V, T_A = +25°C, unless otherwise noted.)

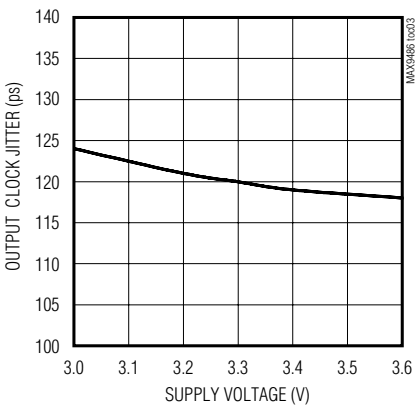
OUTPUT WAVEFORM



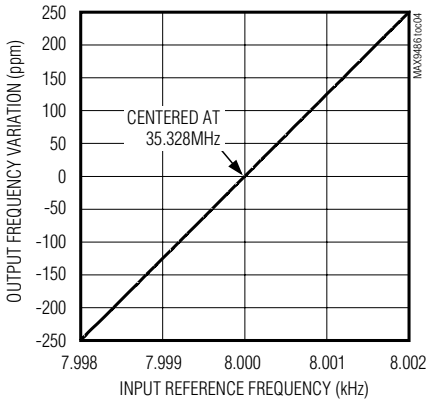
OUTPUT CLOCK JITTER (P-P) vs. TEMPERATURE



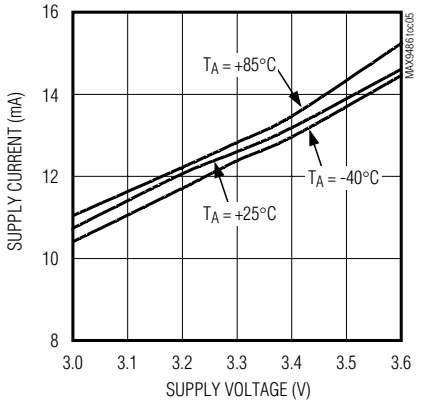
OUTPUT CLOCK JITTER (P-P) vs. SUPPLY VOLTAGE



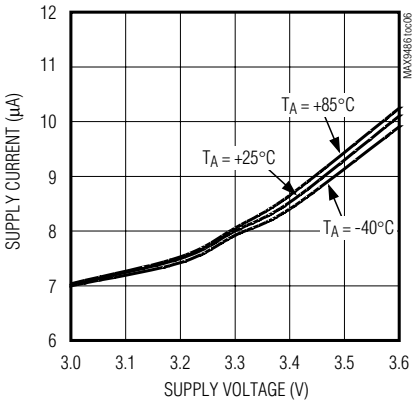
OUTPUT FREQUENCY VARIATION vs. INPUT REFERENCE FREQUENCY



SUPPLY CURRENT (I_{DD} + I_{DDP}) vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE

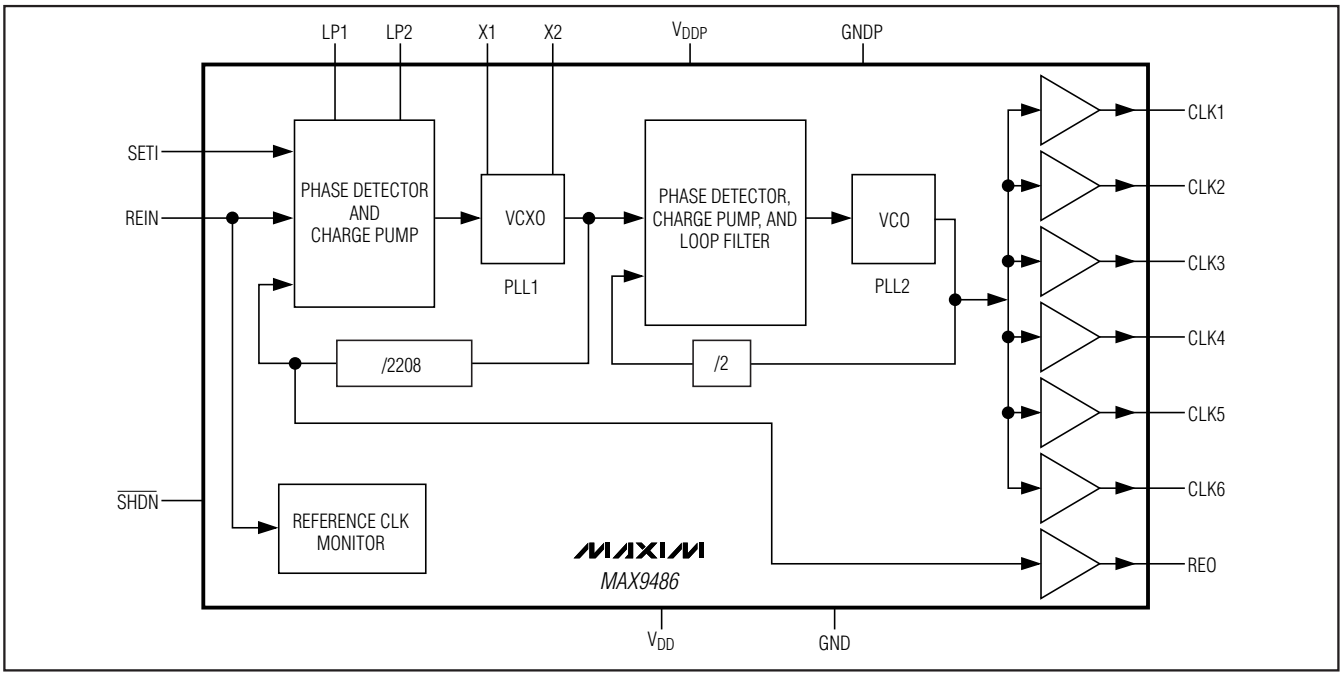


Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Active-Low Shutdown Input
2	REO	Reference Clock Output. REO is an 8kHz reference clock output with jitter suppression.
3	REIN	Reference Input
4	V_{DDP}	Phase-Lock Loop (PLL) Power Supply. Bypass V_{DDP} with 0.1µF and 0.001µF capacitors to GNDP.
5	GNDP	PLL Ground
6	X1	Crystal Input 1. Connect X1 to a fundamental mode crystal for the VCXO.
7, 16, 19, 21	V_{DD}	Digital Power Supply. Bypass V_{DD} with 0.1µF and 0.001µF capacitors to GND.
8	X2	Crystal Input 2. Connect X2 to a fundamental mode crystal for the VCXO.
9, 14, 18, 23	GND	Ground
10	LP2	External Filter 2. Connect the loop filter capacitors and a resistor between LP1 and LP2 *(*see the *Typical Application Circuit).* LP2 is internally connected to GNDP.
11	LP1	External Filter 1. Connect the loop filter capacitors and a resistor between LP1 and LP2 *(*see the *Typical Application Circuit).*
12	SETI	Charge-Pump Current-Setting Input. Connect a resistor from SETI to GNDP to set PLL charge-pump current (see the *Detailed Description* section).
13	CLK6	Clock Output 6 at 35.328MHz
15	CLK5	Clock Output 5 at 35.328MHz
17	CLK4	Clock Output 4 at 35.328MHz
20	CLK3	Clock Output 3 at 35.328MHz
22	CLK2	Clock Output 2 at 35.328MHz
24	CLK1	Clock Output 1 at 35.328MHz

8kHz Reference Clock Synthesizer with Multiple Outputs at 35.328MHz

Functional Diagram



Detailed Description

The MAX9486 is a high-performance clock synthesizer with an 8kHz input reference clock. This device generates six identical buffered LVTTL clock outputs at 35.328MHz. The MAX9486 features two PLLs. The first PLL (PLL1) uses an internal VCXO, locked to the 8kHz reference CLK, to generate a 17.664MHz CLK output for the second PLL (PLL2). PLL2 multiplies the VCXO frequency by a factor of 2 to produce the 35.328MHz outputs. In addition, this device features a low-jitter 8kHz output that provides a better source for the reference clock relay (see the *Functional Diagram*).

Power-Up

At power-up, all the outputs are disabled and pulled low (to GND) for at least 256ms. After 256ms, the crystal oscillator starts oscillation. The input reference clock for PLL1 is 8kHz and its output frequency, 17.664MHz, is also the reference clock for PLL2. If the 8kHz reference clock is not present at power-up, the output frequency of PLL1 is locked to the center frequency of the crystal oscillator.

8kHz Reference CLK Monitor

The MAX9486 features an internal clock (CLK) monitor circuitry to detect the presence of the external 8kHz reference clock. The internal CLK monitor continuously monitors the number of low-to-high transitions within a three-cycle (at 8kHz) time window. If the transition number is less than two, the internal CLK monitor states loss of the reference CLK. However, if in a three-cycle time window the monitor counts two or three transitions, it considers the input reference clock as present. When the monitor detects the absence of the 8kHz reference clock, PLL2 is forced to lock to the crystal oscillator frequency. However, when the monitor detects the return of the reference clock, PLL1 locks to the reference clock again.

Clock Outputs (CLK1 to CLK6) and REO

The MAX9486 uses a 17.664MHz crystal and a reference clock (REIN) to generate six identical outputs, CLK1 to CLK6, at 35.328MHz. All CLK_ outputs are LVTTL with a skew of 185ps. The MAX9486 also regenerates the 8kHz reference CLK at REO output.

Voltage-Controlled Crystal Oscillator (VCXO)

The MAX9486's internal VCXO takes an external 17.664MHz crystal as the base frequency and has a pulling range of approximately ±200ppm. This configuration also makes the VCXO PLL become a narrowband filter to reject high-frequency jitter on the input reference and eliminate it from the REO and CLK_ outputs.

$\overline{SHDN}$ Mode

The MAX9486 features a shutdown mode with a supply current less than 8µA (typ). Drive $\overline{SHDN}$ low to get the device into shutdown mode. In this mode, all the outputs go low and both PLLs are powered down. After $\overline{SHDN}$ goes high, the outputs still stay low for an additional 256ms to allow both PLLs to be stabilized before the outputs are enabled again.

Applications Information

Crystal Selection

The MAX9486 uses a 17.664MHz crystal as the base frequency for the VCXO. It is important to use a correct type of quartz crystal to avoid reducing frequency pulling range, or excessive output phase jitter.

Choose an AT-cut crystal that oscillates at 17.664MHz on its fundamental mode with a variation of ±25ppm including frequency accuracy and operating temperature range. The crystal's load capacitance should be 14pF. Pulling range may vary depending on the crystal used. Refer to the MAX9486 evaluation kit for details.

PLL1 Loop Filter

The MAX9486 features two PLLs: PLL1 and PLL2. The first phased-lock loop, PLL1, contains an integrated VCXO that uses an external crystal to track the input reference signal and attenuate input jitter. Figure 1 shows the external loop filter of the PLL containing resistor R1 and two capacitors, C1 and C2. This loop filter is connected between LP1 and LP2 as shown in the *Typical Operating Circuit*. The loop-filter bandwidth is determined by C1, C2, R1, and R_{SET} where R_{SET} is used to set the value of the charge-pump current. The typical values of C1, C2, R1, and R_{SET} are 22nF, 560pF, 1000kΩ, and 13kΩ, respectively.

Use the following equation to calculate a PLL loop bandwidth in Hz:

$$BW = (R1 \times I_{SETI} \times 940) / N$$

where R1 (Ω) is the resistor in the PLL1 loop filter (Figure 1), I_{SETI} (A) is the charge-pump current calculated from the equation in the *Charge-Pump Current Setting* section, and N is the crystal PLL frequency divider equal to 2208.

The loop-damping factor is calculated by:

$$DampingFactor = \frac{R_1}{2} \times \sqrt{\frac{5900 \times I_{SETI} \times C_1}{N}}$$

where C1 (F) and R1 (Ω) are the values of the capacitor and the resistor in the PLL1 loop filter shown in Figure 1; I_{SETI} is calculated as shown in the *Charge-Pump Current Setting* section and N = 2208.

The following equation shows the relationship between components C1 and C2 in the loop filter:

$$C2 \le C1/20$$

Charge-Pump Current Setting

The MAX9486 also allows external setting of the charge-pump current in PLL1. Connect a resistor from SETI to GNDP to set the PLL1 charge-pump current:

$$\text{Charge-Pump Current} = 2.4 \times 1000 / (R_{SET}(k\Omega) + 1)$$

where R_{SET} is in kΩ and the value of the charge-pump current is in µA.

The loop response can be adjusted to meet individual application requirements since the charge-pump current and all the filter components for the VCXO loop can be set externally.

Board Layout and Bypassing

The MAX9486's high-oscillator frequency makes proper layout important to ensure stability. For best performance, place components as close as possible to the device.

Digital or AC transient signals on GND can create noise at the clock outputs. Return GND to the highest quality ground available. Bypass V_{DD} and V_{DDP} with 0.1µF and 0.001µF capacitors, placed as close to the device as possible. Careful PC board ground layout minimizes crosstalk between the outputs and digital inputs.

Traces must be as short as possible on LP1 and LP2 and connect the capacitors and the resistor as close as possible to the device.

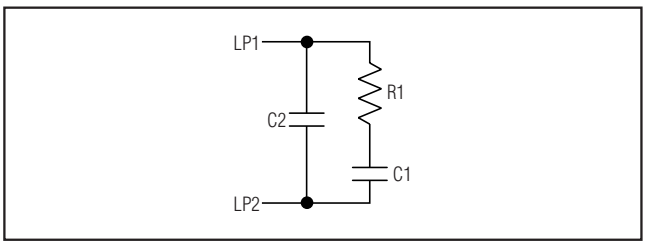


Figure 1. Typical Loop Filter

Chip Information

TRANSISTOR COUNT: 7512

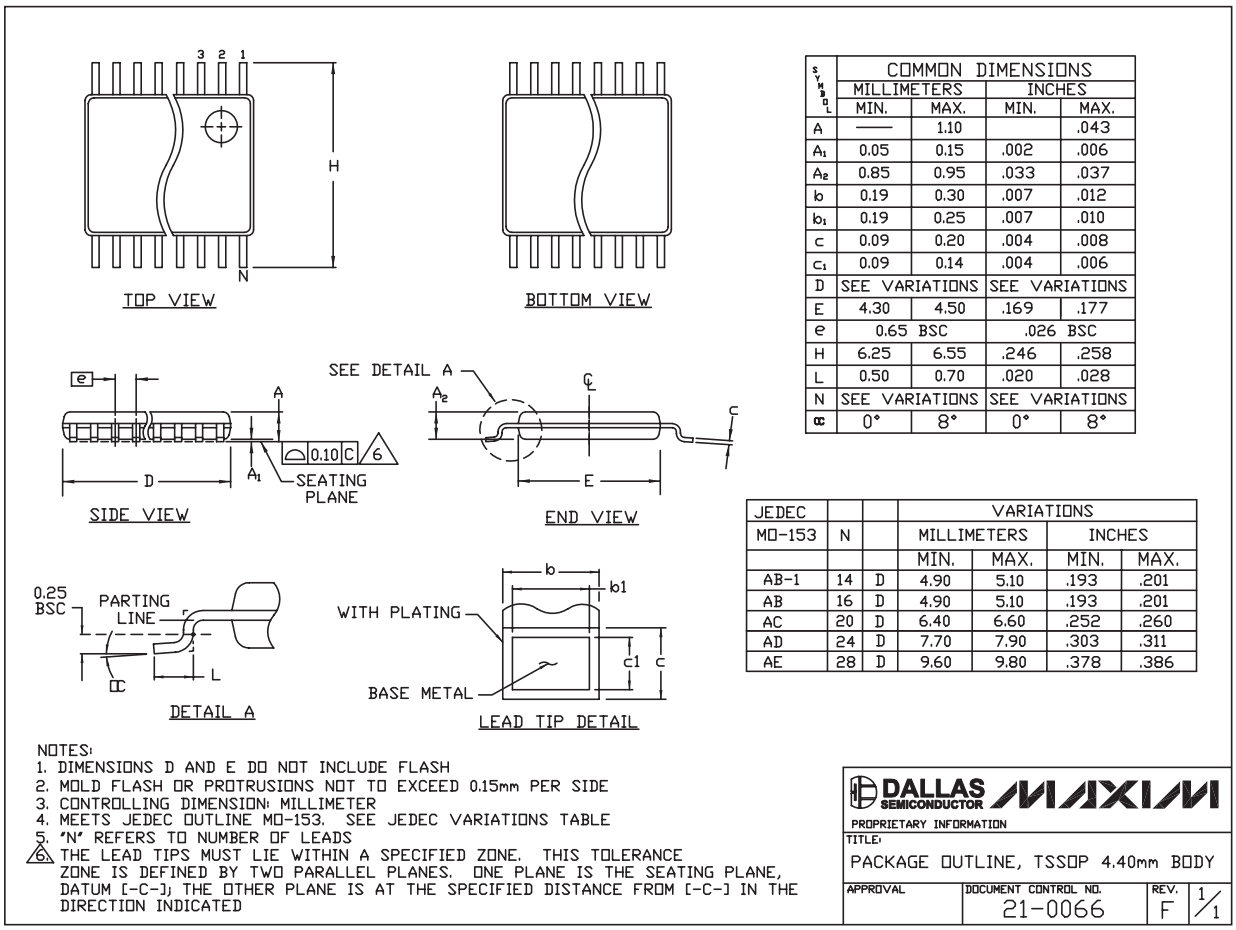
PROCESS: CMOS

8kHz Reference Clock Synthesizer with Multiple Outputs at 35.328MHz

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1