# 700 MHz to 1050 MHz Quadrature Demodulator with Fractional-N PLL

Data Sheet

# ADRF6807

## FEATURES

- IQ demodulator with integrated fractional-N PLL
- LO frequency range: 700 MHz to 1050 MHz
- For the following specifications (LPEN = 0)/(LPEN = 1):
  - Input P1dB: 12.8 dBm/11.7 dBm
  - Input IP3: 26.7 dBm/24.0 dBm
  - Noise figure (DSB): 13.1 dB/12.4 dB
  - Voltage conversion gain: 1.0 dB/4.3 dB
- Quadrature demodulation accuracy
  - Phase accuracy: <0.5°
  - Amplitude accuracy: <0.1 dB
  - Baseband demodulation: 170 MHz/135 MHz, 3 dB bandwidth
- SPI serial interface for PLL programming
- 40-lead, 6 mm × 6 mm LFCSP

## APPLICATIONS

- QAM/QPSK RF/IF demodulators
- Cellular W-CDMA/CDMA/CDMA2000
- Microwave point-to-(multi)point radios
- Broadband wireless and WiMAX

## GENERAL DESCRIPTION

The ADRF6807 is a high dynamic range IQ demodulator with integrated phase-locked loop (PLL) and voltage controlled oscillator (VCO). The fractional-N PLL/synthesizer generates a frequency in the range of 2.8 GHz to 4.2 GHz. A programmable quadrature divider (divide ratio = 4) divides the output frequency of the VCO down to the required local oscillator (LO) frequency to drive the mixers in quadrature. Additionally, an output divider (divide ratio = 4 to 8) generates a divided-down VCO signal for external use.

The PLL reference input is supported from 9 MHz to 160 MHz. The phase detector output controls a charge pump whose output is integrated in an off-chip loop filter. The loop filter output is then applied to an integrated VCO.

The IQ demodulator mixes the differential RF input with the complex LO derived from the quadrature divider. The differential I and Q output paths have excellent quadrature accuracy and can handle baseband signaling or complex IF up to 120 MHz.

A reduced power mode of operation is also provided by programming the serial interface registers to reduce current consumption, with slightly degraded input linearity and output current drive.

The ADRF6807 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40-lead, exposed paddle, RoHS-compliant, 6 mm × 6 mm LFCSP package. Performance is specified over the −40°C to +85°C temperature range.

## FUNCTIONAL BLOCK DIAGRAM

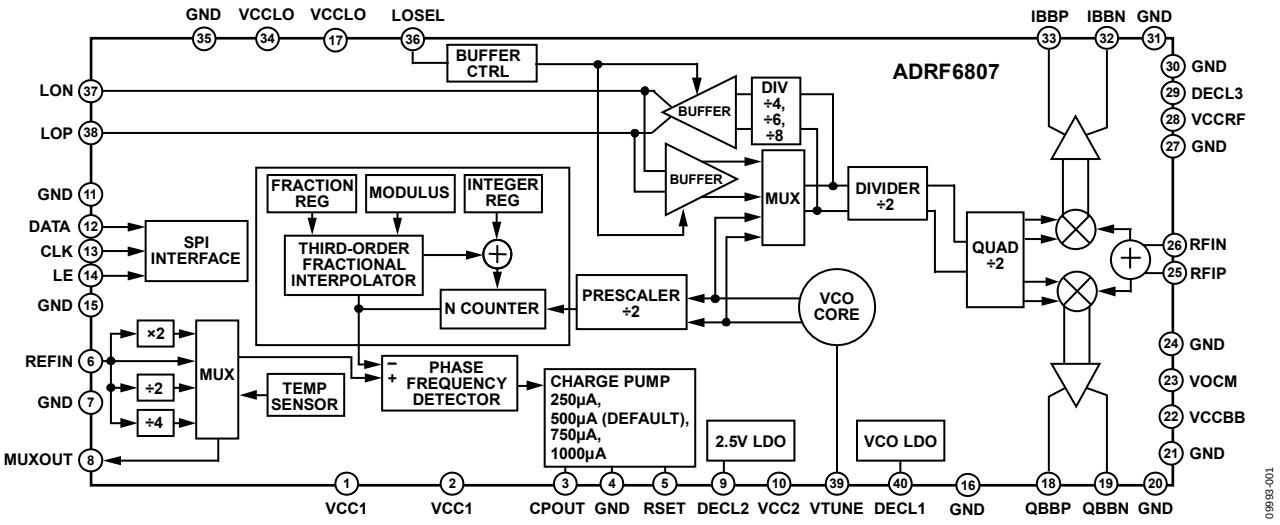


*Figure 1.*

**Rev. B**



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## EVALUATION KITS

- ADRF6807 Evaluation Board

## DOCUMENTATION

**Data Sheet**

- ADRF6807: 700 MHz to 1050 MHz Quadrature Demodulator with Fractional-N PLL Data Sheet

## SOFTWARE AND SYSTEMS REQUIREMENTS

- ADRF6807 Evaluation Board Software (Adapter board with USB controlled Cypress Microcontroller)
- ADRF6807 Evaluation Board Software and Documentation
- Windows 7 Drivers for the SPI Software

## TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

## REFERENCE MATERIALS

**Product Selection Guide**

- RF Source Booklet

## DESIGN RESOURCES

- ADRF6807 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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# TABLE OF CONTENTS



## REVISION HISTORY

**2/12—Rev. A to Rev. B**

Changes to Table 1 ... 3
Changes to Figure 21 and to Changes to Figure 24 Through Figure 26 ... 12
Changes to Figure 34 ... 16
Changes to Figure 37 ... 18
Changes to Figure 38 ... 19
Changes to Figure 39 ... 20
Changes to EVM Measurements Section and Changes to Figure 42 ... 24
Changes to Figure 43 ... 25
Added Figure 44; Renumbered Sequentially ... 26
Changes to Figure 45 and Figure 46 ... 27
Changes to Table 7 ... 29
Changes to Figure 47 ... 30
Changes to Figure 48 ... 31

**9/11—Rev. 0 to Rev. A**

Changes to EVM Measurements Section and Figure 42 ... 24

**8/11—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{S1}$ ($V_{VCCBB}$ and $V_{VCCRF}$) = 5 V, and $V_{S2}$ ($V_{VCC1}$, $V_{VCC2}$, and $V_{VCCLO}$) = 3.3 V; ambient temperature ($T_A$) = 25°C; $f_{REF}$ = 26 MHz, $f_{LO}$ = 900 MHz, $f_{BB}$ = 4.5 MHz, $R_{LOAD}$ = 450 Ω differential, RF port driven from a 1:2 balun to step up the 50 Ω source impedance to match the 100 Ω differential RF input port impedance, all register and PLL settings use the recommended values shown in the Register Structure section, unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| FREQUENCY RANGE | | 700 | | 1050 | MHz |
| RF INPUT at 900 MHz | RFIP, RFIN pins | | | | |
| Input Return Loss | Relative to 100 Ω | | −18 | | dB |
| Input P1dB | LPEN = 0 (standard power mode) | | 12.8 | | dBm |
| | LPEN = 1 (low power mode) | | 11.7 | | dBm |
| Second-Order Input Intercept (IIP2) | LPEN = 0; −5 dBm each tone | | >65 | | dBm |
| | LPEN = 1; −5 dBm each tone | | >65 | | dBm |
| Third-Order Input Intercept (IIP3) | LPEN = 0; −5 dBm each tone | | 26.7 | | dBm |
| | LPEN = 1; −5 dBm each tone | | 24.0 | | dBm |
| Noise Figure | Double sideband from RF to either I or Q output; LPEN = 0 | | 13.1 | | dB |
| | Double sideband from RF to either I or Q output; LPEN = 1 | | 12.4 | | dB |
| | With a −5 dBm interferer 5 MHz away | | 16 | | dB |
| LO-to-RF Leakage | At 1×LO frequency, 100 Ω termination at the RF port | | −73 | | dBm |
| I/Q BASEBAND OUTPUTS | IBBP, IBBN, QBBP, QBBN pins | | | | |
| Voltage Conversion Gain | 450 Ω differential load across IBBP, IBBN (or QBBP, QBBN); LPEN = 0 | | 1 | | dB |
| | 450 Ω differential load across IBBP, IBBN (or QBBP, QBBN); LPEN = 1 | | 4.3 | | dB |
| Demodulation Bandwidth | 1 V p-p signal 3 dB bandwidth; LPEN = 0 | | 170 | | MHz |
| | 1 V p-p signal 3 dB bandwidth; LPEN = 1 | | 135 | | MHz |
| Quadrature Phase Error | | | 0.35 | | Degrees |
| I/Q Amplitude Imbalance | | | 0.05 | | dB |
| Output DC Offset (Differential) | | | ±8 | | mV |
| Output Common-Mode Reference | VOCM applied input voltage | 1.55 | 1.65 | 1.75 | V |
| Common-Mode Offset | $\lvert(V_{IBBP} + V_{IBBN})/2 - V_{VOCM}\rvert$, $\lvert(V_{QBBP} + V_{QBBN})/2 - V_{VOCM}\rvert$ | | 25 | | mV |
| Gain Flatness | Any 5 MHz | | 0.2 | | dB p-p |
| Maximum Output Swing | Differential 450 Ω load | | 3 | | V p-p |
| | Differential 200 Ω load | | 2.4 | | V p-p |
| Maximum Output Current | Each pin | | 6 | | mA p-p |
| LO INPUT/OUTPUT | LOP, LON | | | | |
| Output Level (LPEN = 0) | Into a differential 50 Ω load, LO buffer enabled (output frequency = 800 MHz) | | 1 | | dBm |
| Output Level (LPEN = 1) | Into a differential 50 Ω load, LO buffer enabled (output frequency = 800 MHz) | | −0.75 | | dBm |
| Input Level | Externally applied 2×LO, PLL disabled | | 0 | | dBm |
| Input Impedance | Externally applied 2×LO, PLL disabled | | 50 | | Ω |
| LO Main Divider | VCO to mixer, including quadrature divider, see Table 5 for divider programming | | 4 | | |
| VCO Output Divider Range | VCO to (LOP, LON), see Table 6 for supported output divider modes | 4 | | 8 | |
| VCO Operating Frequency | | 2800 | | 4200 | MHz |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SYNTHESIZER SPECIFICATIONS | All synthesizer specifications measured with recommended settings provided in Figure 33 through Figure 40 | | | | |
| Channel Spacing | $f_{PFD}$ = 26 MHz | | 25 | | kHz |
| PLL Bandwidth | Can be adjusted with off-chip loop filter component values and $R_{SET}$ | | 67 | | kHz |
| SPURS | $f_{LO}$ = 900 MHz, $f_{REF}$ = 26 MHz, $f_{PFD}$ = 26 MHz, measured at baseband outputs with $f_{BB}$ = 50 MHz | | | | |
| Reference Spurs | $f_{REF}$ = 26 MHz, $f_{PFD}$ = 26 MHz | | −93 | | dBc |
| | $f_{REF}/2$ | | −104 | | dBc |
| | $f_{REF} \times 2$ | | −85 | | dBc |
| | $f_{REF} \times 3$ | | −97 | | dBc |
| PHASE NOISE (USING 67 kHz LOOP FILTER) | $f_{LO}$ = 900 MHz, $f_{REF}$ = 26 MHz, $f_{PFD}$ = 26 MHz, measured at baseband outputs with $f_{BB}$ = 50 MHz | | | | |
| | At 1 kHz offset | | −104 | | dBc/Hz |
| | At 10 kHz offset | | −107 | | dBc/Hz |
| | At 100 kHz offset | | −111 | | dBc/Hz |
| | At 500 kHz offset | | −131 | | dBc/Hz |
| | At 1 MHz offset | | −138 | | dBc/Hz |
| | At 5 MHz offset | | −149 | | dBc/Hz |
| | At 10 MHz offset | | −152 | | dBc/Hz |
| Integrated Phase Noise | 1 kHz to 10 MHz integration bandwidth | | 0.13 | | °rms |
| Phase Detector Frequency | | 20 | 26 | 40 | MHz |
| PHASE NOISE (USING 2.5 kHz LOOP FILTER) | $f_{LO}$ = 900 MHz, $f_{REF}$ = 26 MHz, $f_{PFD}$ = 26 MHz, measured at baseband outputs with $f_{BB}$ = 50 MHz | | | | |
| | At 1 kHz offset | | −73 | | dBc/Hz |
| | At 10 kHz offset | | −90 | | dBc/Hz |
| | At 100 kHz offset | | −119 | | dBc/Hz |
| | At 500 kHz offset | | −135 | | dBc/Hz |
| | At 1 MHz offset | | −141 | | dBc/Hz |
| | At 5 MHz offset | | −150 | | dBc/Hz |
| | At 10 MHz offset | | −152 | | dBc/Hz |
| PLL FIGURE OF MERIT (FOM) | Measured with $f_{REF}$ = 26 MHz, $f_{PFD}$ = 26 MHz | | −215.4 | | dBc/Hz/Hz |
| | Measured with $f_{REF}$ = 104 MHz, $f_{PFD}$ = 26 MHz | | −220.9 | | dBc/Hz/Hz |
| Phase Detector Frequency | | 20 | 26 | 40 | MHz |
| REFERENCE CHARACTERISTICS | REFIN, MUXOUT pins | | | | |
| REFIN Input Frequency | Usable range | 9 | | 160 | MHz |
| REFIN Input Capacitance | | | 4 | | pF |
| MUXOUT Output Level | $V_{OL}$ (lock detect output selected) | | | 0.25 | V |
| | $V_{OH}$ (lock detect output selected) | 2.7 | | | V |
| REFOUT Duty Cycle | | | 50 | | % |
| CHARGE PUMP | | | | | |
| Pump Current | | | 500 | | µA |
| Output Compliance Range | | 1 | | 2.8 | V |
| LOGIC INPUTS | CLK, DATA, LE pins | | | | |
| Input High Voltage, $V_{INH}$ | | 1.4 | | 3.3 | V |
| Input Low Voltage, $V_{INL}$ | | 0 | | 0.7 | V |
| Input Current, $I_{INH}/I_{INL}$ | | | 0.1 | | µA |
| Input Capacitance, $C_{IN}$ | | | 5 | | pF |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLIES | VCC1, VCC2, VCCLO, VCCBB, VCCRF pins | | | | |
| Voltage Range (3.3 V) | VCC1, VCC2, VCCLO | 3.135 | 3.3 | 3.465 | V |
| Voltage Range (5 V) | VCCBB, VCCRF | 4.75 | 5 | 5.25 | V |
| Supply Current (3.3 V) (LPEN = 0) | Normal Rx mode | | 170 | | mA |
| | Rx mode with LO buffer enabled | | 227 | | mA |
| Supply Current (5 V) (LPEN = 0) | Normal Rx mode | | 86 | | mA |
| | Rx mode with LO buffer enabled | | 86 | | mA |
| Supply Current (3.3 V) (LPEN = 1) | Normal Rx mode | | 166 | | mA |
| | Rx mode with LO buffer enabled | | 214 | | mA |
| Supply Current (5 V) (LPEN = 1) | Normal Rx mode | | 76 | | mA |
| | Rx mode with LO buffer enabled | | 76 | | mA |
| Supply Current (5 V) | Power-down mode | | 10 | | mA |
| Supply Current (3.3 V) | Power-down mode | | 15 | | mA |

## TIMING CHARACTERISTICS

$V_{S1}$ ($V_{VCCBB}$ and $V_{VCCRF}$) = 5 V, and $V_{S2}$ ($V_{VCC1}$, $V_{VCC2}$, and $V_{VCCLO}$) = 3.3 V.

**Table 2.**

| Parameter | Limit at $T_{MIN}$ to $T_{MAX}$ | Unit | Test Conditions/Comments |
|---|---|---|---|
| $t_1$ | 20 | ns min | LE setup time |
| $t_2$ | 10 | ns min | DATA to CLK setup time |
| $t_3$ | 10 | ns min | DATA to CLK hold time |
| $t_4$ | 25 | ns min | CLK high duration |
| $t_5$ | 25 | ns min | CLK low duration |
| $t_6$ | 10 | ns min | CLK to LE setup time |
| $t_7$ | 20 | ns min | LE pulse width |

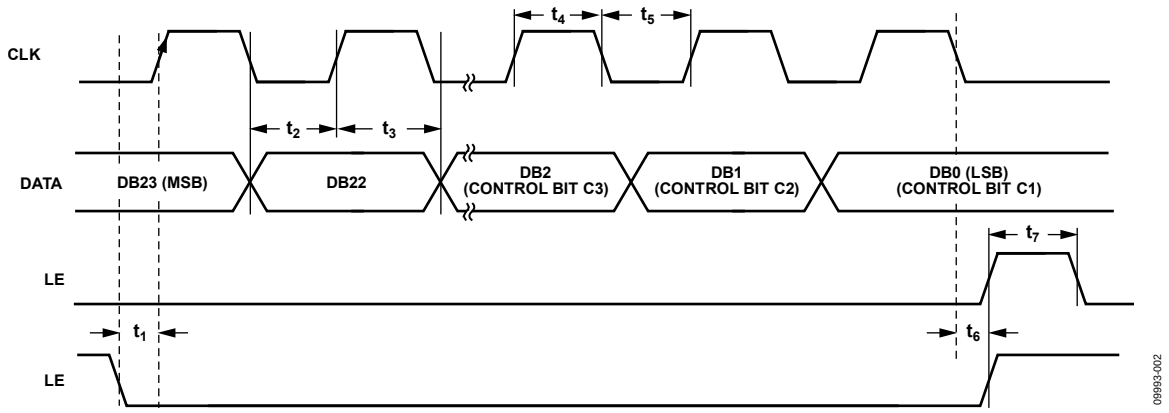



*Figure 2. Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

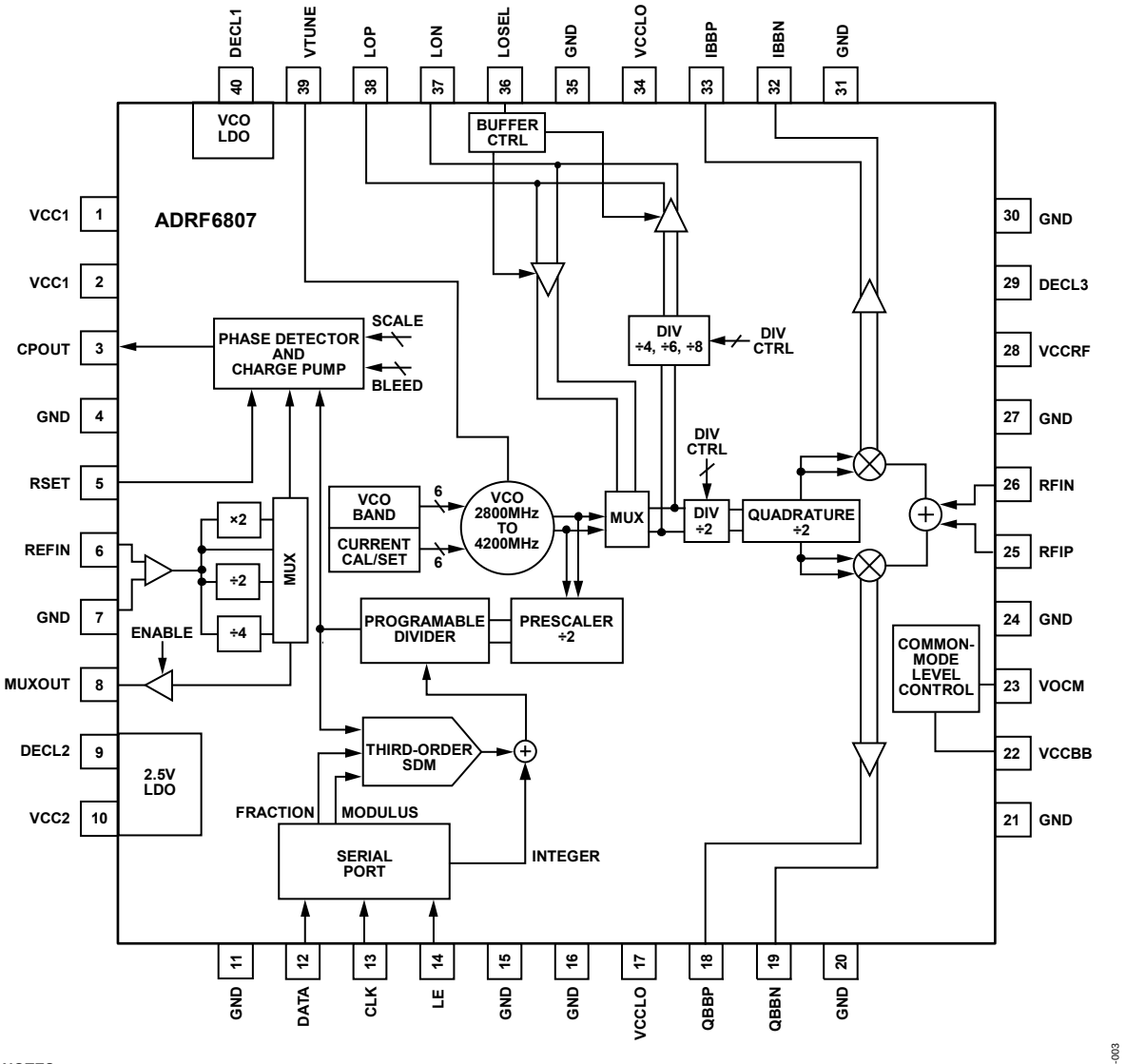
| Parameter | Rating |
|---|---|
| Supply Voltage, VCCBB and VCCRF ($V_{S1}$) | −0.5 V to +5.5 V |
| Supply Voltage, VCC1, VCC2, and VCCLO ($V_{S2}$) | −0.5 V to +3.6 V |
| Digital I/O, CLK, DATA, and LE | −0.3 V to +3.6 V |
| RFIP and RFIN (Each Pin AC-Coupled) | 13 dBm |
| $\theta_{JA}$ (Exposed Paddle Soldered Down) | 30°C/W |
| Maximum Junction Temperature | 150°C |
| Operating Temperature Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




NOTES
1. THE EXPOSED PADDLE SHOULD BE SOLDERED TO A LOW IMPEDANCE GROUND PLANE.

*Figure 3. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 2 | VCC1 | The 3.3 V Power Supply for VCO and PLL. |
| 3 | CPOUT | Charge Pump Output Pin. Connect this pin to VTUNE through the loop filter. |
| 4, 7, 11, 15, 16, 20, 21, 24, 27, 30, 31, 35 | GND | Ground. Connect these pins to a low impedance ground plane. |
| 5 | RSET | Charge Pump Current. The nominal charge pump current can be set to 250 µA, 500 µA, 750 µA, or 1 mA using DB10 and DB11 of Register 4 and by setting DB18 to 0 (internal reference current). In this mode, no external $R_{SET}$ is required. If DB18 is set to 1, the four nominal charge pump currents ($I_{NOMINAL}$) can be externally tweaked according to the following equation where the resulting value is in units of ohms. $R_{SET} = \left[\frac{217.4 \times I_{CP}}{I_{NOMINAL}}\right] - 37.8$ |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 6 | REFIN | Reference Input. Nominal input level is 1 V p-p. Input range is 9 MHz to 160 MHz. |
| 8 | MUXOUT | Multiplexer Output. This output can be programmed to provide the reference output signal or the lock detect signal. The output is selected by programming the appropriate register. |
| 9 | DECL2 | Connect a 0.1 µF capacitor between this pin and ground. |
| 10 | VCC2 | 3.3 V Power Supply for 2.5 V LDO. |
| 12 | DATA | Serial Data Input. The serial data is loaded MSB first with the three LSBs being the control bits. |
| 13 | CLK | Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. Maximum clock frequency is 20 MHz. |
| 14 | LE | Load Enable. When the LE input pin goes high, the data stored in the shift registers is loaded into one of the six registers, the relevant latch being selected by the first three control bits of the 24-bit word. |
| 17, 34 | VCCLO | 3.3 V Power Supply for LO Path Blocks. |
| 18, 19 | QBBP, QBBN | Demodulator Q-Channel Differential Baseband Outputs (Differential Output Impedance of 28 Ω). |
| 22 | VCCBB | 5 V Power Supply for Demodulator Blocks. |
| 23 | VOCM | Baseband Common-Mode Reference Input; 1.65 V Nominal. It sets the dc common-mode level of the IBBx and QBBx outputs. |
| 25, 26 | RFIP, RFIN | Differential 100 Ω, Internally Biased RF Inputs. These pins must be ac-coupled. |
| 28 | VCCRF | 5 V Power Supply for Demodulator Blocks. |
| 29 | DECL3 | Connect a 2.2 µF capacitor between this pin and ground. |
| 32, 33 | IBBN, IBBP | Demodulator I-Channel Differential Baseband Outputs (Differential Output Impedance of 28 Ω). |
| 36 | LOSEL | LO Select. Connect this pin to ground for the simplest operation and to completely control the LO path and input/output direction from the register programming of the SPI.<br>For additional control without register reprogramming, this input pin can determine whether the LOP and LON pins operate as inputs or outputs. LOP and LON become inputs if the LOSEL pin is set low, the LDRV bit of Register 5 is set low, and the LXL bit of Register 5 is set high. The externally applied LO drive must be at M×LO frequency (where M corresponds to the main LO divider setting). LON and LOP become outputs when LOSEL is high or if the LDRV bit of Register 5 (DB3) is set high and the LXL bit of Register 5 (DB4) is set to low. The output frequency is controlled by the LO output divider bits in Register 7. This pin should not be left floating. |
| 37, 38 | LON, LOP | Local Oscillator Input/Output (Differential Output Impedance of 28 Ω). When these pins are used as output pins, a differential frequency divided version of the internal VCO is available on these pins. When the internal LO generation is disabled, an external M×LO frequency signal can be applied to these pins, where M corresponds to the main divider setting. |
| 39 | VTUNE | VCO Control Voltage Input. This pin is driven by the output of the loop filter. The nominal input voltage range on this pin is 1.0 V to 2.8 V. |
| 40 | DECL1 | Connect a 10 µF capacitor between this pin and ground as close to the device as possible because this pin serves as the VCO supply and loop filter reference. |
| | EP | Exposed Paddle. The exposed paddle should be soldered to a low impedance ground plane. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{S1}$ = 5 V, $V_{S2}$ = 3.3 V, $T_A$ = 25°C, RF input balun loss is de-embedded, unless otherwise noted. LO = 700 MHz to 1050 MHz; Mini-Circuits ADTL2-18 balun on RF inputs.

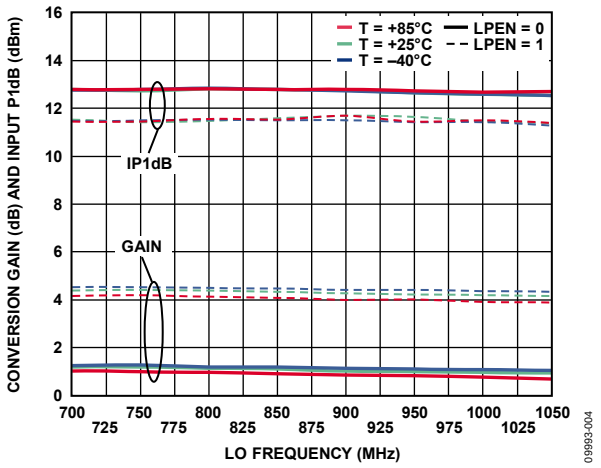



Figure 4. Conversion Gain and Input P1dB vs. LO Frequency

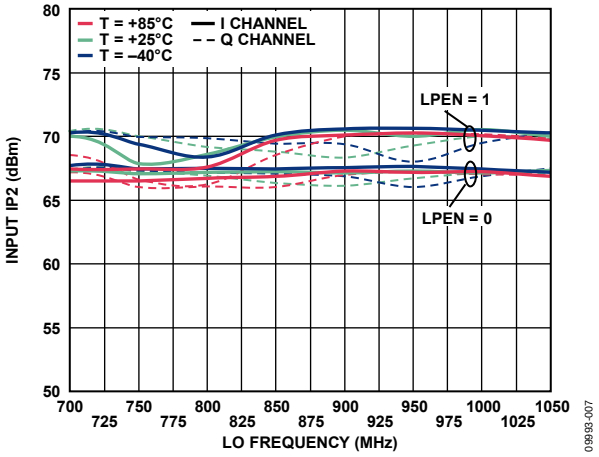



Figure 7. Input IP2 vs. LO Frequency

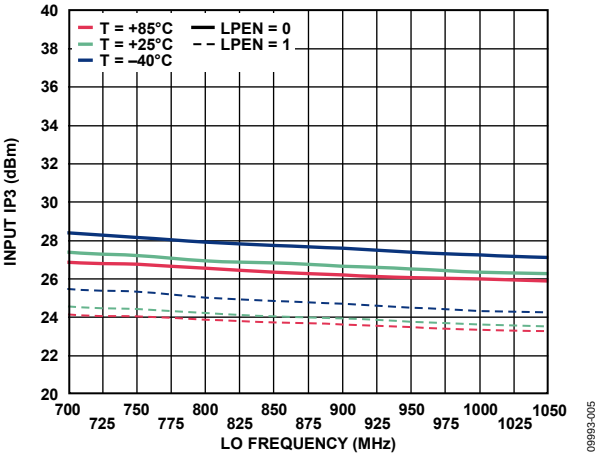



Figure 5. Input IP3 vs. LO Frequency

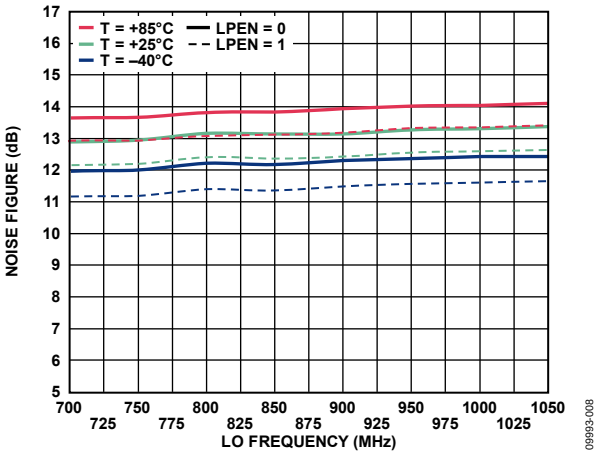



Figure 8. Noise Figure vs. LO Frequency

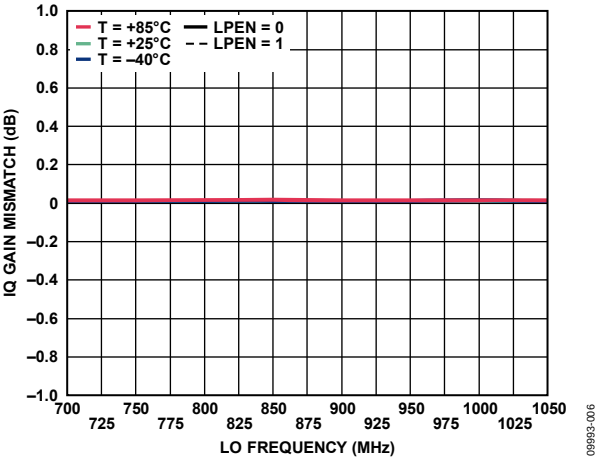



Figure 6. IQ Gain Mismatch vs. LO Frequency

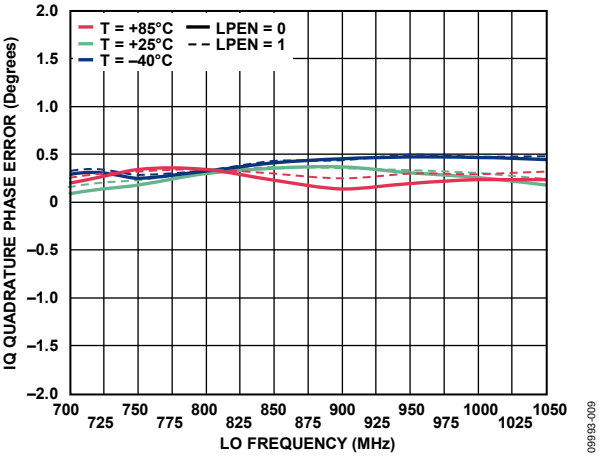



Figure 9. IQ Quadrature Phase Error vs. LO Frequency

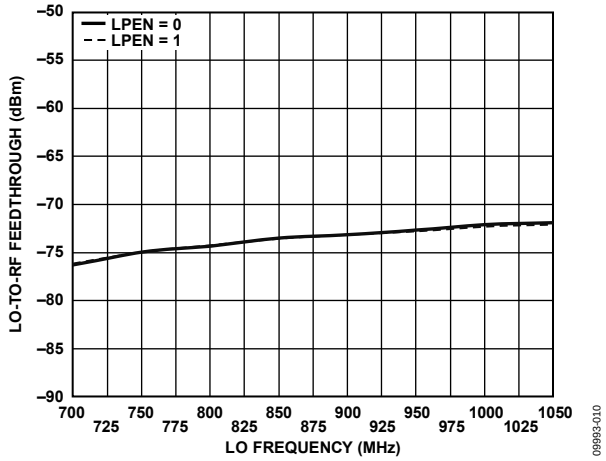



Figure 10. LO-to-RF Feedthrough vs. LO Frequency, LO Output Turned Off

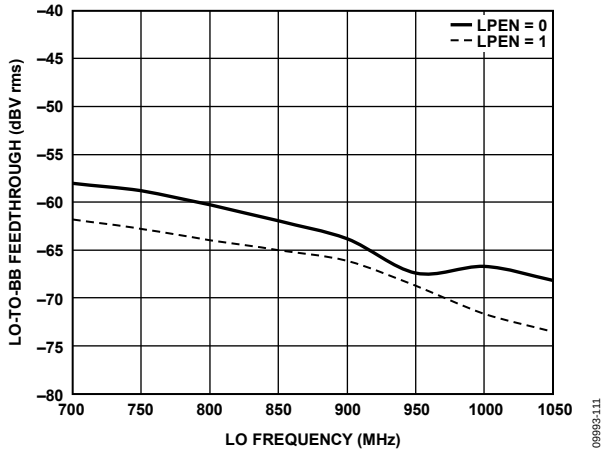



Figure 11. LO-to-BB Feedthrough vs. LO Frequency, LO Output Turned Off

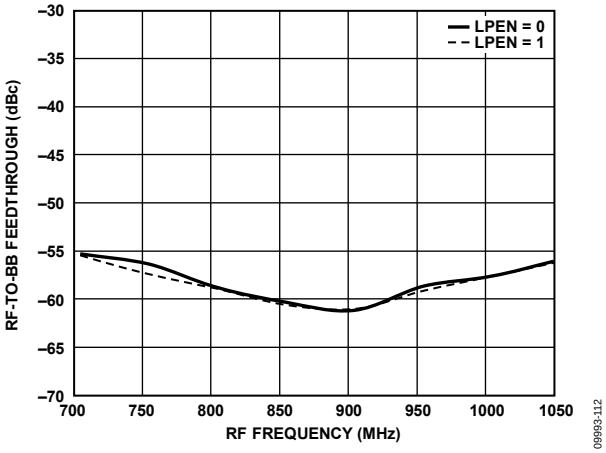



Figure 12. RF-to-BB Feedthrough vs. RF Frequency

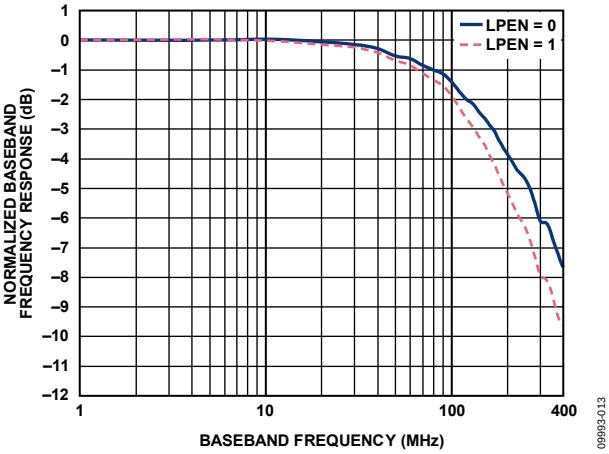



Figure 13. Normalized BB Frequency Response

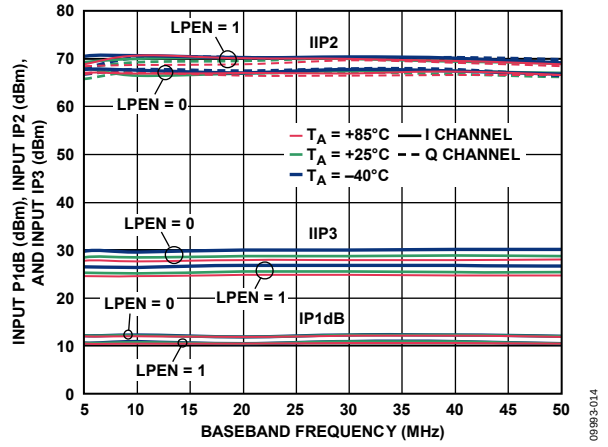



Figure 14. Input P1dB, Input IP2, and Input IP3 vs. BB Frequency

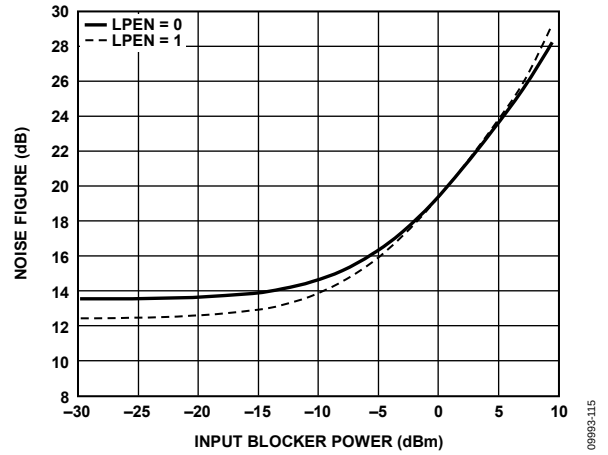



Figure 15. Noise Figure vs. Input Blocker Power, $f_{LO}$ = 900 MHz (RF Blocker 5 MHz Offset)

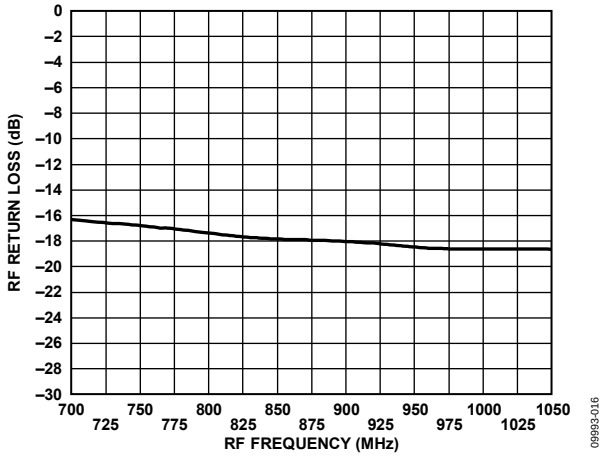



Figure 16. RF Input Return Loss vs. RF Frequency, Measured Through ADTL2-18 2-to-1 Input Balun

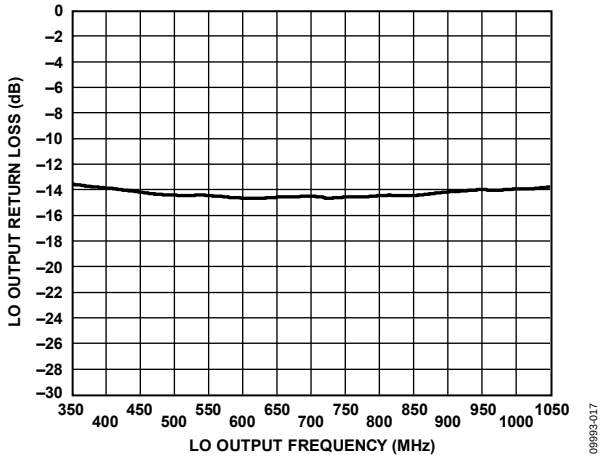



Figure 17. LO Output Return Loss vs. LO Output Frequency, LO Output Enabled (350 MHz to 1050 MHz)

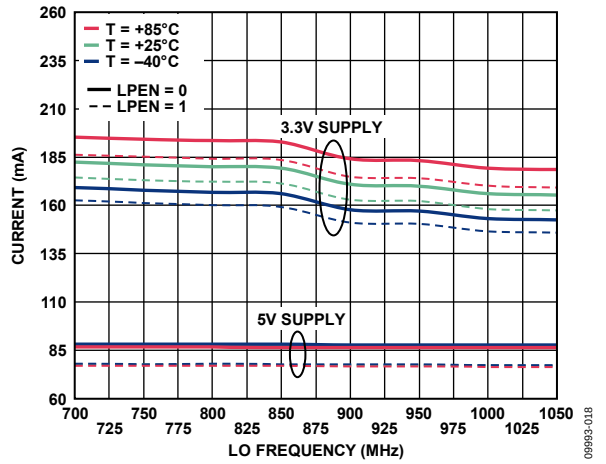



Figure 18. 5 V and 3.3 V Supply Currents vs. LO Frequency, LO Output Disabled

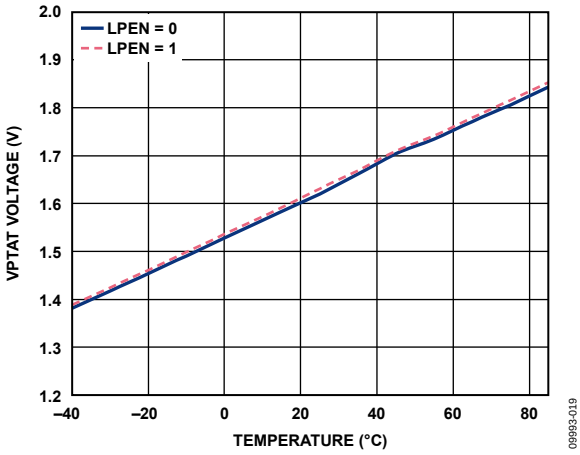



Figure 19. VPTAT Voltage vs. Temperature

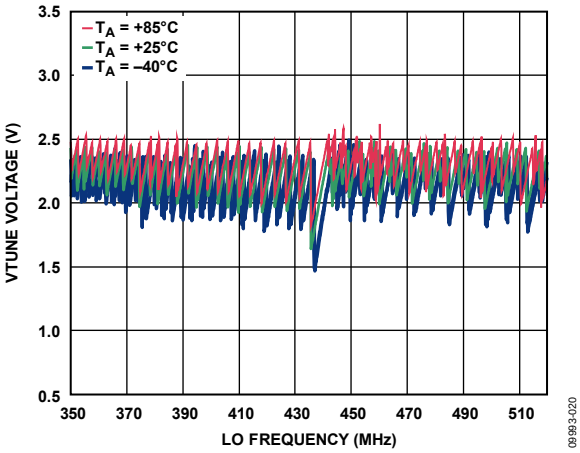



Figure 20. VTUNE Voltage vs. LO Frequency, Measured at the LO Output Pins with LO Output in Divide-by-8 Mode

## SYNTHESIZER/PLL

$V_{S1}$ = 5 V, $V_{S2}$ = 3.3 V, see the Register Structure section for recommended settings used. External loop filter bandwidth of ~67 kHz, $f_{REF} = f_{PFD}$ = 26 MHz, measured at BB output, $f_{BB}$ = 50 MHz, unless otherwise noted.

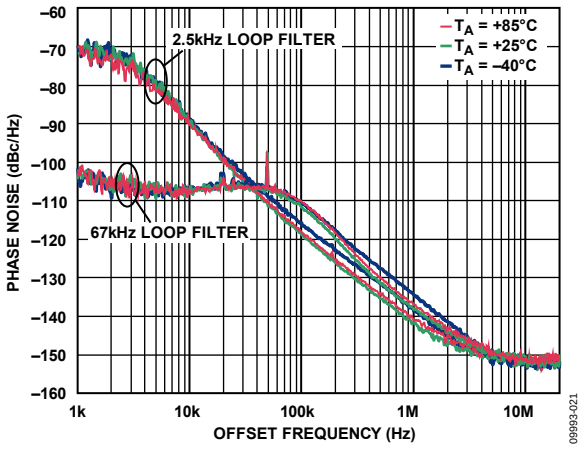



Figure 21. Phase Noise vs. Offset Frequency, $f_{LO}$ = 900 MHz

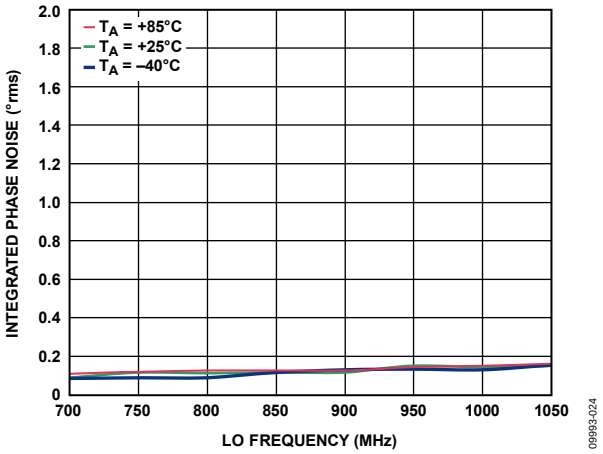



Figure 24. Integrated Phase Noise vs. LO Frequency (Spurs Omitted)

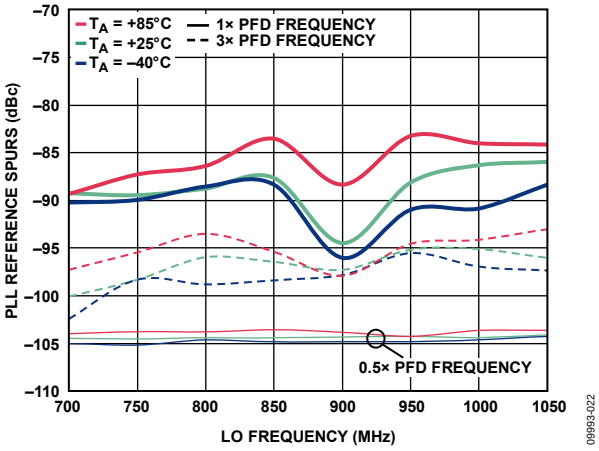



Figure 22. PLL Reference Spurs vs. LO Frequency

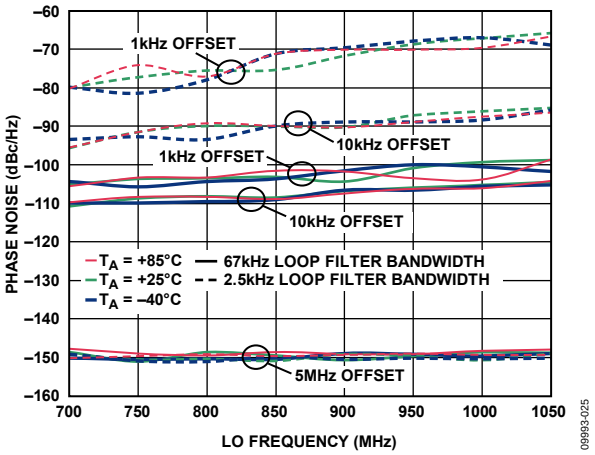



Figure 25. Phase Noise vs. LO Frequency (1 kHz, 10 kHz, and 5 MHz Offsets)

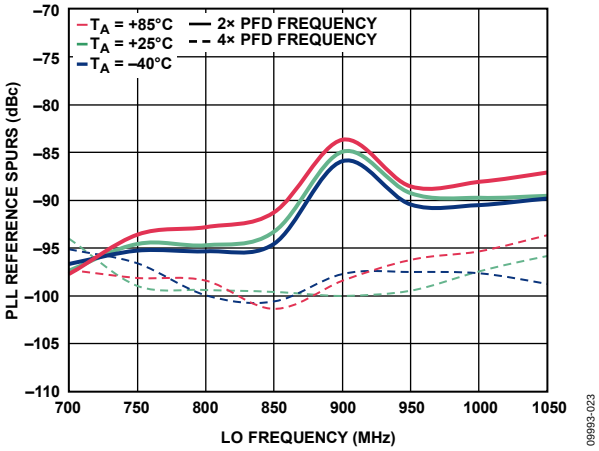



Figure 23. PLL Reference Spurs vs. LO Frequency

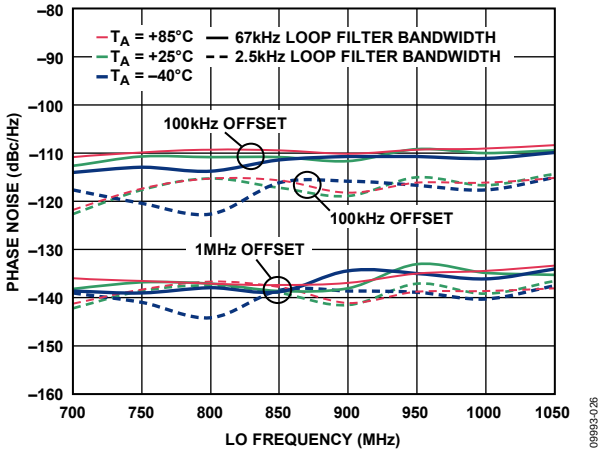



Figure 26. Phase Noise vs. LO Frequency (100 kHz and 1 MHz Offsets)

## COMPLEMENTARY CUMULATIVE DISTRIBUTION FUNCTIONS (CCDF)

$V_{S1}$ = 5 V, $V_{S2}$ = 3.3 V, $f_{LO}$ = 900 MHz, $f_{BB}$ = 4.5 MHz.

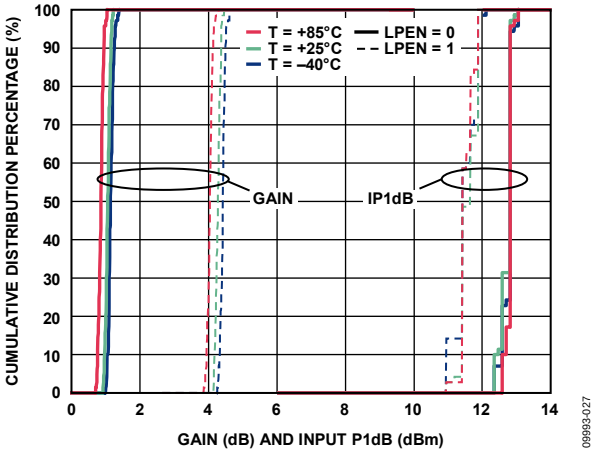



Figure 27. Gain and Input P1dB

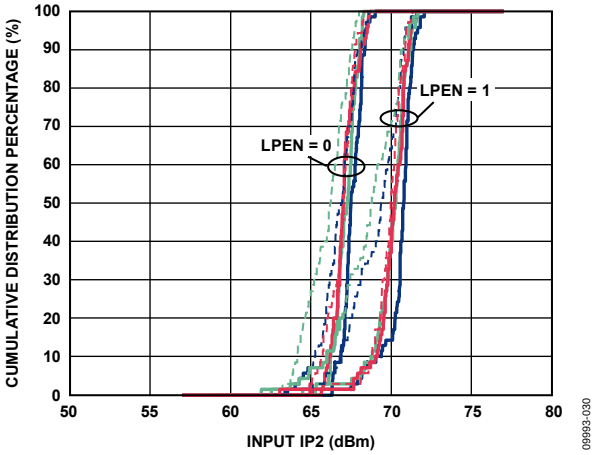



Figure 30. Input IP2

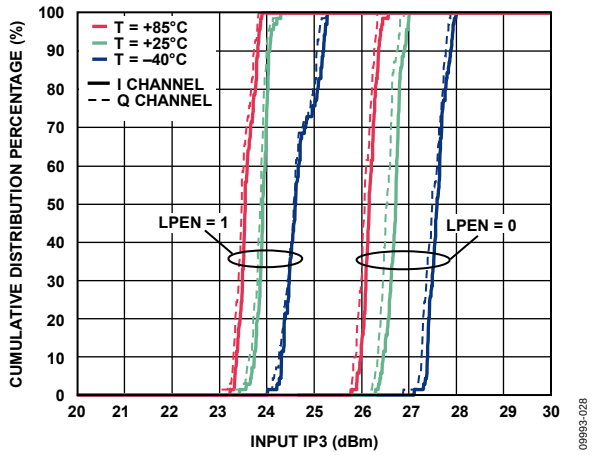



Figure 28. Input IP3

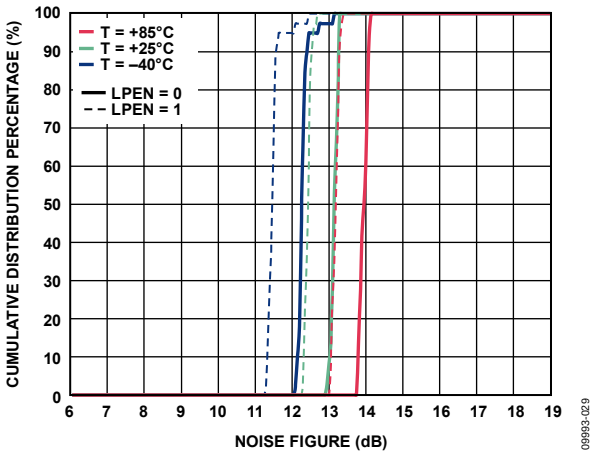



Figure 31. Noise Figure

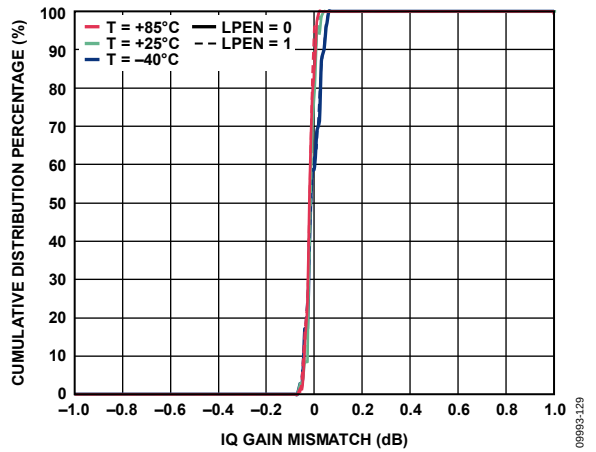



Figure 29. IQ Gain Mismatch

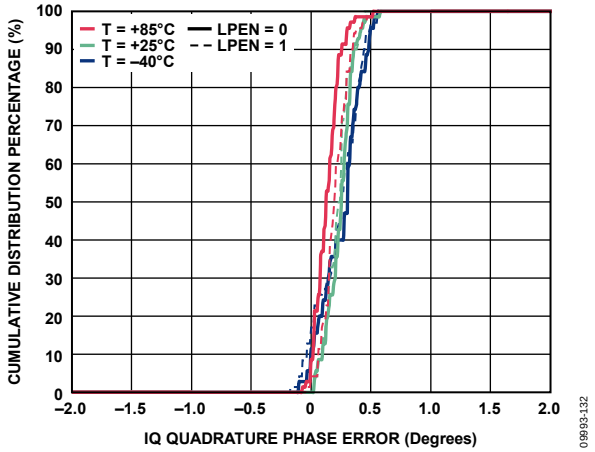



Figure 32. IQ Quadrature Phase Error

# CIRCUIT DESCRIPTION

The ADRF6807 integrates a high performance IQ demodulator with a state-of-the-art fractional-N PLL. The PLL also integrates a low noise VCO. The SPI port allows the user to control the fractional-N PLL functions, the demodulator LO divider functions, and optimization functions, as well as allowing for an externally applied LO.

The ADRF6807 uses a high performance mixer core that results in an exceptional input IP3 and input P1dB, with a very low output noise floor for excellent dynamic range.

## LO QUADRATURE DRIVE

A signal at 2× the desired mixer LO frequency is delivered to a divide-by-2 quadrature phase splitter followed by limiting amplifiers, which then drive the I and Q mixers, respectively.

## V-TO-I CONVERTER

The differential RF input signal is applied to a V-to-I converter that converts the differential input voltage to output currents. The V-to-I converter provides a differential 100 Ω input impedance. The V-to-I bias current can be reduced by putting the device in low power mode (setting LPEN = 1 by setting Register 5, DB5 = 1). Generally with LPEN = 1, input IP3 and input P1dB degrade, but the noise figure is slightly better. Overall, the dynamic range is reduced by setting LPEN = 1.

## MIXERS

The ADRF6807 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistive loads that then feed into the subsequent emitter follower buffers. When the part is put into its low power mode (LPEN = 1), the mixer core load resistors are increased, which does increase the gain by roughly 3 dB; however, as previously stated in the V-to-I Converter section, the overall dynamic range does decrease slightly.

## EMITTER FOLLOWER BUFFERS

The output emitter followers drive the differential I and Q signals off chip. The output impedance is set by on-chip 14 Ω series resistors that yield a 28 Ω differential output impedance for each baseband port. The fixed output impedance forms a voltage divider with the load impedance that reduces the effective gain. For example, a 500 Ω differential load has ~0.5 dB lower effective gain than a high (10 kΩ) differential load impedance.

The common-mode dc output levels of the emitter follower outputs are set by the voltage applied to the VOCM pin. The VOCM pin must be driven with a voltage (typically 1.65 V) for the emitter follower buffers to function. If the VOCM pin is left open, the emitter follower outputs do not bias up properly.

## BIAS CIRCUITRY

There are several band gap reference circuits and two low dropout regulators (LDOs) in the ADRF6807 that generate the reference currents and voltages used by different sections. One of the LDOs is the 2.5V_LDO, which is always active and provides the 2.5 V supply rail used by the internal digital logic blocks. The 2.5V_LDO output is connected to the DECL2 pin (Pin 9) for the user to provide external decoupling. The other LDO is the VCO_LDO, which acts as the positive supply rail for the internal VCO. The VCO_LDO output is connected to the DECL1 pin (Pin 40) for the user to provide external decoupling. The VCO_LDO can be powered down by setting Register 6, DB18 = 0, which allows the user to save power when not using the VCO. Additionally, the bias current for the mixer V-to-I stage, which drives the mixer core, can be reduced by putting the device in low power mode (setting LPEN = 1 by setting Register 5, DB5 = 1).

## REGISTER STRUCTURE

The ADRF6807 provides access to its many programmable features through a 3-wire SPI control interface that is used to program the seven internal registers. The minimum delay and hold times are shown in the timing diagram (see Figure 2). The SPI provides digital control of the internal PLL/VCO as well as several other features related to the demodulator core, on-chip referencing, and available system monitoring functions. The MUXOUT pin provides a convenient, single-pin monitor output signal that can be used to deliver a PLL lock-detect signal or an internal voltage proportional to the local junction temperature.

Note that internal calibration for the PLL must run when the ADRF6807 is initialized at a given frequency. This calibration is run automatically whenever Register 0, Register 1, or Register 2 is programmed. Because the other registers affect PLL performance, Register 0, Register 1, and Register 2 must always be programmed last. For ease of use, starting the initial programming with Register 7 and then programming the registers in descending order ending with Register 0 is recommended. Once the PLL and other settings are programmed, the user can change the PLL frequency simply by programming Register 0, Register 1, or Register 2 as necessary.

| | | | | | | | | | | | | | DIVIDE MODE | INTEGER DIVIDE RATIO | | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DM | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | C3(0) | C2(0) | C1(0) |

| DM | DIVIDE MODE |
|---|---|
| 0 | FRACTIONAL (DEFAULT) |
| 1 | INTEGER |

| ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | DIVIDE RATIO |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 21 (INTEGER MODE ONLY) |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 22 (INTEGER MODE ONLY) |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 23 (INTEGER MODE ONLY) |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 24 |
| ... | ... | ... | ... | ... | ... | ... | ... |
| ... | ... | ... | ... | ... | ... | ... | ... |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 56 (DEFAULT) |
| ... | ... | ... | ... | ... | ... | ... | ... |
| ... | ... | ... | ... | ... | ... | ... | ... |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 119 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 120 (INTEGER MODE ONLY) |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 121 (INTEGER MODE ONLY) |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 122 (INTEGER MODE ONLY) |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 123 (INTEGER MODE ONLY) |

09993-031

*Figure 33. Integer Divide Control Register (R0)*

### *Register 0—Integer Divide Control*

With R0[2:0] set to 000, the on-chip integer divide control register is programmed as shown in Figure 33. The internal VCO frequency ($f_{VCO}$) equation is

$$f_{VCO} = f_{PFD} \times (INT + (FRAC/MOD)) \times 2 \quad (1)$$

where:

$f_{VCO}$ is the output frequency of the internal VCO.
*INT* is the preset integer divide ratio value (21 to 123 for integer mode, 24 to 119 for fractional mode).
*FRAC* is the preset fractional divider ratio value (0 to MOD − 1).
*MOD* is the preset fractional modulus (1 to 2047).

The integer divide ratio sets the INT value in Equation 1. The INT, FRAC, and MOD values make it possible to generate output frequencies that are spaced by fractions of the PFD frequency.

Note that the demodulator LO frequency is given by $f_{LO} = f_{VCO}/M$, where M is the programmed LO main divider (see Table 5).

### *Divide Mode*

Divide mode determines whether fractional mode or integer mode is used. In integer mode, the VCO output frequency, $f_{VCO}$, is calculated by

$$f_{VCO} = f_{PFD} \times (INT) \times 2 \quad (2)$$

### *Register 1—Modulus Divide Control*

With R1[2:0] set to 001, the on-chip modulus divide control register is programmed as shown in Figure 34. The MOD value is the preset fractional modulus ranging from 1 to 2047.

| | | | | | | | | | | MODULUS DIVIDE RATIO | | | | | | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD10 | MD9 | MD8 | MD7 | MD6 | MD5 | MD4 | MD3 | MD2 | MD1 | MD0 | C3(0) | C2(0) | C1(1) |

| MD10 | MD9 | MD8 | MD7 | MD6 | MD5 | MD4 | MD3 | MD2 | MD1 | MD0 | MODULUS VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1536 (DEFAULT) |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2047 |

09993-032

*Figure 34. Modulus Divide Control Register (R1)*

### *Register 2—Fractional Divide Control*

With R2[2:0] set to 010, the on-chip fractional divide control register is programmed as shown in Figure 35. The FRAC value is the preset fractional modulus ranging from 0 to MOD − 1.

| | | | | | | | | | | FRACTIONAL DIVIDE RATIO | | | | | | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FD10 | FD9 | FD8 | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 | C3(0) | C2(1) | C1(0) |

| FD10 | FD9 | FD8 | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 | FRACTIONAL VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 768 (DEFAULT) |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| FRACTIONAL VALUE MUST BE LESS THAN MODULUS | | | | | | | | | | | <MDR |

09993-033

*Figure 35. Fractional Divide Control Register (R2)*

### *Register 3—Sigma Delta (Σ-Δ) Modulator Dither Control*

With R3[2:0] set to 011, the on-chip Σ-Δ modulator dither control register is programmed as shown in Figure 36. The dither restart value can be programmed from 0 to 217, though a value of 1 is typically recommended.

| | DITHER MAGNITUDE | | DITHER ENABLE | DITHER RESTART VALUE | | | | | | | | | | | | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | DITH1 | DITH0 | DEN | DV16 | DV15 | DV14 | DV13 | DV12 | DV11 | DV10 | DV9 | DV8 | DV7 | DV6 | DV5 | DV4 | DV3 | DV2 | DV1 | DV0 | C3(0) | C2(1) | C1(1) |

| DEN | DITHER ENABLE |
|---|---|
| 0 | DISABLE |
| 1 | ENABLE (DEFAULT, RECOMMENDED) |

| DITH1 | DITH0 | DITHER MAGNITUDE |
|---|---|---|
| 0 | 0 | 15 (DEFAULT) |
| 0 | 1 | 7 |
| 1 | 0 | 3 |
| 1 | 1 | 1 (RECOMMENDED) |

| DV16 | DV15 | DV14 | DV13 | DV12 | DV11 | DV10 | DV9 | DV8 | DV7 | DV6 | DV5 | DV4 | DV3 | DV2 | DV1 | DV0 | DITHER RESTART VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0x00001 (DEFAULT) |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0x1FFFF |

09993-034

*Figure 36. Σ-Δ Modulator Dither Control Register (R3)*

### *Register 4—Charge Pump, PFD, and Reference Path Control*

With R4[2:0] set to 100, the on-chip charge pump, PFD, and reference path control register is programmed as shown in Figure 37.

The charge pump current is controlled by the base charge pump current ($I_{CP, BASE}$), and the value of the charge pump current multiplier ($I_{CP, MULT}$).

The base charge pump current can be set using an internal or external resistor (according to DB18 of Register 4). When using an external resistor, the value of $I_{CP, BASE}$ can be varied according to

$$R_{SET}\ [\Omega] = \left[\frac{217.4 \times I_{CP, BASE}}{250}\right] - 37.8$$

The actual charge pump current can be programmed to be a multiple (1, 2, 3, or 4) of the charge pump base current. The multiplying value ($I_{CP, MULT}$) is equal to 1 plus the value of the DB11 and DB10 bits in Register 4.

The PFD phase offset multiplier ($\theta_{PFD, OFS}$), which is set by Bit DB16 to Bit DB12 of Register 4, causes the PLL to lock with a nominally fixed phase offset between the PFD reference signal and the divided-down VCO signal. This phase offset is used to linearize the PFD-CP transfer function and can improve fractional spurs. The magnitude of the phase offset is determined by

$$|\Delta\Phi|[\text{deg}] = 22.5\frac{\theta_{PFD, OFS}}{I_{CP, MULT}}$$

Finally, the phase offset can be either positive or negative, depending on the value of the DB17 bit in Register 4.

The reference frequency applied to the PFD can be manipulated using the internal reference path source. The external reference frequency applied can be internally scaled in frequency by 2×, 1×, 0.5×, or 0.25×. This allows a broader range of reference frequency selections while keeping the reference frequency applied to the PFD within an acceptable range.

The ADRF6807 also provides a MUXOUT pin that can be programmed to output a selection of several internal signals. The default mode provides a lock-detect output that allows users to verify when the PLL has locked to the target frequency. In addition, several other internal signals can be routed to the MUXOUT pin as shown in Figure 37.

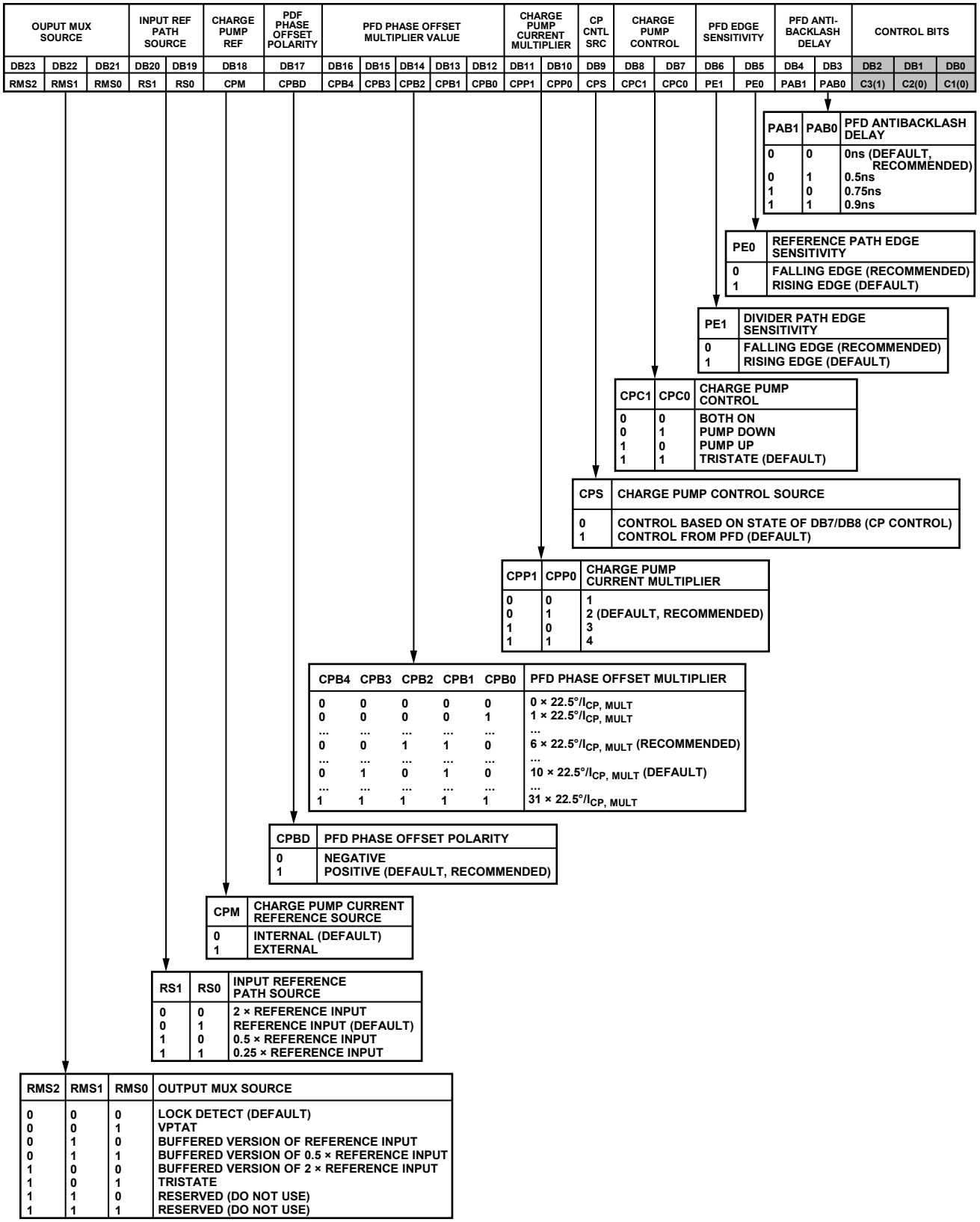



*Figure 37. Charge Pump, PFD, and Reference Path Control Register (R4)*

### *Register 5—LO Path and Demodulator Control*

With R5[DB5] = 1, the ADRF6807 is in a lower power operating mode. The device is still fully functional in this lower power mode, but the mixer performance is shifted (see the Typical Performance Characteristics section for details on performance differences). Setting R5[DB5] = 0 causes the ADRF6807 mixer stage to run at a higher current, thereby achieving a higher IIP3.

Register 5 also controls whether the LOIP and LOIN pins act as an input or output and whether the output driver is enabled as detailed in Figure 38.

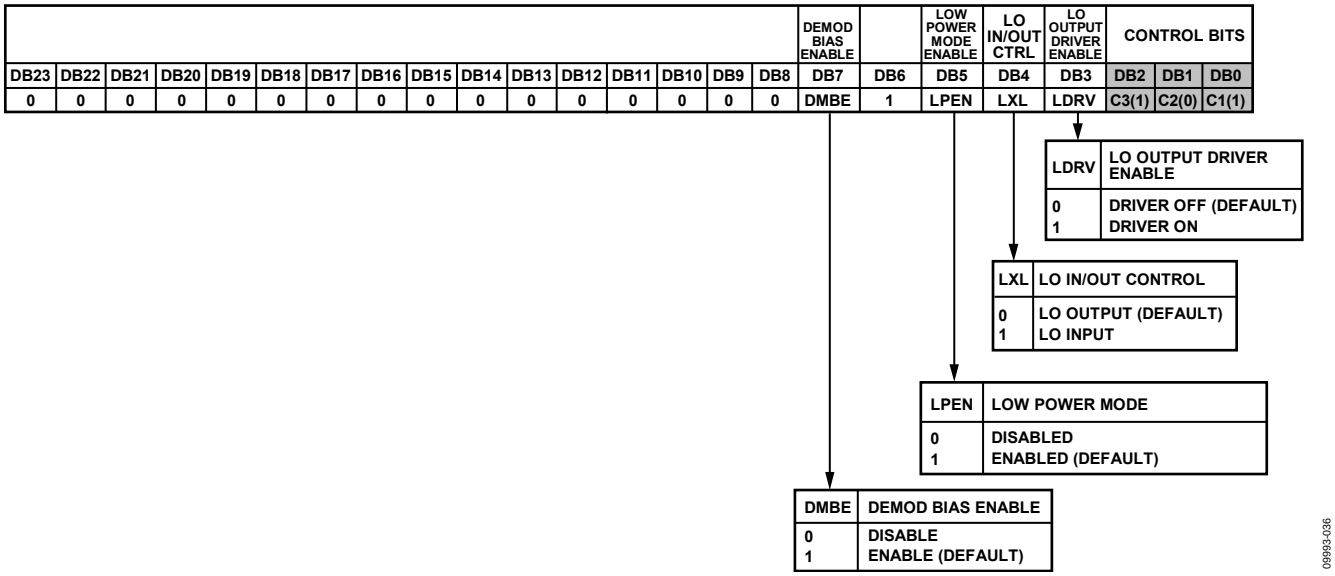



*Figure 38. LO Path and Demodulator Control Register (R5)*

### *Register 6—VCO Control and Enables*

With R6[2:0] set to 110, the VCO control and enables register is programmed as shown in Figure 39.

VCO band selection is normally selected based on an internal BANDCAL calibration; however, the VCO band can be selected directly using Register 6. The VCO BS SRC determines whether the BANDCAL calibration determines the optimum VCO tuning band or if the external SPI interface is used to select the VCO tuning band based on the value of the VCO band select.

The VCO amplitude can be controlled through Register 6. The VCO amplitude setting can be controlled between 0 and 31 decimal, with a default value of 24.

The internal VCO can be disabled using Register 6. The internal VCO LDO can be disabled if an external clean 3.0 V supply is available.

The internal charge pump can be disabled through Register 6. Normally, the charge pump is enabled.

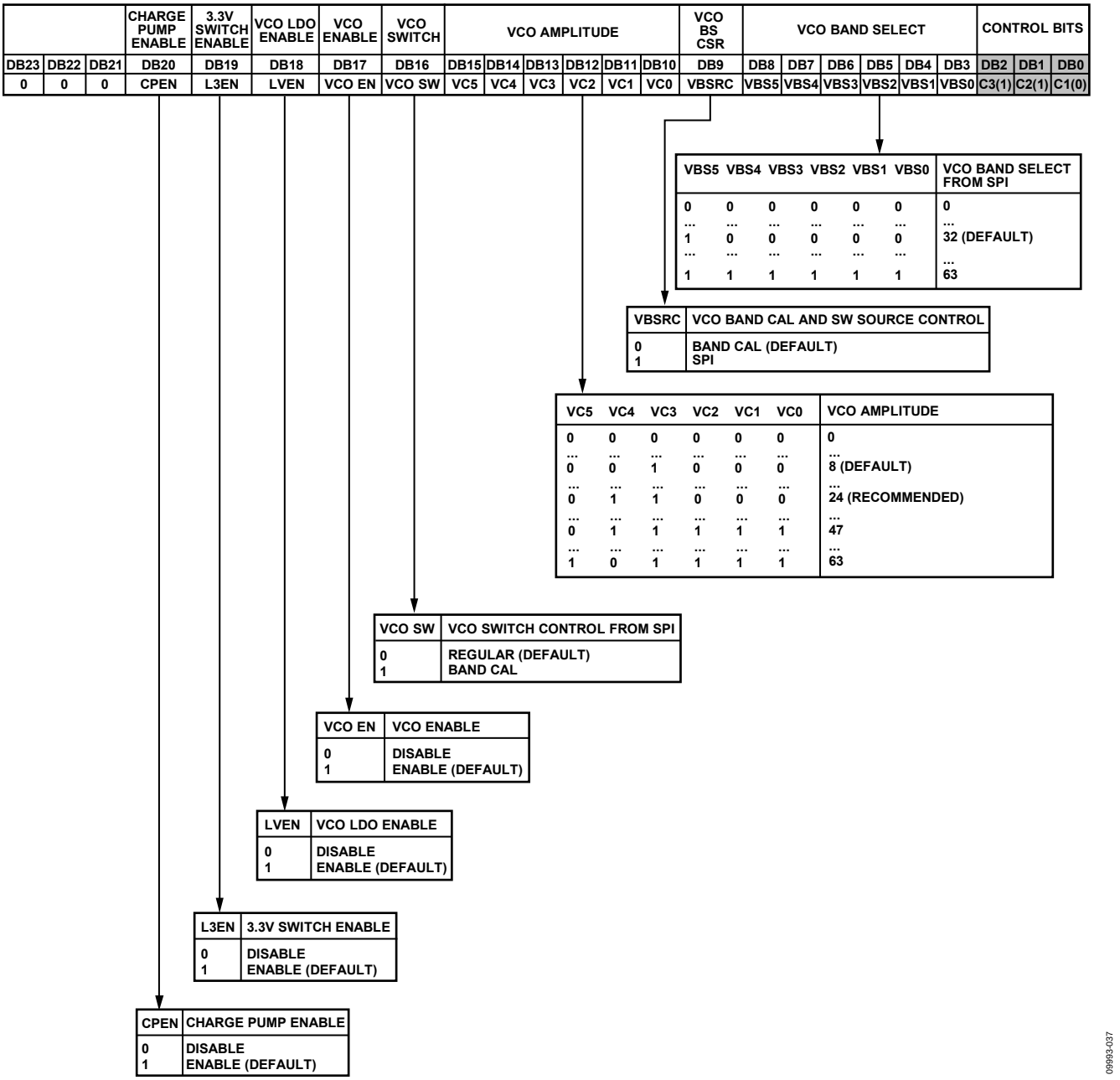



*Figure 39. VCO Control and Enables (R6)*

### *Register 7—LO Divider Control*

Register 7 controls the LO path main divider settings as well as the LO output path divider setting. Table 5 indicates how to program this register to achieve the specified divider mode.

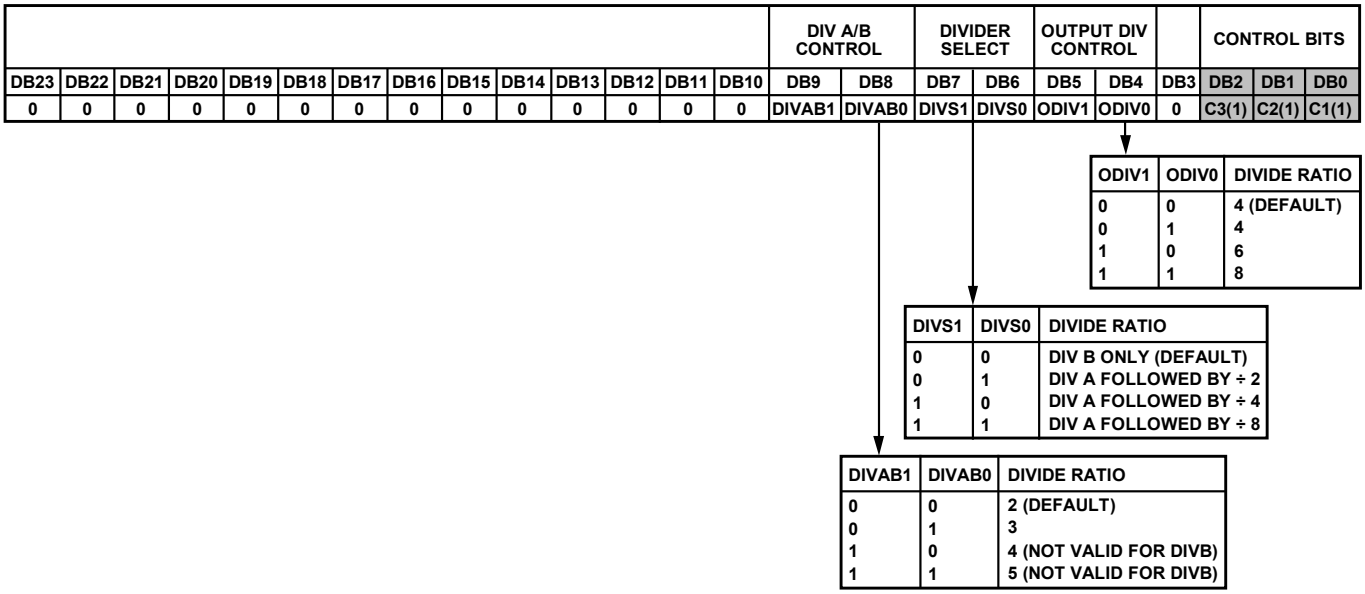



*Figure 40. LO Divider Control Register (R7)*

## LO DIVIDER PROGRAMMING

**Table 5. Main Divider (Only Divide Ratios and Combinations Specified Are Guaranteed)**

| $f_{LO}$ (MHz) | LO Divider Ratio | $f_{VCO}$ (MHz) | Divider Cascade | | | Register 7, DB[9:6] |
|---|---|---|---|---|---|---|
| | | | Divide-by-2 to Divide-by-5 | Divide-by-2, Divide-by-4, or Divide-by-8 | Quadrature Divide-by-2 | |
| 700 to 1050 | 4 | 2800 to 4200 | 2 | Not used | 2 | 00 00 |

**Table 6. Output Divider**

| $f_{LO}$ Output (MHz) | Output Divider Ratio | $f_{VCO}$ (MHz) | Register 7, DB[5:4] |
|---|---|---|---|
| 350 to 525 | 8 | 2800 to 4200 | 11 |
| 466.67 to 700 | 6 | 2800 to 4200 | 10 |
| 700 to 1050 | 4 | 2800 to 4200 | 01 |

## PROGRAMMING EXAMPLE

For example, internal LO frequency = 700 MHz. This can be accomplished with the VCO/PLL frequency at 2800 MHz and an LO divide ratio of 4. The choice of output divider ratio of 8 gives an output frequency of 350 MHz. To achieve this combination, a binary code of 00 00 11 should be programmed into DB[9:4] of Register 7.

# APPLICATIONS INFORMATION

## BASIC CONNECTIONS

The basic circuit connections for a typical ADRF6807 application are shown in Figure 41.

## SUPPLY CONNECTIONS

The ADRF6807 has several supply connections and on-board regulated reference voltages that should be bypassed to ground using low inductance bypass capacitors located in close proximity to the supply and reference pins of the ADRF6807. Specifically, Pin 1, Pin 2, Pin 9, Pin 10, Pin 17, Pin 22, Pin 23, Pin 28, Pin 29, Pin 34, and Pin 40 should be bypassed to ground using individual bypass capacitors. Pin 40 is the decoupling pin for the on-board VCO LDO, and for best phase noise performance, several bypass capacitors ranging from 100 pF to 10 µF may help to improve phase noise performance. For additional details on bypassing the supply nodes, see the evaluation board schematic in Figure 43.

## SYNTHESIZER CONNECTIONS

The ADRF6807 includes an on-board VCO and PLL for LO synthesis. An external reference must be applied for the PLL to operate. A 1 V p-p nominal external reference must be applied to Pin 6 through an ac coupling capacitor. The reference is compared to an internally divided version of the VCO output frequency to create a charge pump error current to control and lock the VCO. The charge pump output current is filtered and converted to a control voltage through the external loop filter that is then applied to the VTUNE pin (Pin 39). ADIsimPLL™ can be a helpful tool when designing the external charge pump loop filter. The typical Kv of the VCO, the charge pump output current magnitude, and PFD frequency should all be considered when designing the loop filter. The charge pump current magnitude can be set internally or with an external RSET resistor connected to Pin 5 and ground, along with the internal digital settings applied to the PLL (see the Register 4—Charge Pump, PFD, and Reference Path Control section for more details).

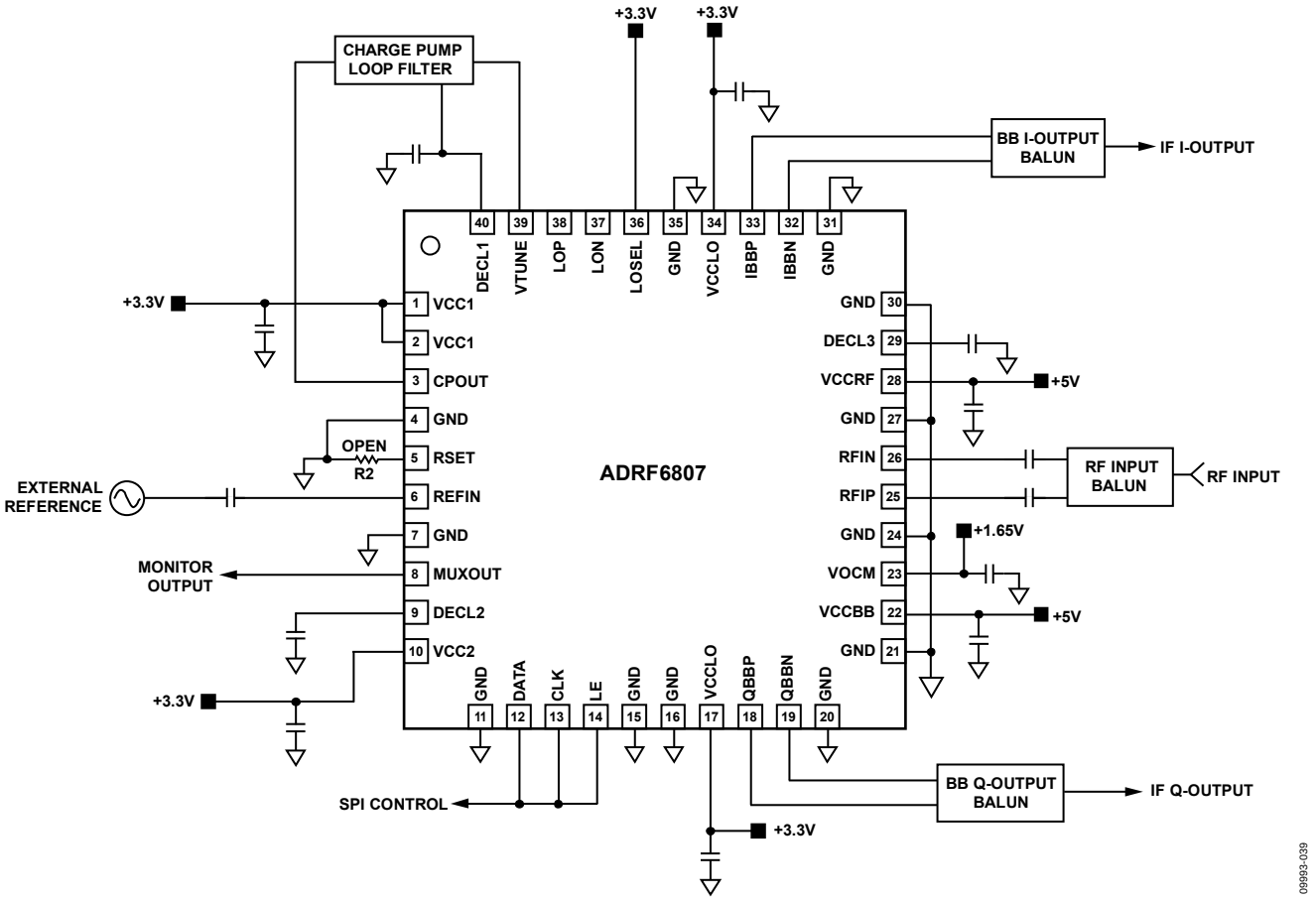



*Figure 41. Basic Connections*

## I/Q OUTPUT CONNECTIONS

The ADRF6807 has I and Q baseband outputs. Each output stage consists of emitter follower output transistors with a low differential impedance of 28 Ω and can source up to 12 mA p-p differentially. A Mini-Circuits TCM9-1+ balun is used to transform a single-ended 50 Ω load impedance into a nominal 450 Ω differential impedance.

## RF INPUT CONNECTIONS

The ADRF6807 uses a Mini-Circuits ADTL2-18+ balun with a 2:1 impedance ratio to transform a single-ended 50 Ω impedance into a differential 100 Ω impedance. Coupling capacitors whose impedance is small compared to 100 Ω at the frequency of operation are used to isolate the dc bias points of the RF input stage.

## CHARGE PUMP/VTUNE CONNECTIONS

The ADRF6807 uses a loop filter to create the VTUNE voltage for the internal VCO. The loop filter in its simplest form is an integrating capacitor. It converts the current mode error signal coming out of the CPOUT pin into a voltage to control the VCO via the VTUNE voltage. The stock filter on the evaluation board has a bandwidth of 67 kHz. The loop filter contains five components, three capacitors, and two resistors. Changing the values of these components changes the bandwidth of the loop filter.

## LO SELECT INTERFACE

The ADRF6807 has the option of either monitoring a scaled version of the internally generated LO (LOSEL pin driven high at 3.3 V) or providing an external LO source (LOSEL pin driven low to ground, the LDRV bit in Register 5 set low, and the LXL bit in Register 5 set high). See the Pin Configuration and Function Descriptions section for full operation details.

## EXTERNAL LO INTERFACE

The ADRF6807 provides the option to use an external signal source for the LO into the IQ demodulating mixer core. It is important to note that the applied LO signal is divided down by a divider (programmable to between 4 and 80) prior to the actual IQ demodulating mixer core. The divider is determined by the register settings in the LO path and mixer control register (see the Register 5—LO Path and Demodulator Control section). The LO input pins (Pin 37 and Pin 38) present a broadband differential 50 Ω input impedance. The LOP and LON input pins must be ac-coupled. This is achieved on the evaluation board via a Mini-Circuits TC1-1-13+ balun with a 1:1 impedance ratio. When not in use, the LOP and LON pins can be left unconnected.

## SETTING THE FREQUENCY OF THE PLL

The frequency of the VCO/PLL, once locked, is governed by the values programmed into the PLL registers, as follows:

$$f_{PLL} = f_{PFD} \times 2 \times (INT + FRAC/MOD)$$

where:
$f_{PLL}$ is the frequency at the VCO when the loop is locked.
$f_{PFD}$ is the frequency at the input of the phase frequency detector.
*INT* is the integer divide ratio programmed into Register 0.
*FRAC* is the fractional value programmed into Register 2.
*MOD* is the modulus divide ratio programmed into Register 1.

The practical lower limit of the reference input frequency is determined by the combination of the desired $f_{PLL}$ and the maximum programmable integer divide ratio of 119 and reference input frequency multiplier of 2. For a maximum $f_{PLL}$ of 4200 MHz,

$$f_{REF} > \sim f_{PLL}/(f_{PFD} \times 2 \times 2), \text{ or } 8.8 \text{ MHz}$$

A lock detect signal is available as one of the selectable outputs through the MUXOUT pin, with logic high signifying that the loop is locked.

## REGISTER PROGRAMMING

Because Register 6 controls the powering of the VCO and charge pump, it must be programmed once before programming the PLL frequency (Register 0, Register 1, and Register 2).

The registers should be programmed starting with the highest register (Register 7) first and then sequentially down to Register 0 last. When Register 0, Register 1, or Register 2 is programmed, an internal VCO calibration is initiated that must execute when the other registers are set. Therefore, the order must be Register 7, Register 6, Register 5, Register 4, Register 3, Register 2, Register 1, and then Register 0. Whenever Register 0, Register 1, or Register 2 is written to, it initializes the VCO calibration (even if the value in these registers does not change). After the device has been powered up and the registers configured for the desired mode of operation, only Register 0, Register 1, or Register 2 must be programmed to change the LO frequency.

If none of the register values are changing from their defaults, there is no need to program them.

## EVM MEASUREMENTS

EVM is a measure used to quantify the performance of a digital radio transmitter or receiver. A signal received by a receiver has all constellation points at their ideal locations; however, various imperfections in the implementation (such as magnitude imbalance, noise floor, and phase imbalance) cause the actual constellation points to deviate from their ideal locations.

In general, a demodulator exhibits three distinct EVM limitations vs. received input signal power. As signal power increases, the distortion components increase. At large signal levels, where the distortion components due to the harmonic nonlinearities in the device are falling in-band, EVM degrades as signal levels increase. At medium signal levels, where the demodulator behaves in a linear manner and the signal is well above any notable noise contributions, the EVM has a tendency to reach an optimal level determined dominantly by either quadrature accuracy and I/Q gain match of the demodulator or the precision of the test equipment. As signal levels decrease, such that the noise is a major contribution, the EVM performance vs. the signal level exhibits a decibel-for-decibel degradation with decreasing signal level. At lower signal levels, where noise proves to be the dominant limitation, the decibel EVM proves to be directly proportional to the SNR.

The basic test setup for testing the EVM of the ADRF6807 consisted of an Agilent E4438C, which was used as a signal source. The 900 MHz modulated signal was driven single ended into the RFIN SMA connector of the ADRF6807 evaluation board. The IQ baseband outputs were taken differentially into a pair of AD8130 difference amplifiers to convert the differential signals to single ended. The output impedance that the ADRF6807 drove was set to 450 Ω differential. The single-ended I and Q signals were then sampled by an Agilent DSO7104B oscilloscope. The Agilent 89400 VSA software was used to calculate the EVM of the signal. The signal source that was used for the reference input was a Wenzel 100 MHz quarts oscillator set at an amplitude of 1 V p-p. The reference path was set to a divide-by-four, thus making the PFD frequency 25 MHz.

Figure 42 shows the excellent EVM of the ADRF6807 being better than −40 dB over an RF input range of about 40 dB for a 4 QAM modulated signal, at a 5 MHz symbol rate and at a 0 Hz IF. The roll-off, or alpha, of the pulse shaping filter was set to 0.35. The reported RF input power is the power integrated across the bandwidth of

$$BW = (1 + \alpha) \times (Symbol\ Rate)$$

EVM was tested for both power modes: low power mode disabled (LPEN = 0) and low power mode enabled (LPEN = 1). When the low power mode is enabled, the EVM is better at lower RF input signal levels due to less noise while running in the low power mode.

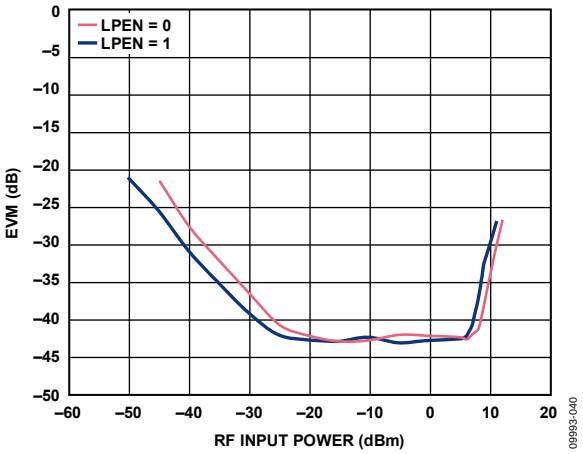



*Figure 42. EVM Measurements at 900 MHz 4 QAM, Symbol Rate = 5 MHz, Baseband Frequency = 0 Hz IF*

# EVALUATION BOARD LAYOUT AND THERMAL GROUNDING

An evaluation board is available for testing the ADRF6807. The evaluation board schematic is shown in Figure 43.

Table 7 provides the component values and suggestions for modifying the component values for the various modes of operation.

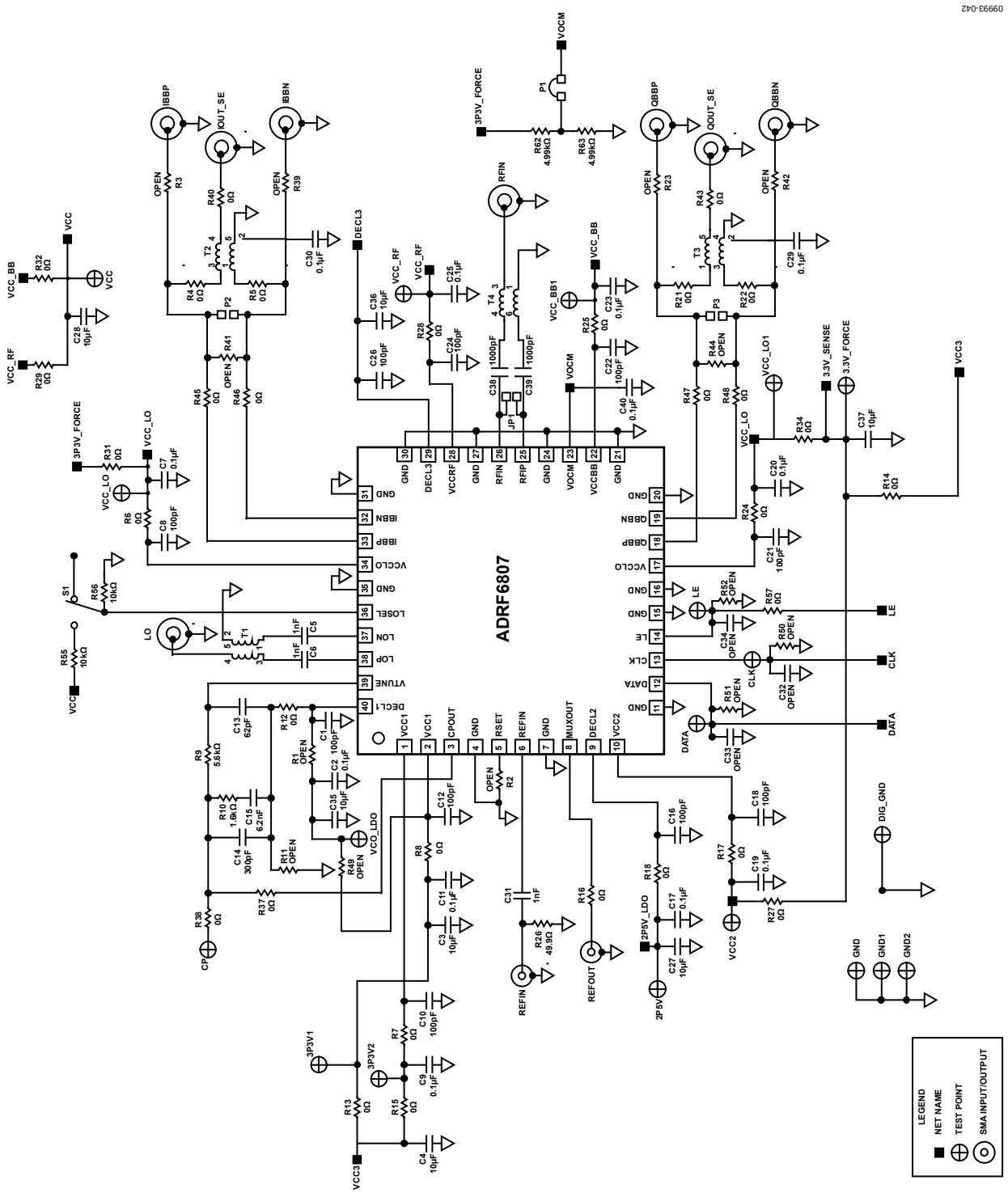



*Figure 43. Evaluation Board Schematic*

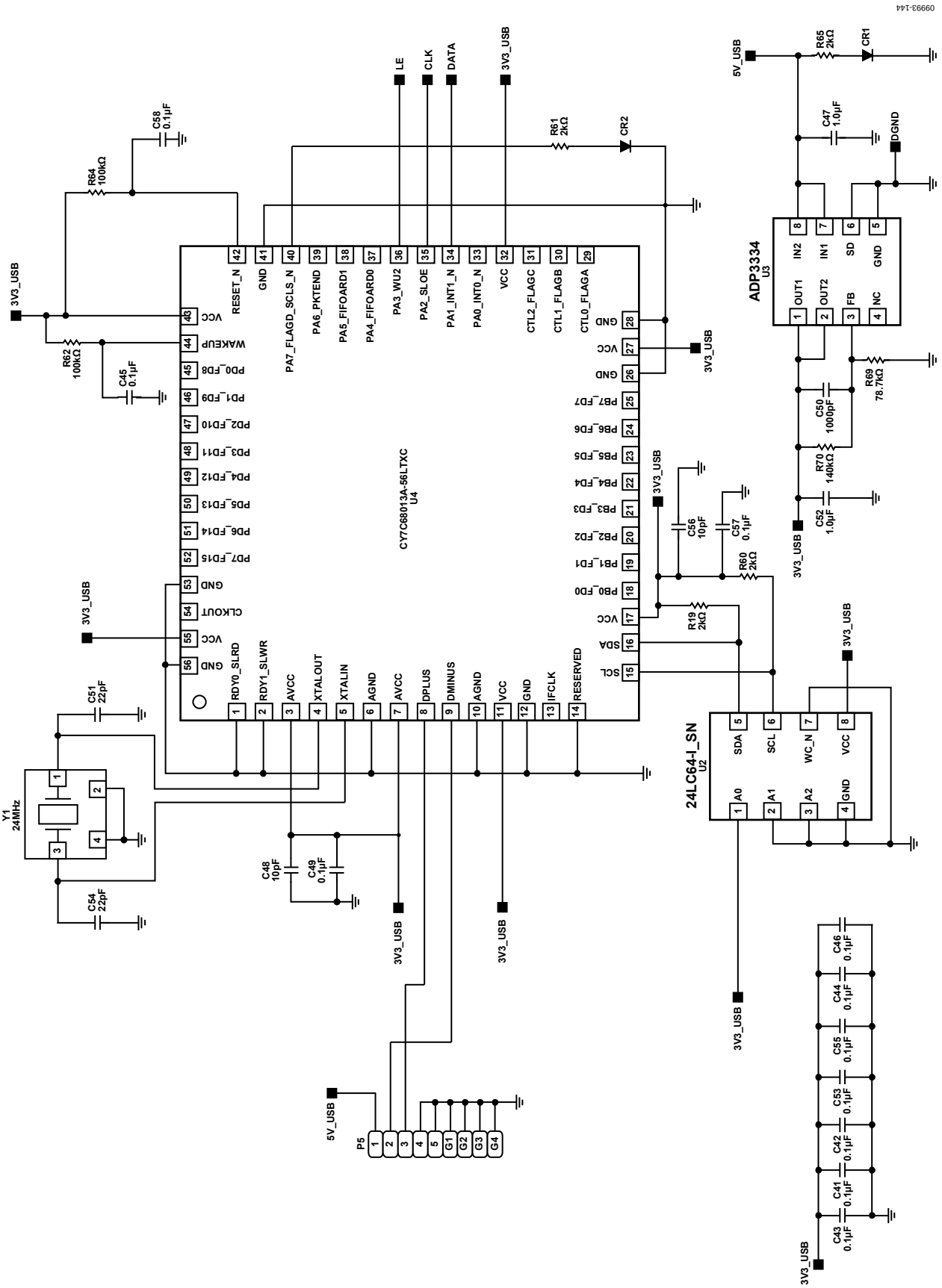



*Figure 44. Evaluation Board USB Section Schematic*

The package for the ADRF6807 features an exposed paddle on the underside that should be well soldered to an exposed opening in the solder mask on the evaluation board. Figure 45 illustrates the dimensions used in the layout of the ADRF6807 footprint on the ADRF6807 evaluation board (1 mil = 0.0254 mm).

Note the use of nine via holes on the exposed paddle. These ground vias should be connected to all other ground layers on the evaluation board to maximize heat dissipation from the device package. Under these conditions, the thermal impedance of the ADRF6807 was measured to be approximately 30°C/W in still air.

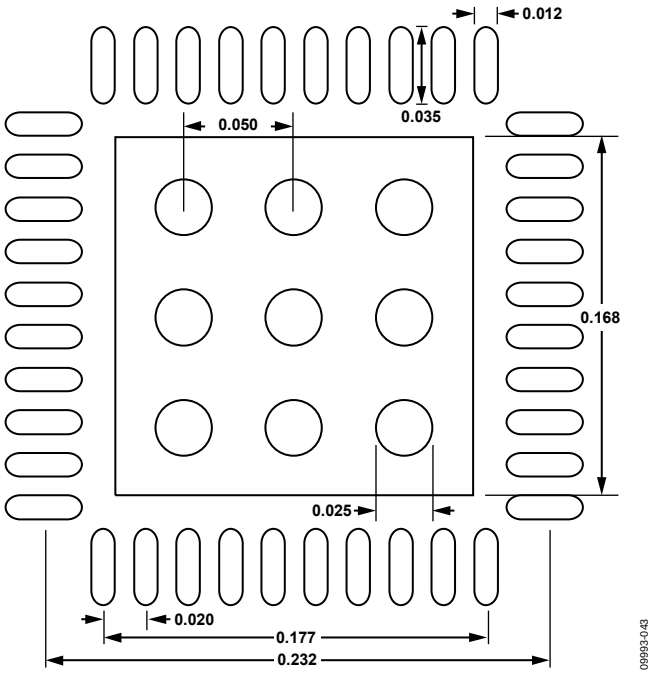



Figure 45. Evaluation Board Layout Dimensions for the ADRF6807 Package

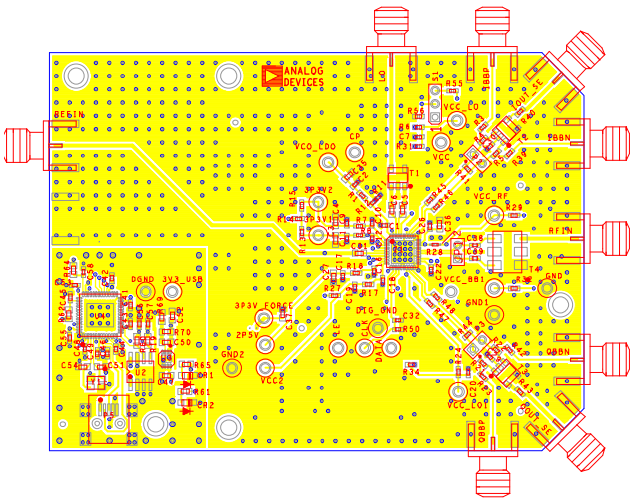



Figure 46. ADRF6807 Evaluation Board Top Layer

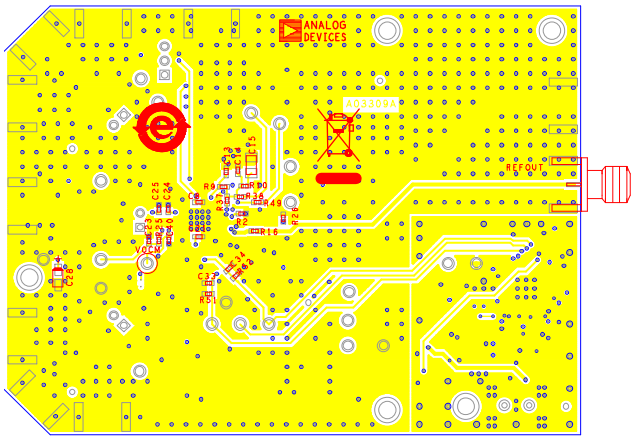



Figure 47. ADRF6807 Evaluation Board Bottom Layer

**Table 7. Evaluation Board Configuration Options**

| Component | Function | Default Condition |
|---|---|---|
| VCC, VCC2, VCC_LDO, VCC_LO, VCC_LO1, VCC_RF, VCC_BB1, 3P3V1, 3P3V2, 3P3V_FORCE, 2P5V, CLK, DATA, LE, CP, DIG_GND, GND, GND1, GND2 | Power supply, ground and other test points. Connect a 5 V supply to VCC. Connect a 3.3 V supply to 3P3V_FORCE. | VCC, VCC2, VCC_LO, VCC_RF, VCC_BB1, VCC_LO1, VCO_LDO, 3P3V1, 3P3V2, 2P5V = Components Corporation TP-104-01-02, CP, LE, CLK, DATA, 3P3V_FORCE = Components Corporation TP-104-01-06, GND, GND1, GND2, DIG_GND = Components Corporation TP-104-01-00 |
| R1, R6, R7, R8, R13, R14, R15, R17, R18, R24, R25, R27, R28, R29, R31, R32, R34, R36, R49 | Power supply decoupling. Shorts or power supply decoupling resistors. | R1, R6, R7, R8 = 0 Ω (0402),<br>R13, R14, R15, R17 = 0 Ω (0402),<br>R18, R24, R25, R27 = 0 Ω (0402),<br>R28, R29, R31, R32 = 0 Ω (0402),<br>R34, R36 = 0 Ω (0402),<br>R49 = open (0402) |
| C1, C2, C3, C4, C7, C8, C9, C10, C11, C12, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C35, C36, C37, C40 | The capacitors provide the required decoupling of the supply-related pins. | C1, C8, C10, C12 = 100 pF (0402),<br>C16, C18, C21, C22 = 100 pF (0402),<br>C24, C26 = 100 pF (0402),<br>C2, C7, C9, C11 = 0.1 µF (0402),<br>C17, C19, C20, C23 = 0.1 µF (0402),<br>C25, C40 = 0.1 µF (0402),<br>C3, C4, C27, C35 = 10 µF (0603),<br>C36, C37 = 10 µF (0603),<br>C28 = 10 µF (3216) |
| T1, C5, C6 | External LO path. The T1 transformer provides single-ended-to-differential conversion. C5 and C6 provide the necessary ac coupling. | C5, C6 = 1 nF (0603),<br>T1 = TC1-1-13+ Mini-Circuits |
| R16, R26, R58, C31 | REFIN input path. R26 provides a broadband 50 Ω termination followed by C31, which provides the ac coupling into REFIN. R16 provides an external connectivity to the MUXOUT feature described in Register 4. R58 provides option for connectivity to the P1-6 line of a 9-pin D-sub connector for dc measurements. | R26 = 49.9 Ω (0402),<br>R16 = 0 Ω (0402),<br>R58 = open (0402),<br>C31 = 1 nF (0603) |
| R2, R9, R10, R11, R12, R37, R38, R59, C14, C15, C13 | Loop filter component options. A variety of loop filter topologies is supported using component placements, C13, C14, C15, R9, and R10. R38 and R59 provide connectivity options to numerous test points for engineering evaluation purposes. R2 provides resistor programmability of the charge pump current (see the Register 4—Charge Pump, PFD, and Reference Path Control section). R37 connects the charge pump output to the loop filter. R12 references the loop filter to the VCO_LDO. | R12, R37, R38 = 0 Ω (0402),<br>R59 = open (0402),<br>R9 = 5.6 kΩ (0402),<br>R10 = 1.6 kΩ (0402),<br>R2, R11 = open (0402),<br>C13 = 62 pF (0402),<br>C14 = 300 pF (0402),<br>C15 = 6.2 nF (1206) |
| R3, R4, R5, R21, R22, R23, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, C29, C30, T2, T3, P2, P3 | IF I/Q output paths. The T2 and T3 baluns provide a 9:1 impedance transformation; therefore, with a 50 Ω load on the single-ended IOUT/QOUT side, the center tap side of the balun presents a differential 450 Ω to the ADRF6807. The center taps of the baluns are ac grounded through C29 and C30. The baluns create a differential-to-single-ended conversion for ease of testing and use, but an option to have straight differential outputs is achieved by populating R3, R39, R23, and R42 with 0 Ω resistors and removing R4, R5, R21, and R22. P2 and P3 are differential measurement test points (not to be used as jumpers). | R4, R5, R21, R22, = 0 Ω (0402),<br>R40, R43, R45, R46 = 0 Ω (0402),<br>R47, R48 = 0 Ω (0402),<br>R3, R23, R39, R41, R42, R44 = open (0402),<br>C29, C30, = 0.1 µF (0402),<br>T2, T3 = TCM9-1+ Mini-Circuits,<br>P2, P3 = Samtec SSW-102-01-G-S |
| C38, C39, T4 | RF input interface. T4 provides the single-ended-to-differential conversion required to drive RFIP and RFIN. T4 provides a 2:1 impedance transformation. A single-ended 50 Ω load on the RFIN SMA connector transforms to a differential 100 Ω presented across the RFIP (Pin 25) and RFIN (Pin 26) pins. C38 and C39 are ac coupling capacitors. | C38, C39 = 1000 pF (0402),<br>T4 = ADTL2-18+ Mini-Circuits |

| Component | Function | Default Condition |
|---|---|---|
| R50, R51, R52, C32, C33, C34 | Serial port interface. Optional RC filters can be installed on the CLK, DATA, and LE lines to filter the PC signals through R50 to R52 and C32 to C34. CLK, DATA, and LE signals can be observed via test points for debug purposes. | R50, R51, R52 = open (0402),<br>C32, C33, C34 = open (0402) |
| R33, R55, R56, S1 | LO select interface. The LOSEL pin, in combination with the LDRV and LXL bits in Register 5, controls whether the LOP and LON pins operate as inputs or outputs. A detailed description of how the LOSEL pin, LDRV bit, and the LXL bit work together to control the LOP and LON pins is found in Table 4 under the LOSEL pin description. Using the S1 switch, the user can pull LOSEL to a logic high ($V_{CC}$/2) or a logic low (ground). Resistors R55 and R56 form a resistor divider to provide a logic high of $V_{CC}$/2. LO select can also be controlled through Pin 9 of J1. The 0 Ω jumper, R33, must be installed to control LOSEL via J1. | R33 = 0 Ω (0402),<br>R55, R56 = 10 kΩ (0402),<br>S1 = Samtec TSW-103-08-G-S |
| J1, P1, R62, R63 | Engineering test points and external control. J1 is a 10-pin connector connected to various important points on the evaluation board that the user can measure or force voltages upon. R62 and R63 form a voltage divider to force a voltage of 1.65 V on VOCM. Note that Jumper P5 must be connected to drive VOCM with the resistor divider. | R62 = R63 = 4.99 kΩ (0402),<br>P1 = Samtec SSW-102-01-G-S,<br>J1 = Molex Connector Corp. 10-89-7102 |
| U2, U3, U4, P5 | Cypress microcontroller, EEPROM and LDO. | U2 = Microchip MICRO24LC64<br>U3 = Analog Devices ADP3334ACPZ<br>U4 = Cypress Semiconductor CY7C68013A-56LTXC<br>P5 = Mini USB connector |
| C41, C42, C43, C44, C46, C53, C55 | 3.3 V supply decoupling. Several capacitors are used for decoupling on the 3.3 V supply. | C41, C42, C43, C44, C46, C53, C55 = 0.1 µF (0402) |
| C48, C49, C45, C56, C57, C58, R19, R60, R61, R62, R64, CR2 | Cypress and EEPROM components. | C48, C56 = 10 pF (0402)<br>C45, C49, C57, C58 = 0.1 µF (0402)<br>R19, R60, R61 = 2 kΩ (0402)<br>R62, R64 = 100 kΩ (0402)<br>CR2 = ROHM SML-21OMTT86 |
| C47, C50, C52, R65, R69, R70, CR1 | LDO components. | C47, C52 = 1 µF (0402)<br>C50 = 1000 pF (0402)<br>R65 = 2 kΩ (0402)<br>R69 = 78.7 kΩ (0402)<br>R70 = 140 kΩ (0402)<br>CR1 = ROHM SML-21OMTT86 |
| Y1, C51, C54 | Crystal oscillator and components. 24 MHz crystal oscillator. | Y1 = NDK NX3225SA-24 MHz<br>C51, C54 = 22 pF (0402) |

## ADRF6807 SOFTWARE

The ADRF6807 evaluation board can be controlled from PCs using a USB adapter board, which is also available from Analog Devices, Inc. The USB adapter evaluation documentation and ordering information can be found on the EVAL-ADF4XXXZ-USB product page. The basic user interfaces are shown in Figure 48 and Figure 49.

The software allows the user to configure the ADRF6807 for various modes of operation. The internal synthesizer is controlled by clicking any of the numeric values listed in **RF Section**.

Attempting to program **Ref Input Frequency**, **PFD Frequency**, **VCO Frequency (2×LO)**, **LO Frequency**, or other values in **RF Section** launches the **Synth Form** window shown in Figure 49. Using **Synth Form**, the user can specify values for **Local Oscillator Frequency (MHz)** and **External Reference Frequency (MHz)**. The user can also enable the LO output buffer and divider options from this menu. After setting the desired values, it is important to click **Upload all registers** for the new setting to take effect.

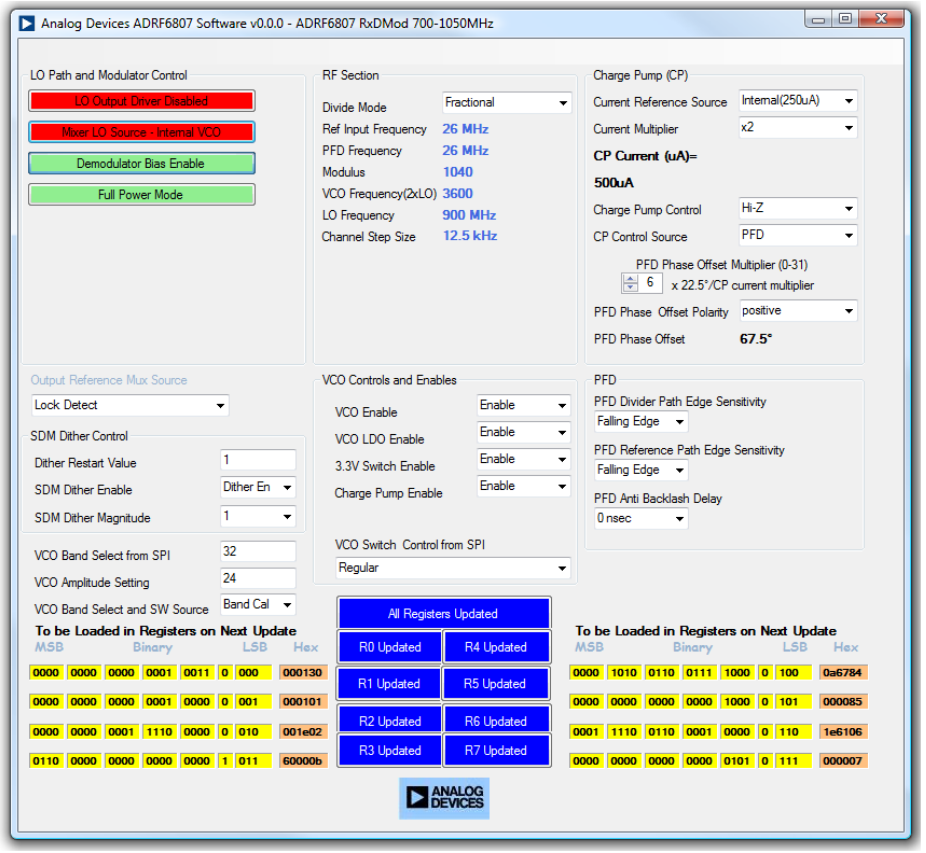



*Figure 48. Evaluation Board Software Main Window*

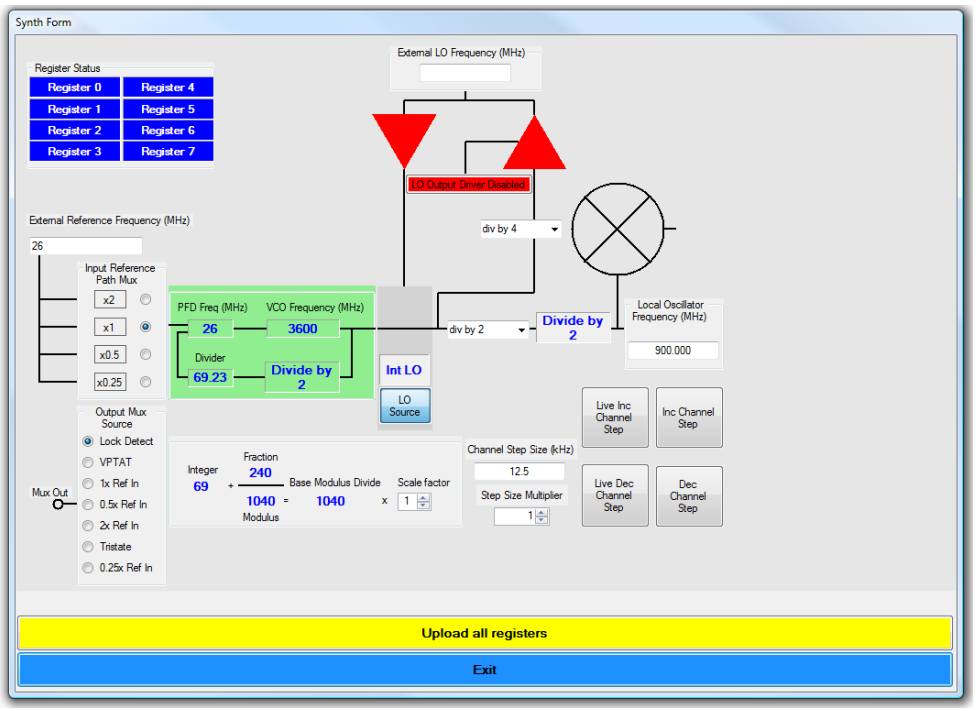



*Figure 49. Evaluation Board Software Synth Form Window*

# CHARACTERIZATION SETUPS

Figure 50 to Figure 52 show the general characterization bench setups used extensively for the ADRF6807. The setup shown in Figure 50 was used to perform the bulk of the testing. An automated Agilent VEE program was used to control the equipment over the IEEE bus. This setup was used to measure gain, input P1dB, output P1dB, input IP2, input IP3, IQ gain mismatch, IQ quadrature accuracy, and supply current. The evaluation board was used to perform the characterization with a Mini-Circuits TCM9-1+ balun on each of the I and Q outputs. When using the TCM9-1+ balun below 5 MHz (the specified 1 dB low frequency corner of the balun), distortion performance degrades; however, this is not the ADRF6807 degrading, merely the low frequency corner of the balun introducing distortion effects. Through this balun, the 9-to-1 impedance transformation effectively presented a 450 Ω differential load at each of the I and Q channels. The use of the broadband Mini-Circuits ADTL2-18+ balun on the input provided a differential balanced RF input. The losses of both the input and output baluns were de-embedded from all measurements.

To perform phase noise and reference spur measurements, the setup shown in Figure 52 was used. Phase noise was measured at the baseband output (I or Q) at a baseband carrier frequency of 50 MHz. The baseband carrier of 50 MHz was chosen to allow phase noise measurements to be taken at frequencies of up to 20 MHz offset from the carrier. The noise figure was measured using the setup shown in Figure 51 at a baseband frequency of 10 MHz.

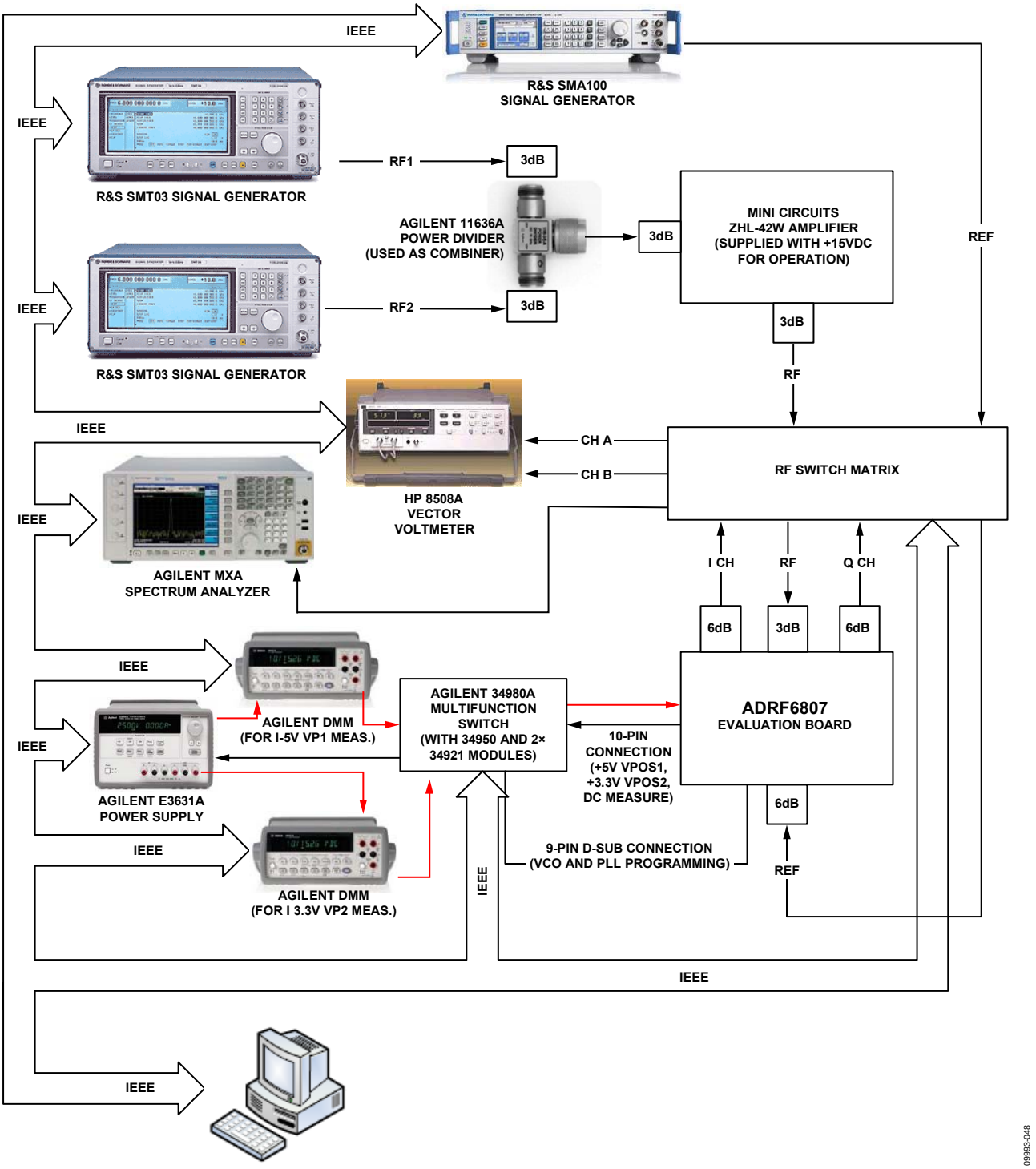



*Figure 50. General Characterization Setup*

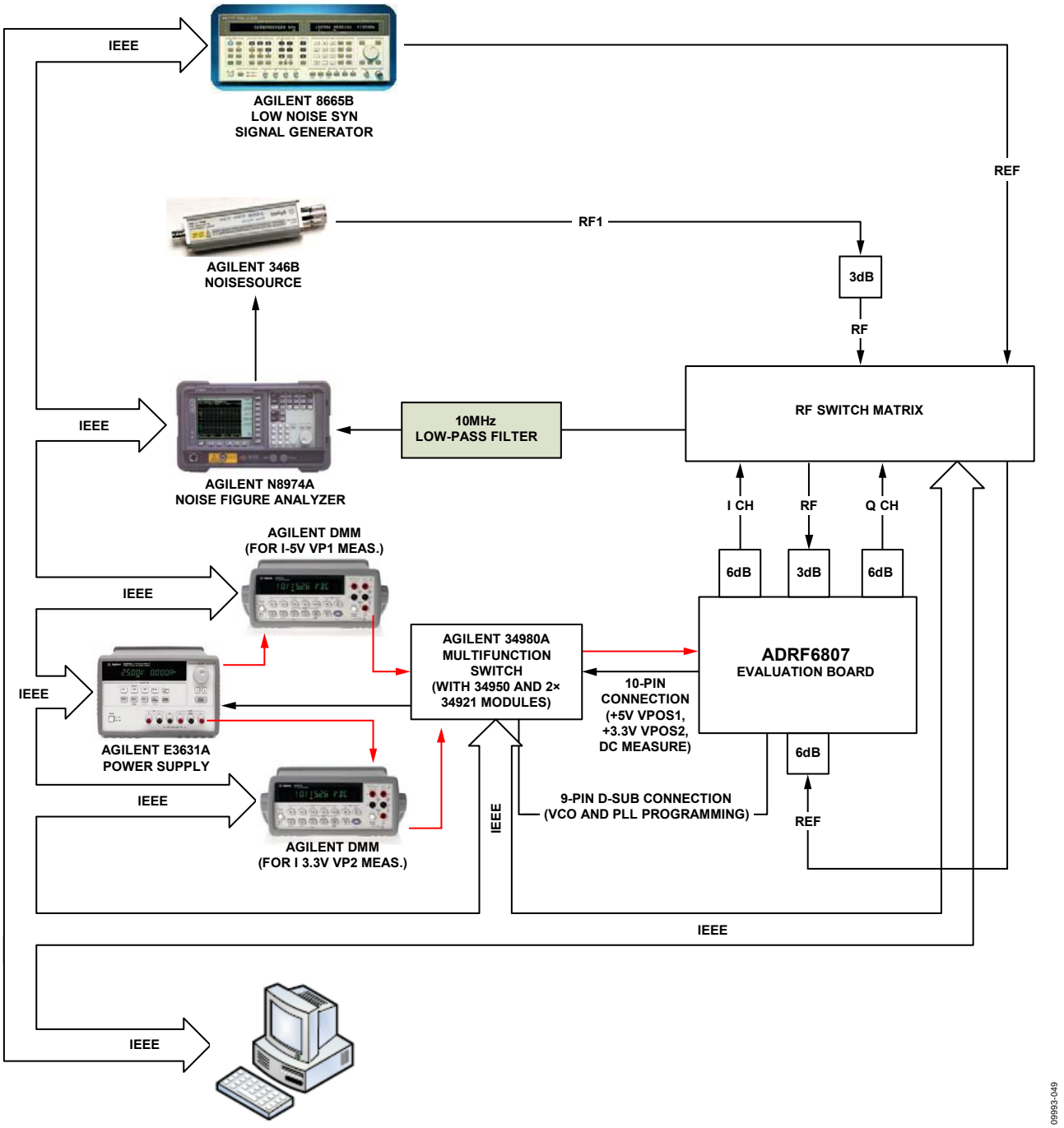



*Figure 51. Noise Figure Characterization Setup*

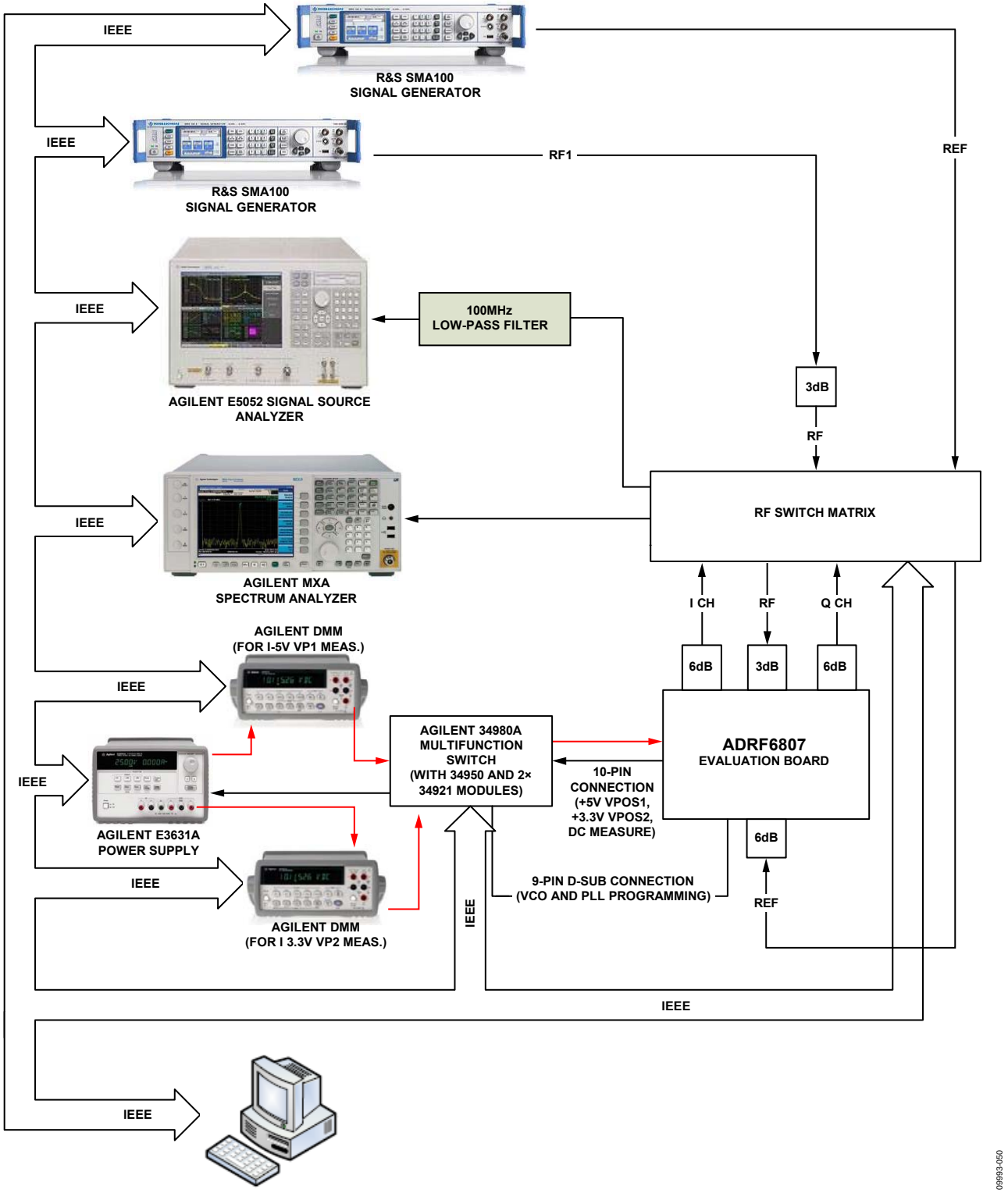



*Figure 52. Phase Noise Characterization Setup*

# OUTLINE DIMENSIONS

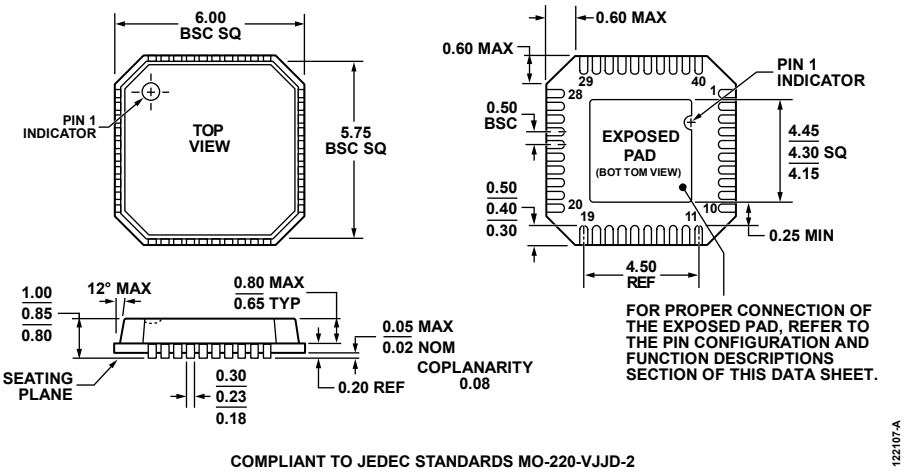



*Figure 53. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*6 mm × 6 mm Body, Very Thin Quad*
*(CP-40-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Ordering Quantity |
|---|---|---|---|---|
| ADRF6807ACPZ-R7 | −40°C to +85°C | 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ] | CP-40-4 | 750 |
| ADRF6807-EVALZ | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.


D09993-0-2/12(B)