MAXIM

Low-Voltage, Single-Supply Analog Multiplexers/Switches

MAX4524L/MAX4525L

_____General Description

The MAX4524L/MAX4525L are low-voltage, single-supply CMOS analog switches configured as a 4-channel multiplexer/demultiplexer (MAX4524L) and a double-pole/double-throw (DPDT) switch (MAX4525L). The MAX4524L/MAX4525L have an inhibit input to simultaneously open all switches.

These devices operate from a single supply of +2V to +12V. They are optimized for operation with a +12V supply. The on-resistance is 100Ω with a +12V supply. Each switch can handle Rail-to-Rail analog signals. Off-leakage current measures only 2nA at +25°C. All digital inputs have 0.8V to 2.0V logic thresholds to ensure TTL/CMOS-logic compatibility when using a +12V supply.

_____Features

♦ **+3V Logic-Compatible Inputs
  (V_{IH} = 2.0V, V_{IL} = 0.8V)**

♦ **+2V to +12V Supply Operation**

♦ **100Ω On-Resistance with +12V Supply**

♦ **Guaranteed 10Ω On-Resistance Match at +12V**

♦ **Guaranteed 2nA Maximum Off-Leakage at +12V**

♦ **TTL/CMOS-Logic Compatible**

♦ **Tiny 10-Pin TDFN (3mm × 3mm) and 10-Pin µMAX
  Packages**

_____Applications

Audio and Video Signal Routing

Data-Acquisition Systems
  Communications Circuits
  Automotive
  DSL Modems

_____Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4524LEUB	-40°C to +85°C	10 µMAX	—
MAX4524LETB	-40°C to +85°C	10 TDFN-EP* (3mm x 3mm)	AAL
MAX4525LEUB	-40°C to +85°C	10 µMAX	—
MAX4525LETB	-40°C to +85°C	10 TDFN-EP* (3mm x 3mm)	AAM

*EP = Exposed pad.

_____Pin Configurations/Functional Diagrams/Truth Tables

MAX4524L

INH	ADDB	ADDA	ON SWITCH
1	X	X	NONE
0	0	0	COM-NO0
0	0	1	COM-NO1
0	1	0	COM-NO2
0	1	1	COM-NO3

MAX4525L

INH	ADDB	ON SWITCH
1	X	NONE
0	0	COMA-NCA, COMB-NCB
0	1	COMA-NOA, COMB-NOB

MAXIM _____ **Maxim Integrated Products   1**

Low-Voltage, Single-Supply Analog Multiplexers/Switches

ABSOLUTE MAXIMUM RATINGS

(All Voltages Referenced to GND, Unless Otherwise Noted.)

V+ ....-0.3V to +13V
Voltage at Any Pin (Note 1) ....-0.3V to (V+ + 0.3V)
Continuous Current into Any Terminal ....±20mA
Peak Current NO_, NC_ or COM_
  (pulsed at 1ms, 10% duty cycle) ....±40mA
ESD per Method 3015.7 ....>2000V

Continuous Power Dissipation (T$_A$ = +70°C)
  10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
  10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range
  MAX452_E_ _...-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature..+150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: Voltages exceeding V+ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +12V Supply

(V+ = 12V ±5%, GND = 0V, V$_{IH}$ = 2.0V, V$_{IL}$ = 0.8V, T$_A$ = T$_{MIN}$ to T$_{MAX}$, unless otherwise noted. Typical values are at T$_A$ = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V$_{COM}$, V$_{NO\_\_}$			-40°C to +85°C	0		V+	V
COM-NO/NC On-Resistance	R$_{ON}$	V+ = 11.4V, I$_{COM}$ = 1mA, V$_{COM}$ = 10V		+25°C		45	80	Ω
				-40°C to +85°C			100	
COM-NO/NC On-Resistance Match Between Channels	ΔR$_{ON}$	V+ = 11.4V, I$_{COM}$ = 1mA, V$_{COM}$ = 10V (Note 4)		+25°C		2	10	Ω
				-40°C to +85°C			15	
COM-NO/NC On-Resistance Flatness	R$_{FLAT}$	V+ = 11.4V, I$_{COM}$ = 1mA, V$_{COM}$ = 1.5V, 6.0V, 10V (Note 5)		+25°C		5	12	Ω
NO/NC Off-Leakage	I$_{NO(OFF)}$ I$_{NC(OFF)}$	V+ = 12.6V, V$_{NO}$ = 1.0V, 10V, V$_{COM}$ = 10V, 1.0V (Note 6)		+25°C	-2		+2	nA
				-40°C to +85°C	-10		+10	
COM Off-Leakage	I$_{COM(OFF)}$	V+ = 12.6V, V$_{NO}$ = 1V, 10V; V$_{COM}$ = 10V, 1V (Note 6)	MAX4524L	+25°C	-2		+2	nA
				-40°C to +85°C	-50		+50	
			MAX4525L	+25°C	-2		+2	
				-40°C to +85°C	-25		+25	
COM ON-Leakage	I$_{COM(ON)}$	V+ = 12.6V, V$_{COM}$ = 10V, 1V (Note 6)	MAX4524L	+25°C	-2		+2	nA
				-40°C to +85°C	-50		+50	
			MAX4525L	+25°C	-2		+2	
				-40°C to +85°C	-25		+25	
DIGITAL I/O (INH, ADD_)								
Logic-Input Threshold High	V$_{IH}$			-40°C to +85°C		1.5	2.0	V
Logic-Input Threshold Low	V$_{IL}$			-40°C to +85°C	0.8	1.5		V
Input Current High	I$_{IH}$	V$_{ADD\_}$ = V$_{INH}$ = 2.0V		+25°C	-1		+1	µA
Input Current Low	I$_{IL}$	V$_{ADD\_}$ = V$_{INH}$ = 0.8V		+25°C	-1		+1	µA

/MAXIM

ELECTRICAL CHARACTERISTICS—Single +12V Supply (continued)

(V+ = 12V ±5%, GND = 0V, V_{IH} = 2.0V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Inhibit Turn-On Time	t_{ON}	$V_{NO\_}$= 10V, R_L = 300Ω, C_L = 35pF, Figure 1		+25°C		90	150	ns
				-40°C to +85°C			200	
Inhibit Turn-Off Time	t_{OFF}	$V_{NO\_}$= 10V, R_L = 300Ω, C_L = 35pF, Figure 1		+25°C		40	120	ns
				-40°C to +85°C			180	
Address Transition Time	t_{TRANS}	$V_{NO\_}$= 10V, R_L = 300Ω, C_L = 35pF, Figure 2		+25°C		90	150	ns
				-40°C to +85°C			200	
Break-Before-Make Time	t_{BBM}	V_{NO} = 10V, R_L = 300Ω, C_L = 35pF, Figure 3		+25°C		20		ns
Charge Injection	Q	C = 1nF, Figure 4 (Note 7)		+25°C		0.8		pC
NO/NC Off-Capacitance	$C_{NO(OFF)}$	$V_{NO\_}$ = 0V, f = 1MHz, Figure 5		+25°C		4		pF
COM Off-Capacitance	$C_{COM(OFF)}$	$V_{NO\_}$ = 0V, f = 1MHz, Figure 5	MAX4524L	+25°C		14		pF
			MAX4525L	+25°C		6		
COM On-Capacitance	$C_{COM(ON)}$	$V_{NO\_}$ = 0V, f = 1MHz, Figure 5	MAX4524L	+25°C		20		pF
			MAX4525L	+25°C		12		
Off-Isolation	V_{ISO}	R_L = 50Ω, f = 1MHz, Figure 6		+25°C		92		dB
Channel-to-Channel Crosstalk (MAX4525L)	V_{CT}	R_L = 50Ω, f = 1MHz, Figure 6		+25°C		96		dB
On-Channel -3dB Bandwidth	BW	Figure 6		+25°C		200		MHz
Total Harmonic Distortion	THD	R_L = 600Ω, V_{COM} = 2.5V_{P-P}, 20Hz to 20kHz BW		+25°C		0.02		%
POWER SUPPLY								
Power-Supply Range	V+			-40°C to +85°C	2		12.6	V
Power-Supply Current	I+	V+ = 12.6V, $V_{ADD\_}$ = V_{INH} = V+ or 0V		+25°C	-1		+1	µA
				-40°C to +85°C	-10		+10	

Note 2: The TDFN package is production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 3: The algebraic convention used in this data sheet is where the most negative value is a minimum column.
Note 4: ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$.
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
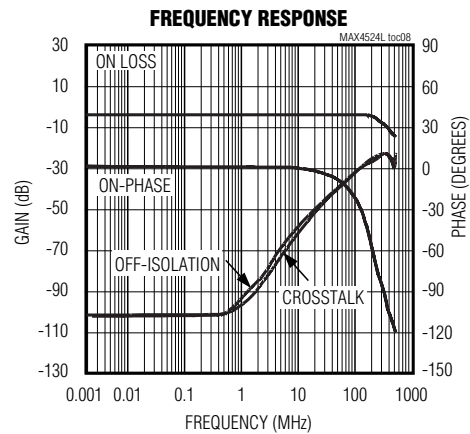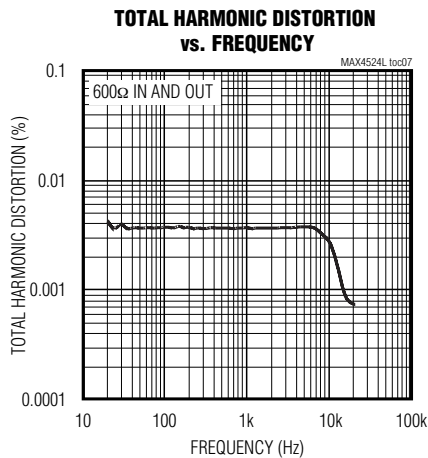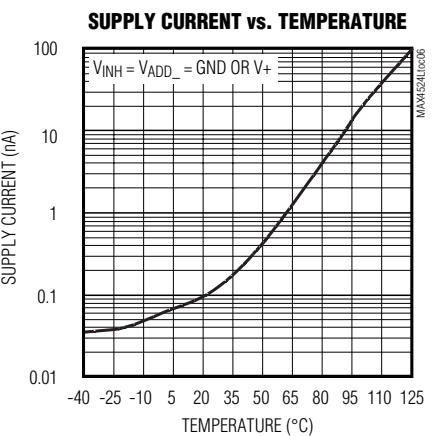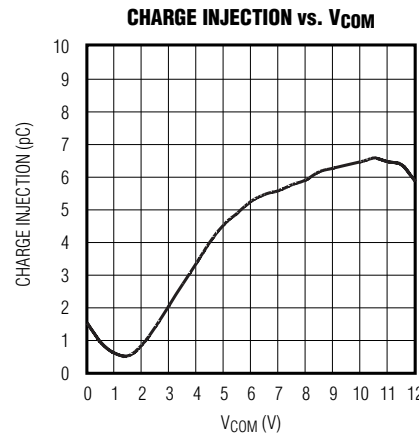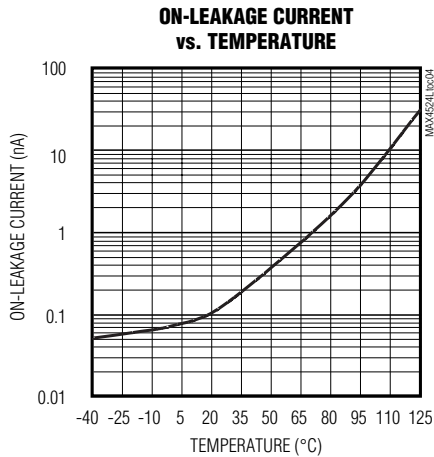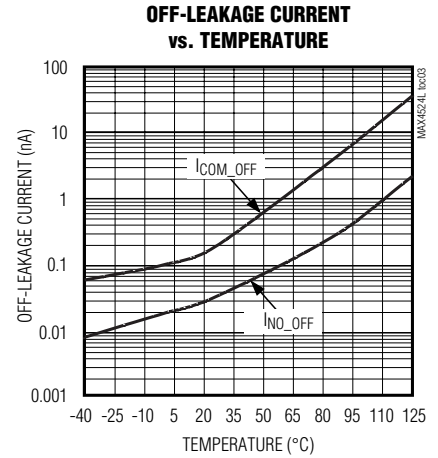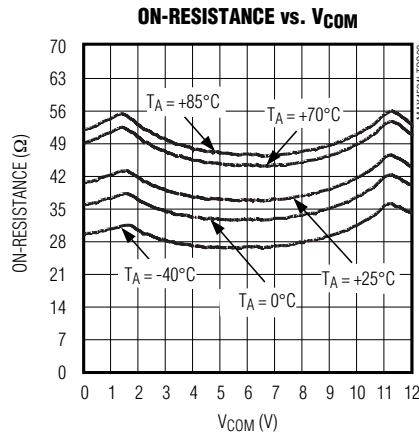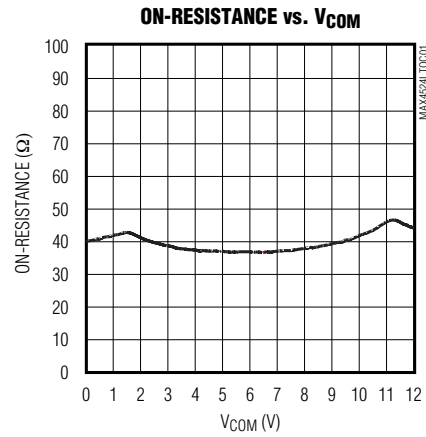**Note 6:** Leakage parameters are 100% tested at maximum-rated hot operating temperature and guaranteed by design at T_A = +25°C.
Note 7: Guaranteed by design, not production tested.

Low-Voltage, Single-Supply Analog Multiplexers/Switches

_____*Typical Operating Characteristics*

(V+ = 12V, V$_{INH}$ = GND, T$_A$ = +25°C, unless otherwise noted.)

ON-RESISTANCE vs. V$_{COM}$

ON-RESISTANCE vs. V$_{COM}$

OFF-LEAKAGE CURRENT vs. TEMPERATURE

ON-LEAKAGE CURRENT vs. TEMPERATURE

CHARGE INJECTION vs. V$_{COM}$

SUPPLY CURRENT vs. TEMPERATURE

TOTAL HARMONIC DISTORTION vs. FREQUENCY

FREQUENCY RESPONSE

MAXIM

_____*Typical Operating Characteristics (continued)*

(V+ = 12V, V_{INH} = GND, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. LOGIC-LEVEL VOLTAGE

INPUT LOGIC THRESHOLD vs. SUPPLY VOLTAGE
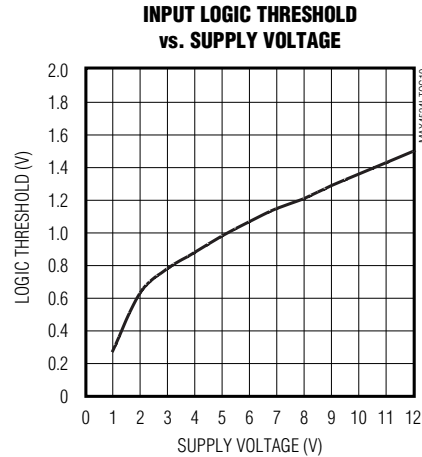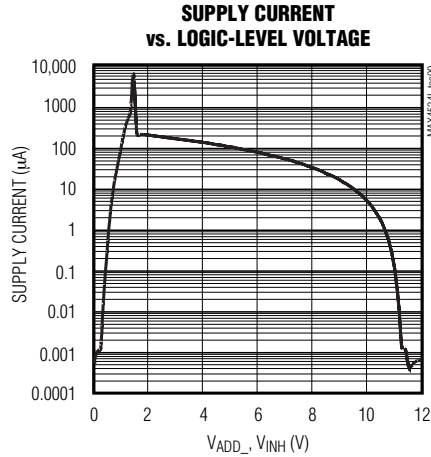
_____*Pin Description*

PIN		NAME	FUNCTION
MAX4524L	MAX4525L		
1	—	NO2	Analog Switch Normally Open Input 2
—	1	NOA	Analog Switch A Normally Open Input
2	—	NO3	Analog Switch Normally Open Input 3
—	2	COMA	Analog Switch A Common
3	—	NO1	Analog Switch Normally Open Input 1
—	3	NCA	Analog Switch A Normally Closed Input
4	4	INH	Inhibit. Drive INH low or connect to GND for normal operation. Drive INH high or connect to V+ to turn all switches off.
5	5	GND	Ground. Connect to digital ground (analog signals have no ground reference, but are limited to V+ and GND).
6	—	ADDB	Logic-Level Address Input (see *Truth Tables*)
—	6	ADD	Logic-Level Address Input (see *Truth Tables*)
7	—	ADDA	Logic-Level Address Input (see *Truth Tables*)
—	7	NCB	Analog Switch B Normally Closed Input
8	—	NO0	Analog Switch Normally Open Input 0
—	8	NOB	Analog Switch B Normally Open Input
9	—	COM	Analog Switch Common
—	9	COMB	Analog Switch A Common
10	10	V+	Positive Analog and Digital Supply Voltage. Bypass with a 0.1µF capacitor to GND.
EP	EP	Exposed PAD	The bottom of the IC (TDFN package only) contains an exposed pad that must be connected externally to V+.

Low-Voltage, Single-Supply Analog Multiplexers/Switches

Detailed Description

The MAX4524L/MAX4525L are low-voltage, single-supply CMOS analog switches that operate from a single supply of +2V to +12V. Operation with a +12V supply optimizes the performance by reducing their on-resistance to 100Ω. The MAX4524L is configured as a 4-channel multiplexer/demultiplexer and the MAX4525L is a double-pole/double-throw (DPDT) switch. These devices have an inhibit input (INH) to simultaneously open all signal paths. Each switch can handle rail-to-rail analog signals. The off-leakage current is typically only 0.1nA at +25°C and 10nA (max) over temperature. All digital inputs have 0.8V to 2.0V logic-level thresholds, ensuring TTL/CMOS-logic compatibility when using a single +12V supply.

Applications Information

Power-Supply Considerations

The MAX4524L/MAX4525Ls' construction is typical of most CMOS analog switches. The supply input, V+, is used to power the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog signal pin and both V+ and GND. If any analog signal exceeds V+ or goes below GND, one of these diodes conducts. During normal operation, these reverse-biased ESD diodes leak, forming the only current drawn from V+ or GND. Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means that leakage varies as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND. V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V+ and GND signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies.
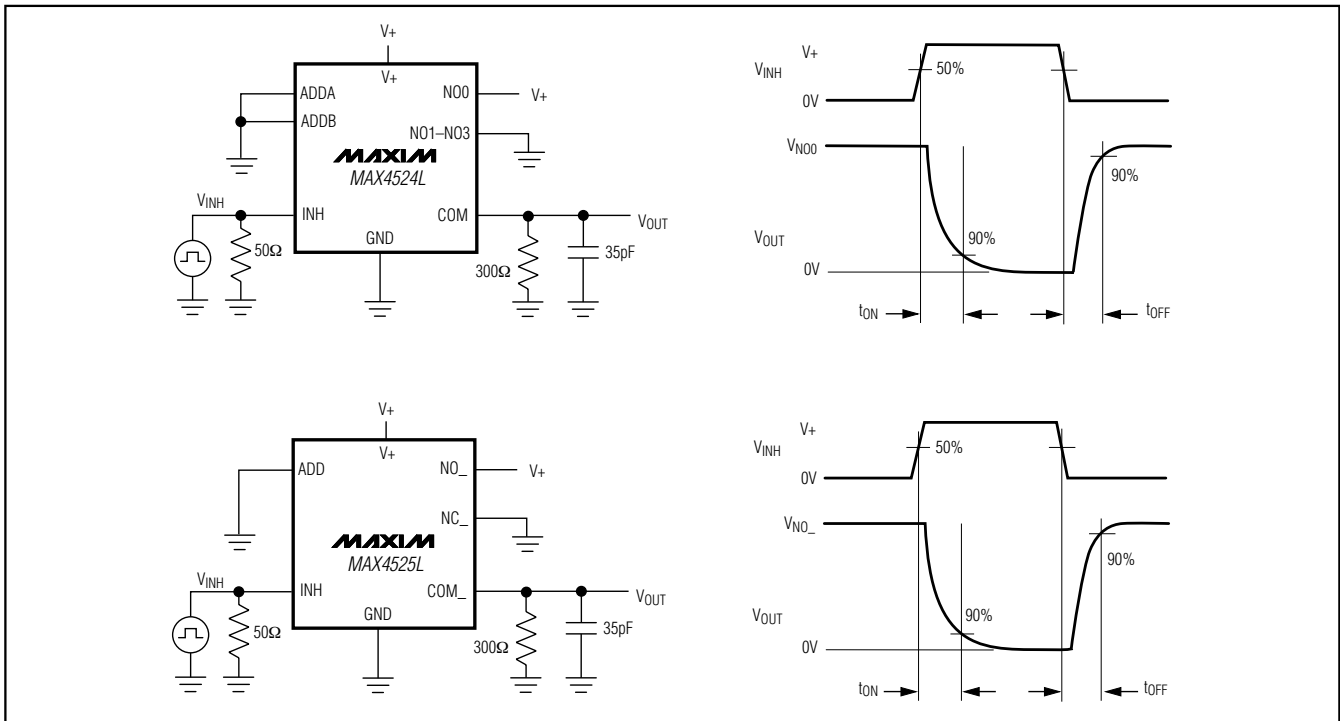
Test Circuits/Timing Diagrams

Figure 1. Inhibit Switching Times

MAXIM

Test Circuits/Timing Diagrams (continued)
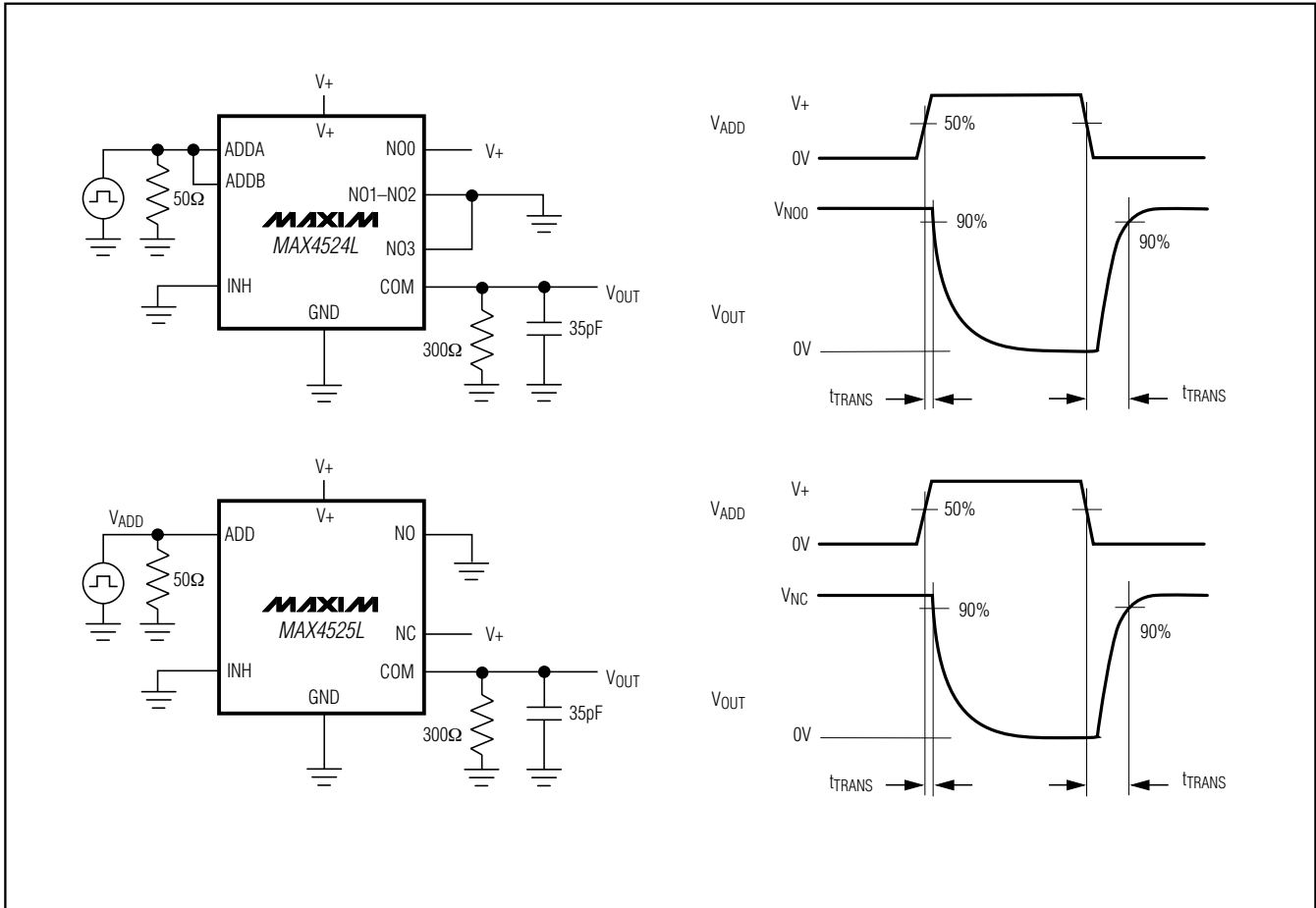
Figure 2. Address Transition Time
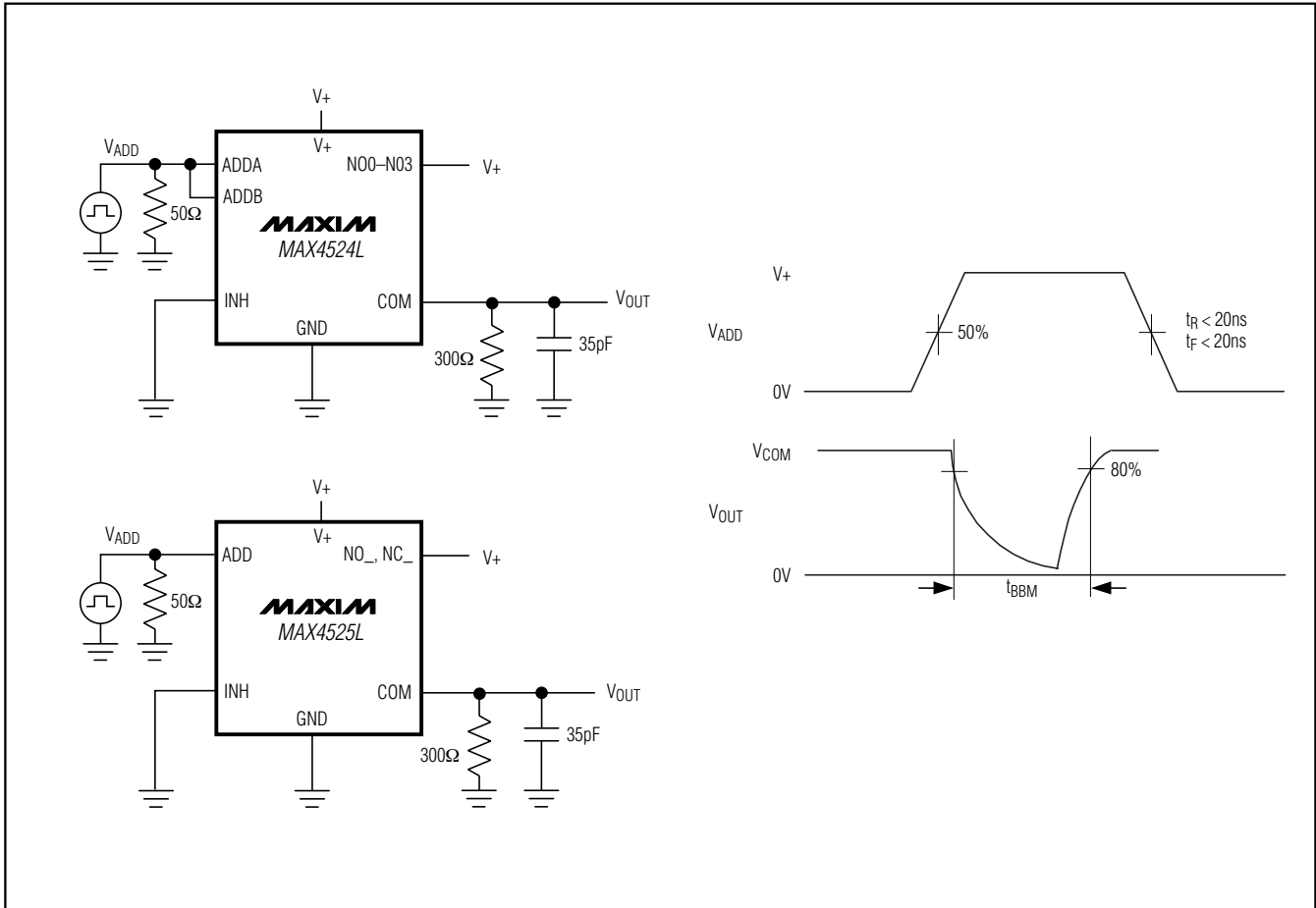
Figure 3. Break-Before-Make Interval
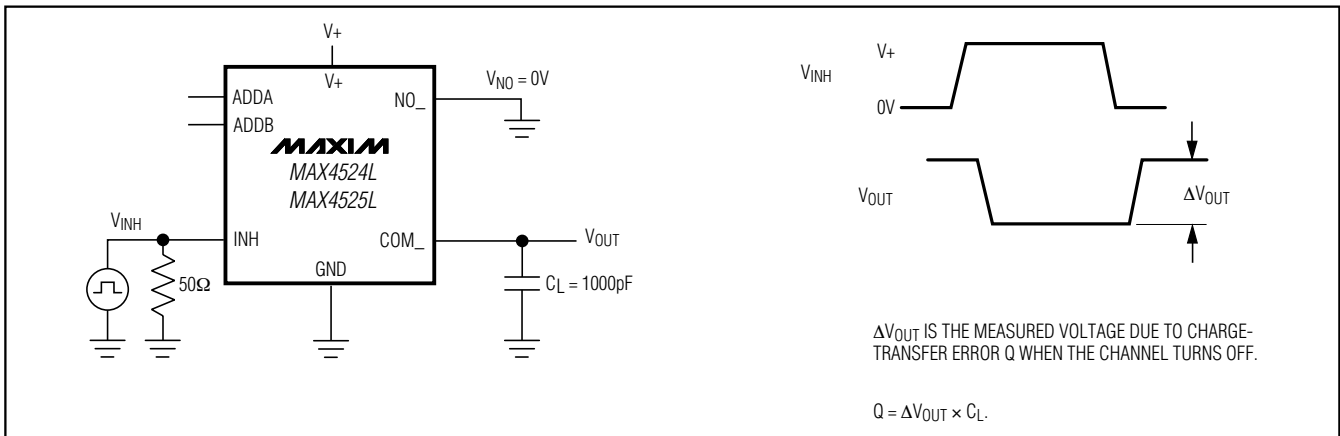
Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)
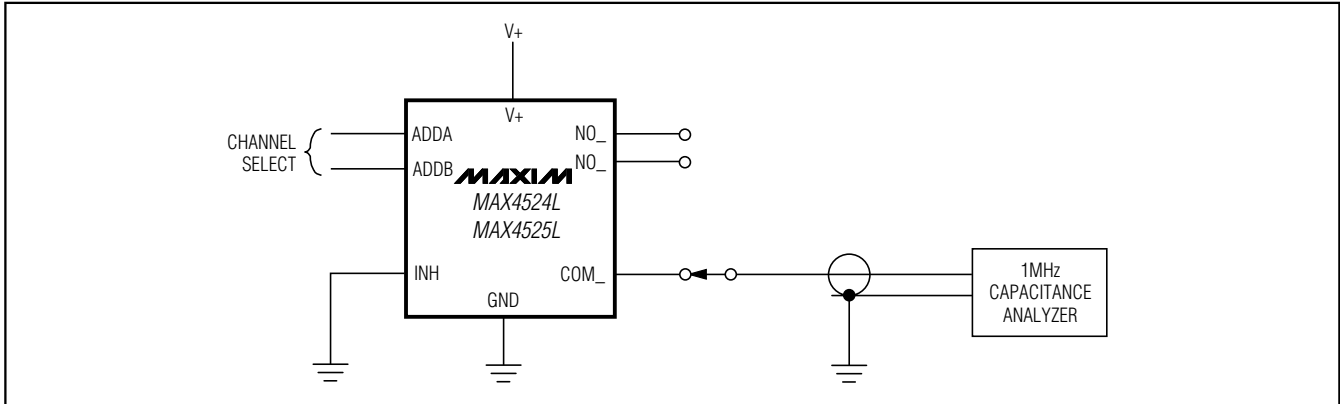
Figure 5. NO/COM Capacitance
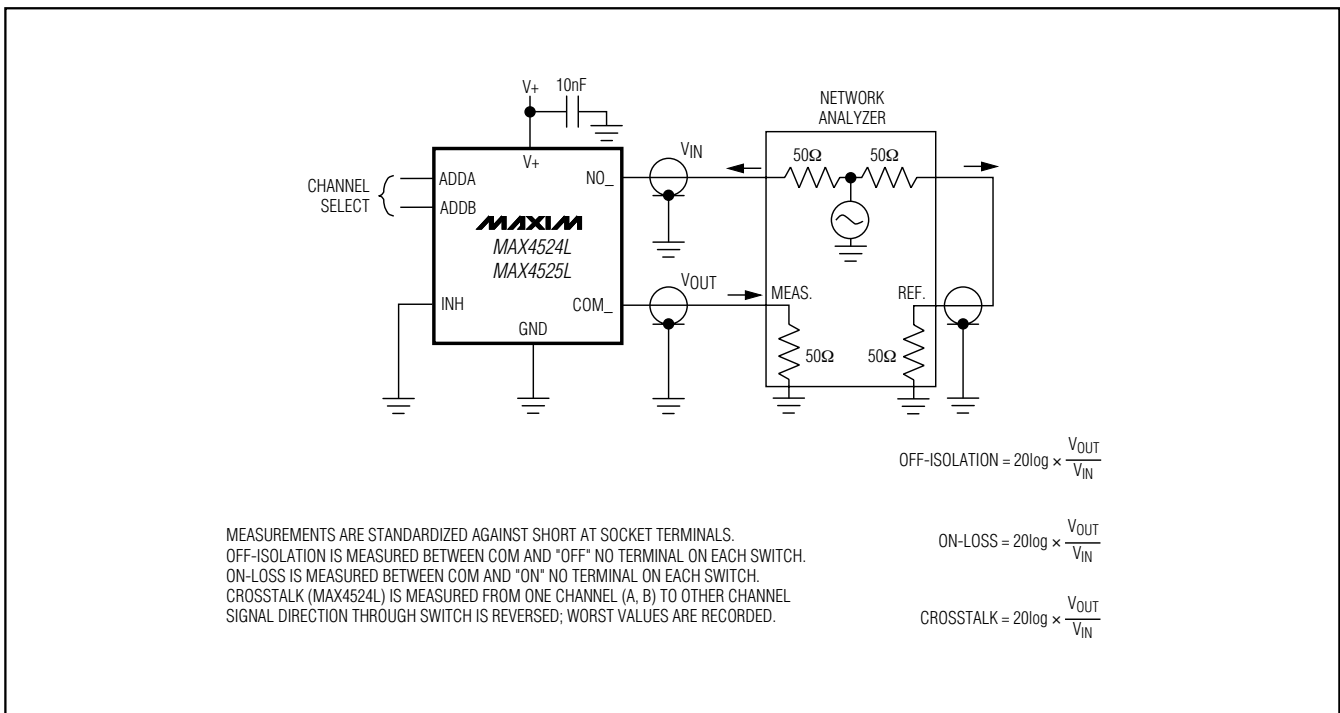
Figure 6. Off-Isolation, On-Loss, and Crosstalk

MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON-LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
CROSSTALK (MAX4524L) IS MEASURED FROM ONE CHANNEL (A, B) TO OTHER CHANNEL
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

$$\text{OFF-ISOLATION} = 20\log \times \frac{V_{OUT}}{V_{IN}}$$

$$\text{ON-LOSS} = 20\log \times \frac{V_{OUT}}{V_{IN}}$$

$$\text{CROSSTALK} = 20\log \times \frac{V_{OUT}}{V_{IN}}$$

Chip Information

TRANSISTOR COUNT: 219
PROCESS: CMOS

Low-Voltage, Single-Supply Analog Multiplexers/Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS
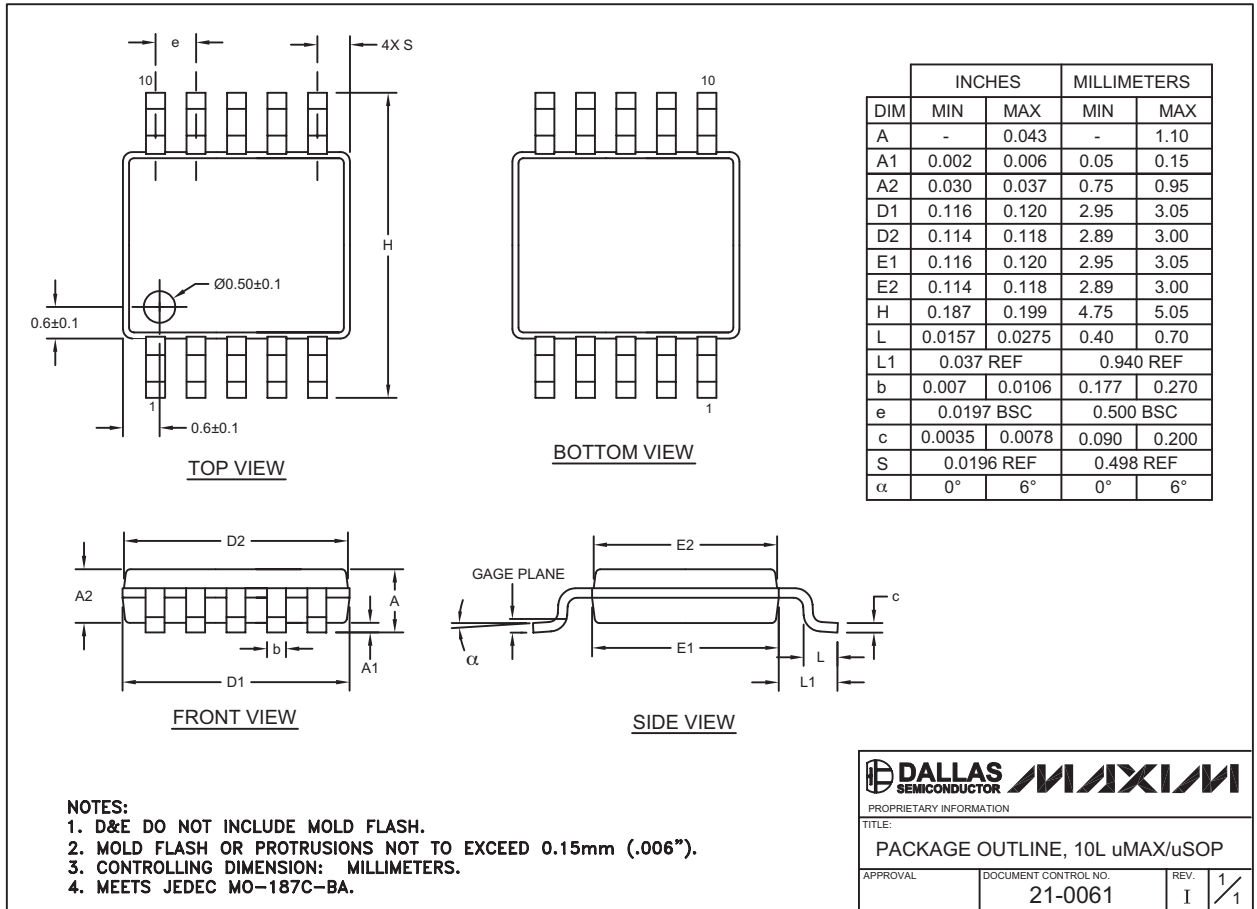
TOP VIEW

Ø0.50±0.1

0.6±0.1

0.6±0.1

4X S

BOTTOM VIEW

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°

FRONT VIEW

SIDE VIEW

GAGE PLANE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR /\/\/XI/\/\

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

/\/\/XI/\/\

Low-Voltage, Single-Supply Analog Multiplexers/Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)
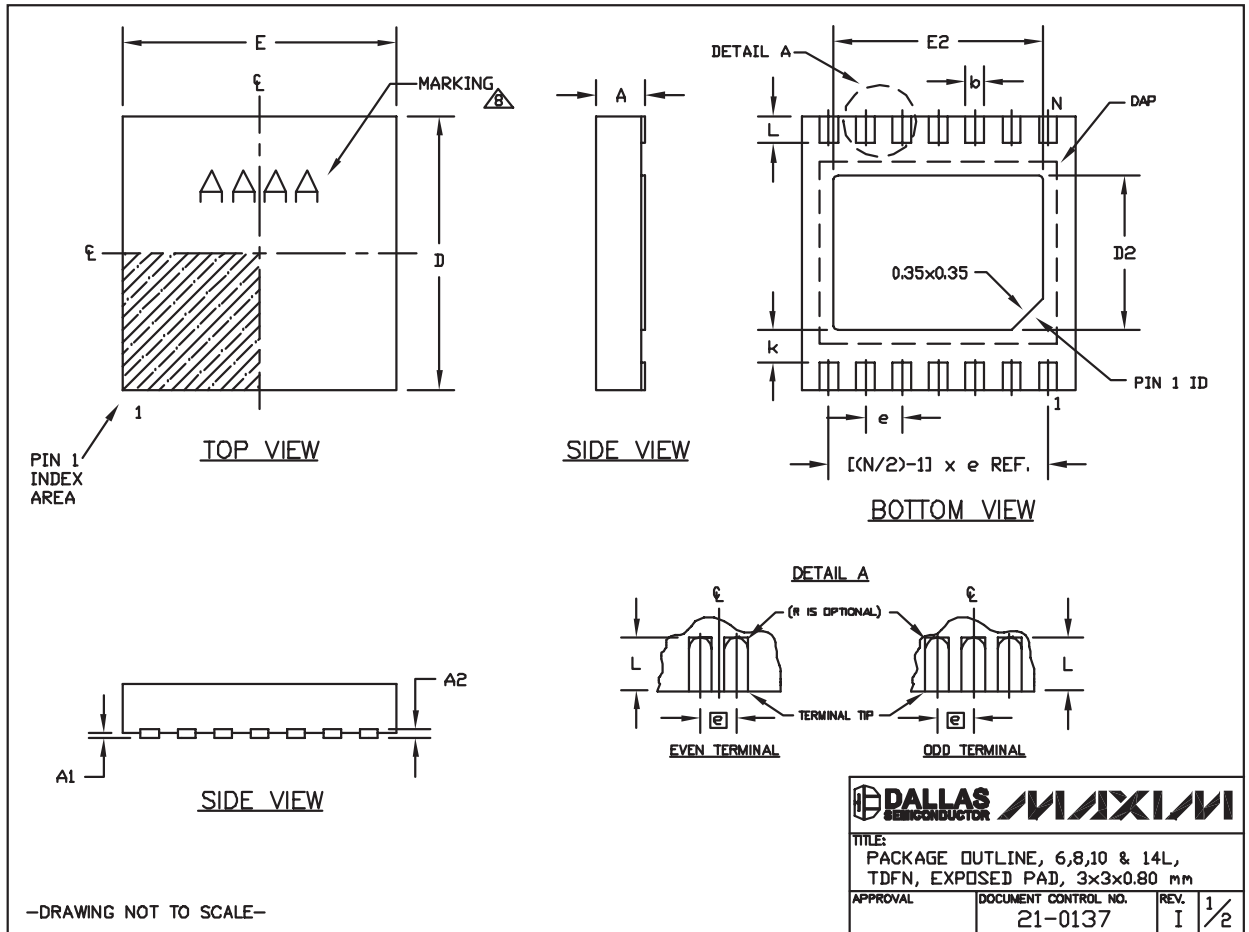

6, 8, &10L, DFN THIN.EPS

TOP VIEW

SIDE VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

EVEN TERMINAL   ODD TERMINAL

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR /ИΙΛΧΙΛΛ

TITLE:
PACKAGE OUTLINE, 6,8,10 & 14L,
TDFN, EXPOSED PAD, 3×3×0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	1/2

MAX4524L/MAX4525L

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR **MAXIM**

TITLE:
PACKAGE OUTLINE, 6,8,10 & 14L,
TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

—DRAWING NOT TO SCALE—

Revision History

Pages changed at Rev 1: 1, 5, 6, 11, 12