Freescale Semiconductor
Data Sheet: Technical Data

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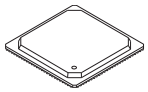
MPC5121E/MPC5123



516 TEPBGA
27 mm x 27 mm

MPC5121E/MPC5123 Data Sheet

The MPC5121e/MPC5123 integrates a high performance e300 CPU core based on the Power Architecture® Technology with a rich set of peripheral functions focused on communications and systems integration.

Major features of the MPC5121e/MPC5123 are:

- e300 Power Architecture processor core
- Power modes include doze, nap, sleep, deep sleep, and hibernate
- AXE – Auxiliary Execution Engine
- MBX Lite – 2D/3D graphics engine (not available in MPC5123)
- DIU – Display interface unit
- DDR1, DDR2, and LPDDR/mobile-DDR SDRAM memory controller
- MEM – 128 KB on-chip SRAM
- USB 2.0 OTG controller with integrated physical layer (PHY)
- DMA subsystem
- EMB – Flexible multi-function external memory bus interface
- NFC – NAND flash controller
- LPC – LocalPlus interface
- 10/100Base Ethernet
- PCI interface, version 2.3
- PATA – Parallel ATA integrated development environment (IDE) controller
- SATA – Serial ATA controller with integrated physical layer (PHY)
- SDHC – MMC/SD/SDIO card host controller
- PSC – Programmable serial controller
- I^2C – inter-integrated circuit communication interfaces
- S/PDIF – Serial audio interface
- CAN – Controller area network
- BDLC – J1850 interface
- VIU – Video Input, ITU-656 compliant
- RTC – On-Chip real-time clock
- On-chip temperature sensor
- IIM – IC Identification module

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Figure 1 shows a simplified MPC5121e/MPC5123 block diagram.

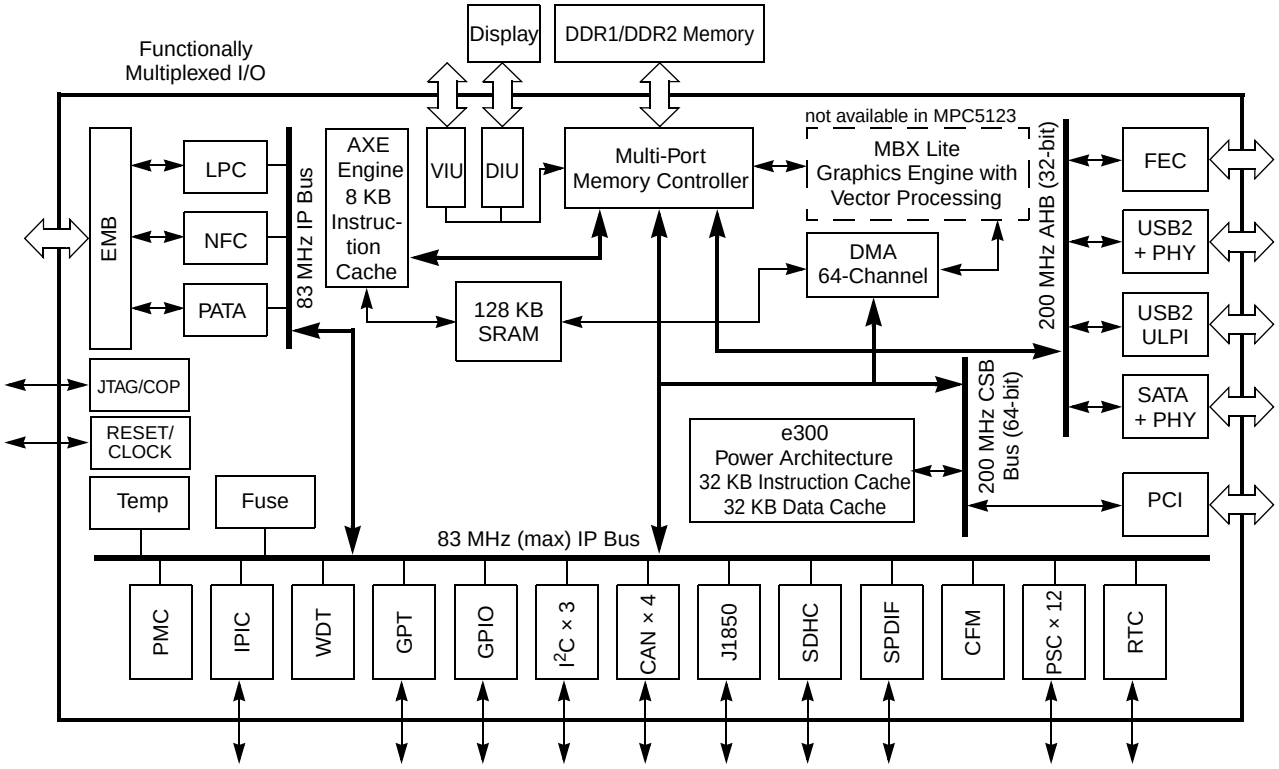

Figure 1. Simplified MPC5121e/MPC5123 Block Diagram

1 Ordering Information

Table 1. MPC5121e Orderable Part Numbers

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5121VY400B	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tray
MPC5121VY400BR	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tape and Reel
MPC5121YVY400B	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tray
MPC5121YVY400BR	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tape and Reel
SPC5121YVY400B	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tray
SPC5121YVY400BR	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tape and Reel

Table 2. MPC5123 Orderable Part Numbers

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5123VY400B	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tray
MPC5123VY400BR	400	0 °C to 70 °C	Consumer	RoHS and Pb-free	Tape and Reel
MPC5123YVY400B	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tray

Table 2. MPC5123 Orderable Part Numbers (continued)

Freescale Part Number	Speed (MHz)	Temperature (ambient)	Qualification	Package	Availability
MPC5123YVY400BR	400	–40 °C to 85 °C	Industrial	RoHS and Pb-free	Tape and Reel
SPC5123YVY400B	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tray
SPC5123YVY400BR	400	–40 °C to 85 °C	Automotive—AEC	RoHS and Pb-free	Tape and Reel

2 Pin Assignments

This section details pin assignments.

2.1 516-TEPBGA Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A		VSS	VSS	SATA_RXN	SATA_RXP	SATA_RX_VSSA	PSC7_4	PSC7_3	PSC6_4	PSC6_2	PSC6_0	PSC11_0	PSC10_2	PSC2_3	PSC1_3	PSC1_1	PSC0_1	CAN1_TX	GPIO28	RTC_XTALO	USB2_DRVVBUS	USB_DM	USB_DP	USB_TPA	VSS	
B	VSS	VSS	VSS	SATA_RX_VSSA	VSS	PSC8_3	VSS	PSC7_0	PSC6_3	VDD_IO	PSC11_1	VSS	PSC10_1	PSC2_1	VDD_IO	PSC0_4	VSS	GPIO31	CAN2_RX	VSS	USB2_VBUS_PWR_FAULT	VSS	USB_VSSA_BIAS	USB_XTALO	VDD_IO	VSS
C	VSS	SATA_XTALO	SATA_XTALI	VSS	SATA_VDDA_1P2	PSC9_0	PSC8_2	PSC7_2	AVDD_FUSEWR	PSC6_1	PSC11_2	PSC10_3	PSC10_0	PSC2_0	PSC1_0	PSC0_3	PSC_MCLK_IN	GPIO30	CAN1_RX	RTC_XTALI	USB_VDDA	USB_VSSA	VSS	USB_XTALI	VSS	PCI_CLK
D	SATA_VDDA_1P2	VSS	SATA_PLL_VSSA	SATA_VDDA_3P3	SATA_VDDA_VREG	PSC9_3	PSC9_1	PSC8_1	VDD_IO	VDD_IO	PSC11_4	VSS	PSC2_4	PSC1_4	VDD_IO	PSC0_0	VSS	HIB_MODE	VBAT_RTC	USB_VDDA	USB_VBUS	USB_VDDA_BIAS	USB_PLL_PWR3	VSS	VSS	PCI_REQ2
E	SATA_TXN	SATA_VDDA_1P2	SATA_PLL_VDDA1P2	SATA_RESREF	SATA_ANAVIZ	PSC9_4	PSC9_2	PSC8_4	PSC8_0	PSC7_1	PSC11_3	PSC10_4	PSC2_2	PSC1_2	PSC0_2	CAN2_TX	GPIO29	VSS	USB_UID	USB_VSSA	USB_VSSA	USB_RREF	USB_PLL_GND	PCI_GNT2	PCI_GNT0	PCI_REQ1
F	SATA_TXP	VSS	VSS	VSS	VSS	VSS		VSS		VSS	VDD_IO		VDD_IO	VDD_IO		VSS	VSS		VDD_IO		VSS	PCI_RST_OUT	VDD_IO	PCI_AD30	VDD_IO	PCI_AD28
G	SATA_TX_VSSA	NFC_RE	NFC_WE	NFC_WP	VSS																	PCI_GNT1	PCI_REQ0	PCI_AD29	PCI_AD26	PCI_C/BE3
H	NFC_R/B	PATA_DACK	NFC_CE0	NFC_ALE	NFC_CLE	VSS															VDD_IO	PCI_AD31	VSS	PCI_AD24	VSS	PCI_AD21
J	PATA_IOR	PATA_IOCHRDY	PATA_INTRQ	PATA_DRQ	VDD_IO																	PCI_AD27	PCI_AD25	PCI_AD23	PCI_AD20	PCI_AD18
K	PATA_CE1	VDD_IO	PATA_ISOLATE	VDD_IO	PATA_IOW	VSS				VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE				VSS	PCI_IDSEL	PCI_AD22	PCI_AD19	PCI_AD17	PCI_IRDY
L	EMB_AD03	EMB_AD02	EMB_AD01	EMB_AD00	PATA_CE2	VSS				VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE				VSS	PCI_AD16	VDD_IO	PCI_C/BE2	VDD_IO	PCI_DEVSEL
M	EMB_AD06	VSS	EMB_AD05	VSS	EMB_AD04					VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE					PCI_TRDY	PCI_FRAME	PCI_STOP	PCI_PERR	PCI_SERR
N	EMB_AD10	EMB_AD09	EMB_AD08	EMB_AD07	VSS	VDD_IO				VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE				VDD_IO	PCI_PAR	VSS	PCI_C/BE1	VSS	PCI_AD15
P	EMB_AD15	EMB_AD14	EMB_AD11	EMB_AD13	EMB_AD12	VDD_IO				VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE				VDD_IO	PCI_C/BE0	PCI_AD09	PCI_AD13	PCI_AD14	PCI_AD12
R	EMB_AD17	VDD_IO	EMB_AD16	VDD_IO	EMB_AD19					VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE					PCI_AD03	PCI_AD06	PCI_AD10	PCI_AD11	PCI_AD08
T	EMB_AD22	EMB_AD18	EMB_AD20	EMB_AD21	EMB_AD23	VSS				VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE				VSS	SYS_PLL_AVDD	VDD_IO	PCI_AD05	VDD_IO	PCI_AD07
U	EMB_AD25	VSS	EMB_AD24	VSS	EMB_AD29	VSS				VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE				VSS	SYS_PLL_AVSS	PCI_INTA	PCI_AD00	PCI_AD02	PCI_AD04
V	EMB_AD26	EMB_AD27	EMB_AD28	EMB_AD30	EMB_AX01																	SRESET	VSS	SYS_XTALI	VSS	PCI_AD01
W	EMB_AD31	EMB_AX00	EMB_AX02	LPC_AX03	LPC_CS0	VDD_IO															VDD_IO	TDO	PORESET	HRESET	TEST	SYS_XTALO
Y	LPC_CS2	VDD_IO	LPC_CS1	VDD_IO	LPC_OE																	J1850_TX	TDI	VSS	TMS	CKSTP_OUT
AA	LPC_RWB	LPC_ACK	PSC4_1	LPC_CLK	PSC4_3	VSS		VDD_MEM_IO		VSS	VSS		VDD_MEM_IO	VDD_MEM_IO		VSS	VSS		CORE_PLL_AVDD		VSS	I2C2_SDA	VDD_IO	J1850_RX	VDD_IO	TRST
AB	PSC4_0	VSS	PSC4_2	VSS	PSC3_1	MDQ1	MVTT0	MDQ5	MDQ10	VSS	MVREF	MDQ19	MDQ21	MDQ27	MDQ31	MA1	MA5	VDD_MEM_IO	MA14	MCKE	SPDIF_TXCLK	I2C1_SCL	I2C1_SDA	VSS	IRQ1	TCK
AC	PSC5_0	PSC4_4	PSC5_1	PSC3_2	VDD_MEM_IO	MDM0	MDQ8	VSS	MDQ14	VDD_MEM_IO	MDQS2	VSS	MDQ25	VDD_MEM_IO	MDQ30	MBA1	VSS	MA7	MA11	VDD_MEM_IO	MODT	VSS	I2C0_SCL	SPDIF_RX	I2C2_SCL	IRQ0
AD	PSC5_2	PSC5_3	VSS	PSC3_3	MDQS0	MDQ6	MDQ11	MDQS1	VDD_MEM_IO	MDQ16	MDQ18	MDQ20	MDQ23	MDQS3	MDQ29	MBA0	MA0	MA4	MA9	MA13	MWE	MCS	CORE_PLL_AVSS	SPDIF_TX	VSS	I2C0_SDA
AE	VDD_IO	VDD_IO	PSC5_4	MDQ2	VDD_MEM_IO	MDQ7	VSS	MDM1	MDQ12	VDD_MEM_IO	MVTT2	VSS	MDQ24	MVTT3	VDD_MEM_IO	MDQ28	VSS	MA2	MA6	VDD_MEM_IO	MA12	MA15	VSS	VDD_IO	VDD_IO	VSS
AF		VDD_IO	PSC3_0	PSC3_4	MDQ0	MDQ3	MDQ4	MDQ9	MVTT1	MDQ13	MDQ15	MDQ17	MDM2	MDQ22	MDQ26	MDM3	MCK	MCK	MBA2	MA3	MA8	MA10	MRAS	MCAS	VDD_IO	

Figure 2. Ball Map for the MPC5121e 516 TEPBGA Package

2.2 Pinout Listings

Table 3 provides the pin-out listing for the MPC5121e/MPC5123.

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 1 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
DDR Memory Interface (67 Total)				
MDQ0	AF5	DDR	$V_{DD\_MEM\_IO}$	—
MDQ1	AB6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ2	AE4	DDR	$V_{DD\_MEM\_IO}$	—
MDQ3	AF6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ4	AF7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ5	AB8	DDR	$V_{DD\_MEM\_IO}$	—
MDQ6	AD6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ7	AE6	DDR	$V_{DD\_MEM\_IO}$	—
MDQ8	AC7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ9	AF8	DDR	$V_{DD\_MEM\_IO}$	—
MDQ10	AB9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ11	AD7	DDR	$V_{DD\_MEM\_IO}$	—
MDQ12	AE9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ13	AF10	DDR	$V_{DD\_MEM\_IO}$	—
MDQ14	AC9	DDR	$V_{DD\_MEM\_IO}$	—
MDQ15	AF11	DDR	$V_{DD\_MEM\_IO}$	—
MDQ16	AD10	DDR	$V_{DD\_MEM\_IO}$	—
MDQ17	AF12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ18	AD11	DDR	$V_{DD\_MEM\_IO}$	—
MDQ19	AB12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ20	AD12	DDR	$V_{DD\_MEM\_IO}$	—
MDQ21	AB13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ22	AF14	DDR	$V_{DD\_MEM\_IO}$	—
MDQ23	AD13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ24	AE13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ25	AC13	DDR	$V_{DD\_MEM\_IO}$	—
MDQ26	AF15	DDR	$V_{DD\_MEM\_IO}$	—
MDQ27	AB14	DDR	$V_{DD\_MEM\_IO}$	—
MDQ28	AE16	DDR	$V_{DD\_MEM\_IO}$	—
MDQ29	AD15	DDR	$V_{DD\_MEM\_IO}$	—
MDQ30	AC15	DDR	$V_{DD\_MEM\_IO}$	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 2 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
MDQ31	AB15	DDR	$V_{DD\_MEM\_IO}$	—
MDM0	AC6	DDR	$V_{DD\_MEM\_IO}$	—
MDM1	AE8	DDR	$V_{DD\_MEM\_IO}$	—
MDM2	AF13	DDR	$V_{DD\_MEM\_IO}$	—
MDM3	AF16	DDR	$V_{DD\_MEM\_IO}$	—
MDQS0	AD5	DDR	$V_{DD\_MEM\_IO}$	—
MDQS1	AD8	DDR	$V_{DD\_MEM\_IO}$	—
MDQS2	AC11	DDR	$V_{DD\_MEM\_IO}$	—
MDQS3	AD14	DDR	$V_{DD\_MEM\_IO}$	—
MBA0	AD16	DDR	$V_{DD\_MEM\_IO}$	—
MBA1	AC16	DDR	$V_{DD\_MEM\_IO}$	—
MBA2	AF19	DDR	$V_{DD\_MEM\_IO}$	—
MA0	AD17	DDR	$V_{DD\_MEM\_IO}$	—
MA1	AB16	DDR	$V_{DD\_MEM\_IO}$	—
MA2	AE18	DDR	$V_{DD\_MEM\_IO}$	—
MA3	AF20	DDR	$V_{DD\_MEM\_IO}$	—
MA4	AD18	DDR	$V_{DD\_MEM\_IO}$	—
MA5	AB17	DDR	$V_{DD\_MEM\_IO}$	—
MA6	AE19	DDR	$V_{DD\_MEM\_IO}$	—
MA7	AC18	DDR	$V_{DD\_MEM\_IO}$	—
MA8	AF21	DDR	$V_{DD\_MEM\_IO}$	—
MA9	AD19	DDR	$V_{DD\_MEM\_IO}$	—
MA10	AF22	DDR	$V_{DD\_MEM\_IO}$	—
MA11	AC19	DDR	$V_{DD\_MEM\_IO}$	—
MA12	AE21	DDR	$V_{DD\_MEM\_IO}$	—
MA13	AD20	DDR	$V_{DD\_MEM\_IO}$	—
MA14	AB19	DDR	$V_{DD\_MEM\_IO}$	—
MA15	AE22	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MWE}}$	AD21	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MRAS}}$	AF23	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MCAS}}$	AF24	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MCS}}$	AD22	DDR	$V_{DD\_MEM\_IO}$	—
MCKE	AB20	DDR	$V_{DD\_MEM\_IO}$	—
MCK	AF17	DDR	$V_{DD\_MEM\_IO}$	—
$\overline{\text{MCK}}$	AF18	DDR	$V_{DD\_MEM\_IO}$	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 3 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
MODT	AC21	DDR	$V_{DD\_MEM\_IO}$	—
LPC Interface (8 Total)				
LPC_CLK	AA4	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_OE}}$	Y5	General IO	V_{DD_IO}	—
LPC_$\overline{\text{RW}}$	AA1	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_CS0}}$	W5	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_CS1}}$	Y3	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_CS2}}$	Y1	General IO	V_{DD_IO}	—
$\overline{\text{LPC\_ACK}}$	AA2	General IO	V_{DD_IO}	—
LPC_AX03	W4	General IO	V_{DD_IO}	—
EMB Interface (35 Total)				
EMB_AX02	W3	General IO	V_{DD_IO}	—
EMB_AX01	V5	General IO	V_{DD_IO}	—
EMB_AX00	W2	General IO	V_{DD_IO}	—
EMB_AD31	W1	General IO	V_{DD_IO}	—
EMB_AD30	V4	General IO	V_{DD_IO}	—
EMB_AD29	U5	General IO	V_{DD_IO}	—
EMB_AD28	V3	General IO	V_{DD_IO}	—
EMB_AD27	V2	General IO	V_{DD_IO}	—
EMB_AD26	V1	General IO	V_{DD_IO}	—
EMB_AD25	U1	General IO	V_{DD_IO}	—
EMB_AD24	U3	General IO	V_{DD_IO}	—
EMB_AD23	T5	General IO	V_{DD_IO}	—
EMB_AD22	T1	General IO	V_{DD_IO}	—
EMB_AD21	T4	General IO	V_{DD_IO}	—
EMB_AD20	T3	General IO	V_{DD_IO}	—
EMB_AD19	R5	General IO	V_{DD_IO}	—
EMB_AD18	T2	General IO	V_{DD_IO}	—
EMB_AD17	R1	General IO	V_{DD_IO}	—
EMB_AD16	R3	General IO	V_{DD_IO}	—
EMB_AD15	P1	General IO	V_{DD_IO}	—
EMB_AD14	P2	General IO	V_{DD_IO}	—
EMB_AD13	P4	General IO	V_{DD_IO}	—
EMB_AD12	P5	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 4 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
EMB_AD11	P3	General IO	V_{DD_IO}	—
EMB_AD10	N1	General IO	V_{DD_IO}	—
EMB_AD09	N2	General IO	V_{DD_IO}	—
EMB_AD08	N3	General IO	V_{DD_IO}	—
EMB_AD07	N4	General IO	V_{DD_IO}	—
EMB_AD06	M1	General IO	V_{DD_IO}	—
EMB_AD05	M3	General IO	V_{DD_IO}	—
EMB_AD04	M5	General IO	V_{DD_IO}	—
EMB_AD03	L1	General IO	V_{DD_IO}	—
EMB_AD02	L2	General IO	V_{DD_IO}	—
EMB_AD01	L3	General IO	V_{DD_IO}	—
EMB_AD00	L4	General IO	V_{DD_IO}	—
PATA Interface (9 Total)				
$\overline{\text{PATA\_CE1}}$	K1	General IO	V_{DD_IO}	ATA name: CS0
$\overline{\text{PATA\_CE2}}$	L5	General IO	V_{DD_IO}	ATA name: CS1
PATA_ISOLATE	K3	General IO	V_{DD_IO}	—
$\overline{\text{PATA\_IOR}}$	J1	General IO	V_{DD_IO}	ATA name: DIOR
$\overline{\text{PATA\_IOW}}$	K5	General IO	V_{DD_IO}	ATA name: DIOW
PATA_IOCHRDY	J2	General IO	V_{DD_IO}	ATA name: IORDY
PATA_INTRQ	J3	General IO	V_{DD_IO}	—
PATA_DRQ	J4	General IO	V_{DD_IO}	ATA name: DMARQ
$\overline{\text{PATA\_DACK}}$	H2	General IO	V_{DD_IO}	ATA name: DMACK
NFC Interface (7 Total)				
$\overline{\text{NFC\_WP}}$	G4	General IO	V_{DD_IO}	—
NFC_R/$\overline{\text{B}}$	H1	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_WE}}$	G3	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_RE}}$	G2	General IO	V_{DD_IO}	—
NFC_ALE	H4	General IO	V_{DD_IO}	—
NFC_CLE	H5	General IO	V_{DD_IO}	—
$\overline{\text{NFC\_CE0}}$	H3	General IO	V_{DD_IO}	—
I2C Interface (6 Total)				
I2C0_SCL	AC23	General IO	V_{DD_IO}	—
I2C0_SDA	AD26	General IO	V_{DD_IO}	—
I2C1_SCL	AB22	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 5 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
I2C1_SDA	AB23	General IO	V_{DD_IO}	—
I2C2_SCL	AC25	General IO	V_{DD_IO}	—
I2C2_SDA	AA22	General IO	V_{DD_IO}	—
IRQ Interface (2 Total)				
$\overline{IRQ0}$	AC26	General IO	V_{DD_IO}	—
$\overline{IRQ1}$	AB25	General IO	V_{DD_IO}	—
CAN Interface (4 Total)				
CAN1_RX	C19	Analog Input	VBAT_RTC	—
CAN1_TX	A18	General IO	V_{DD_IO}	—
CAN2_RX	B19	Analog Input	VBAT_RTC	—
CAN2_TX	E16	General IO	V_{DD_IO}	—
J1850 Interface (2 Total)				
J1850_TX	Y22	General IO	V_{DD_IO}	—
J1850_RX	AA24	General IO	V_{DD_IO}	—
SPDIF Interface (3 Total)				
SPDIF_TXCLK	AB21	General IO	V_{DD_IO}	—
SPDIF_TX	AD24	General IO	V_{DD_IO}	—
SPDIF_RX	AC24	General IO	V_{DD_IO}	—
PCI (54 Total)				
$\overline{PCI\_INTA}$	U23	PCI	V_{DD_IO}	—
$\overline{PCI\_RST\_OUT}$	F22	PCI	V_{DD_IO}	—
PCI_AD00	U24	PCI	V_{DD_IO}	—
PCI_AD01	V26	PCI	V_{DD_IO}	—
PCI_AD02	U25	PCI	V_{DD_IO}	—
PCI_AD03	R22	PCI	V_{DD_IO}	—
PCI_AD04	U26	PCI	V_{DD_IO}	—
PCI_AD05	T24	PCI	V_{DD_IO}	—
PCI_AD06	R23	PCI	V_{DD_IO}	—
PCI_AD07	T26	PCI	V_{DD_IO}	—
PCI_AD08	R26	PCI	V_{DD_IO}	—
PCI_AD09	P23	PCI	V_{DD_IO}	—
PCI_AD10	R24	PCI	V_{DD_IO}	—
PCI_AD11	R25	PCI	V_{DD_IO}	—
PCI_AD12	P26	PCI	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 6 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
PCI_AD13	P24	PCI	V_{DD_IO}	—
PCI_AD14	P25	PCI	V_{DD_IO}	—
PCI_AD15	N26	PCI	V_{DD_IO}	—
PCI_AD16	L22	PCI	V_{DD_IO}	—
PCI_AD17	K25	PCI	V_{DD_IO}	—
PCI_AD18	J26	PCI	V_{DD_IO}	—
PCI_AD19	K24	PCI	V_{DD_IO}	—
PCI_AD20	J25	PCI	V_{DD_IO}	—
PCI_AD21	H26	PCI	V_{DD_IO}	—
PCI_AD22	K23	PCI	V_{DD_IO}	—
PCI_AD23	J24	PCI	V_{DD_IO}	—
PCI_AD24	H24	PCI	V_{DD_IO}	—
PCI_AD25	J23	PCI	V_{DD_IO}	—
PCI_AD26	G25	PCI	V_{DD_IO}	—
PCI_AD27	J22	PCI	V_{DD_IO}	—
PCI_AD28	F26	PCI	V_{DD_IO}	—
PCI_AD29	G24	PCI	V_{DD_IO}	—
PCI_AD30	F24	PCI	V_{DD_IO}	—
PCI_AD31	H22	PCI	V_{DD_IO}	—
PCI_C/$\overline{BE}$0	P22	PCI	V_{DD_IO}	—
PCI_C/$\overline{BE}$1	N24	PCI	V_{DD_IO}	—
PCI_C/$\overline{BE}$2	L24	PCI	V_{DD_IO}	—
PCI_C/$\overline{BE}$3	G26	PCI	V_{DD_IO}	—
PCI_PAR	N22	PCI	V_{DD_IO}	—
$\overline{PCI\_FRAME}$	M23	PCI	V_{DD_IO}	1
$\overline{PCI\_TRDY}$	M22	PCI	V_{DD_IO}	1
$\overline{PCI\_IRDY}$	K26	PCI	V_{DD_IO}	1
$\overline{PCI\_STOP}$	M24	PCI	V_{DD_IO}	1
$\overline{PCI\_DEVSEL}$	L26	PCI	V_{DD_IO}	1
PCI_IDSEL	K22	PCI	V_{DD_IO}	—
$\overline{PCI\_SERR}$	M26	PCI	V_{DD_IO}	1
$\overline{PCI\_PERR}$	M25	PCI	V_{DD_IO}	1
$\overline{PCI\_REQ0}$	G23	PCI	V_{DD_IO}	1
$\overline{PCI\_REQ1}$	E26	PCI	V_{DD_IO}	1
$\overline{PCI\_REQ2}$	D26	PCI	V_{DD_IO}	1

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 7 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
$\overline{\text{PCI\_GNT0}}$	E25	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT1}}$	G22	PCI	V_{DD_IO}	—
$\overline{\text{PCI\_GNT2}}$	E24	PCI	V_{DD_IO}	—
PCI_CLK	C26	PCI	V_{DD_IO}	—
PSC Interface (61 Total)				
PSC_MCLK_IN	C17	General IO	V_{DD_IO}	—
PSC0_0	D16	General IO	V_{DD_IO}	—
PSC0_1	A17	General IO	V_{DD_IO}	—
PSC0_2	E15	General IO	V_{DD_IO}	—
PSC0_3	C16	General IO	V_{DD_IO}	—
PSC0_4	B16	General IO	V_{DD_IO}	—
PSC1_0	C15	General IO	V_{DD_IO}	—
PSC1_1	A16	General IO	V_{DD_IO}	—
PSC1_2	E14	General IO	V_{DD_IO}	—
PSC1_3	A15	General IO	V_{DD_IO}	—
PSC1_4	D14	General IO	V_{DD_IO}	—
PSC2_0	C14	General IO	V_{DD_IO}	—
PSC2_1	B14	General IO	V_{DD_IO}	—
PSC2_2	E13	General IO	V_{DD_IO}	—
PSC2_3	A14	General IO	V_{DD_IO}	—
PSC2_4	D13	General IO	V_{DD_IO}	—
PSC3_0	AF3	General IO	V_{DD_IO}	—
PSC3_1	AB5	General IO	V_{DD_IO}	—
PSC3_2	AC4	General IO	V_{DD_IO}	—
PSC3_3	AD4	General IO	V_{DD_IO}	—
PSC3_4	AF4	General IO	V_{DD_IO}	—
PSC4_0	AB1	General IO	V_{DD_IO}	—
PSC4_1	AA3	General IO	V_{DD_IO}	—
PSC4_2	AB3	General IO	V_{DD_IO}	—
PSC4_3	AA5	General IO	V_{DD_IO}	—
PSC4_4	AC2	General IO	V_{DD_IO}	—
PSC5_0	AC1	General IO	V_{DD_IO}	—
PSC5_1	AC3	General IO	V_{DD_IO}	—
PSC5_2	AD1	General IO	V_{DD_IO}	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 8 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
PSC5_3	AD2	General IO	V_{DD_IO}	—
PSC5_4	AE3	General IO	V_{DD_IO}	—
PSC6_0	A11	General IO	V_{DD_IO}	—
PSC6_1	C10	General IO	V_{DD_IO}	—
PSC6_2	A10	General IO	V_{DD_IO}	—
PSC6_3	B9	General IO	V_{DD_IO}	—
PSC6_4	A9	General IO	V_{DD_IO}	—
PSC7_0	B8	General IO	V_{DD_IO}	—
PSC7_1	E10	General IO	V_{DD_IO}	—
PSC7_2	C8	General IO	V_{DD_IO}	—
PSC7_3	A8	General IO	V_{DD_IO}	—
PSC7_4	A7	General IO	V_{DD_IO}	—
PSC8_0	E9	General IO	V_{DD_IO}	—
PSC8_1	D8	General IO	V_{DD_IO}	—
PSC8_2	C7	General IO	V_{DD_IO}	—
PSC8_3	B6	General IO	V_{DD_IO}	—
PSC8_4	E8	General IO	V_{DD_IO}	—
PSC9_0	C6	General IO	V_{DD_IO}	—
PSC9_1	D7	General IO	V_{DD_IO}	—
PSC9_2	E7	General IO	V_{DD_IO}	—
PSC9_3	D6	General IO	V_{DD_IO}	—
PSC9_4	E6	General IO	V_{DD_IO}	—
PSC10_0	C13	General IO	V_{DD_IO}	—
PSC10_1	B13	General IO	V_{DD_IO}	—
PSC10_2	A13	General IO	V_{DD_IO}	—
PSC10_3	C12	General IO	V_{DD_IO}	—
PSC10_4	E12	General IO	V_{DD_IO}	—
PSC11_0	A12	General IO	V_{DD_IO}	—
PSC11_1	B11	General IO	V_{DD_IO}	—
PSC11_2	C11	General IO	V_{DD_IO}	—
PSC11_3	E11	General IO	V_{DD_IO}	—
PSC11_4	D11	General IO	V_{DD_IO}	—
JTAG (5 Total)				
TCK	AB26	General IO	V_{DD_IO}	2

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 9 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
TDI	Y23	General IO	V_{DD_IO}	3
TDO	W22	General IO	V_{DD_IO}	—
TMS	Y25	General IO	V_{DD_IO}	3
$\overline{\text{TRST}}$	AA26	General IO	V_{DD_IO}	3
Test / Debug (2 Total)				
TEST	W25	General IO	V_{DD_IO}	4, 5
$\overline{\text{CKSTP\_OUT}}$	Y26	General IO	V_{DD_IO}	—
System Control (3 Total)				
$\overline{\text{HRESET}}$	W24	General IO	V_{DD_IO}	6, 2
$\overline{\text{PORESET}}$	W23	General IO	V_{DD_IO}	4, 2
$\overline{\text{SRESET}}$	V22	General IO	V_{DD_IO}	6, 2
System Clock (2 Total)				
SYS_XTALI	V24	Analog Input	SYS_PLL_AVDD	Oscillator Input
SYS_XTALO	W26	Analog Output	SYS_PLL_AVDD	Oscillator Output
RTC (3 Total)				
RTC_XTALI	C20	Analog Input	VBAT_RTC	Oscillator Input
RTC_XTALO	A20	Analog Output	VBAT_RTC	Oscillator Output
$\overline{\text{HIB\_MODE}}$	D18	Analog Output	VBAT_RTC	—
GP Input Only (4 Total)				
GPIO28	A19	Analog Input	VBAT_RTC	—
GPIO29	E17	Analog Input	VBAT_RTC	—
GPIO30	C18	Analog Input	VBAT_RTC	—
GPIO31	B18	Analog Input	VBAT_RTC	—
DDR Reference Voltage				
MVREF	AB11	Analog Input	Voltage Reference for SSTL input pads	
USB – PHY without Power and Ground Supplies (7 Total)				
USB_XTALI	C24	Analog Input	USB_PLL_PWR3	Oscillator Input
USB_XTALO	B24	Analog Output	USB_PLL_PWR3	Oscillator Output
USB_DP	A23	Analog IO	USB_VDDA	—
USB_DM	A22	Analog IO	USB_VDDA	—
USB_TPA	A24	Analog Output	—	USB PHY debug output
USB_VBUS	D21	Analog IO	—	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 10 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
USB_UID	E19	Analog Input	—	—
USB digital IOs (2 Total)				
USB2_VBUS_PWR_FAULT	B21	General IO	V_{DD_IO}	—
USB2_DRVVBUS	A21	General IO	V_{DD_IO}	—
SATA PHY without Power and Ground Supplies (7 Total)				
SATA_XTALI	C3	Analog Input	SATA_VDDA_3P3	Oscillator Input
SATA_XTALO	C2	Analog Output	SATA_VDDA_3P3	Oscillator Output
SATA_ANAVIZ	E5	Analog Output	—	SATA PHY debug output
SATA_TXN	E1	Analog Output	SATA_VDDA_1P2	—
SATA_TXP	F1	Analog Output	SATA_VDDA_1P2	—
SATA_RXP	A5	Analog Input	SATA_VDDA_1P2	—
SATA_RXN	A4	Analog Input	SATA_VDDA_1P2	—
Power and Ground Supplies (without SATA PHY and USB PHY)				
V_{DD_CORE}	K10, K11, K12, K13, K14, K15, K16, K17, L10, L17, M10, M17, N10, N17, P10, P17, R10, R17, T10, T17, U10, U11, U12, U13, U14, U15, U16, U17	Power	—	—
V_{DD_IO}	B10, B15, B25, D9, D10, D15, F11, F13, F14, F19, F23, F25, H21, J5, K2, K4, L23, L25, N6, N21, P6, P21, R2, R4, T23, T25, W6, W21, Y2, Y4, AA23, AA25, AE1, AE2, AE24, AE25, AF2, AF25	Power	—	—
$V_{DD\_MEM\_IO}$	AA8, AA13, AA14, AB18, AC5, AC10, AC14, AC20, AD9, AE5, AE10, AE15, AE20	Power	—	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 11 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
V_{SS}	A2, A3, A25, B1,B2, B3, B5, B7, B12, B17, B20, B22, B26, C1, C4, C23, C25, D2, D12, D17, D24, D25, E18, F2, F3, F4, F5, F6, F8, F10, F16, F17, F21, G5, H6, H23, H25, K6, K21, L6, L11, L12, L13, L14, L15, L16, L21, M2, M4, M11, M12, M13, M14, M15, M16, N5, N11, N12, N13, N14, N15, N16,	Ground	—	—
V_{SS}	N23, N25, P11, P12, P13, P14, P15, P16, R11, R12, R13, R14, R15, R16, T6, T11, T12, T13, T14, T15, T16, T21, U2, U4, U6, U21, V23, V25, Y24, AA6, AA10, AA11, AA16, AA17, AA21, AB2, AB4, AB10, AB24, AC8, AC12, AC17, AC22, AD3, AD25, AE7, AE12, AE17, AE23, AE26	Ground	—	—
SYS_PLL_AVDD	T22	Analog Power	—	—
SYS_PLL_AVSS	U22	Analog Ground	—	—
CORE_PLL_AVDD	AA19	Analog Power	—	—
CORE_PLL_AVSS	AD23	Analog Ground	—	—
VBAT_RTC	D19	Power	—	—
AVDD_FUSEWR	C9	Power	—	—
MVTT0	AB7	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT1	AF9	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT2	AE11	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
MVTT3	AE14	Analog Input	SSTL(DDR2) Termination (ODT) Voltage	
Power and Ground Supplies (USB PHY)				
USB_PLL_GND	E23	Analog Ground	—	—
USB_PLL_PWR3	D23	Analog Power	—	—
USB_RREF	E22	Analog Power	—	—
USB_VSSA_BIAS	B23	Analog Ground	—	—

Table 3. MPC5121e/MPC5123 TE-PBGA Pinout Listing (Sheet 12 of 12)

Signal	Package Pin Number	Pad Type	Power Supply	Notes
USB_VDDA_BIAS	D22	Analog Power	—	—
USB_VSSA	C22, E20, E21	Analog Ground	—	—
USB_VDDA	C21, D20	Analog Power	—	—
Power and Ground Supplies (SATA PHY)				
SATA_RESREF	E4	Analog Power	—	—
SATA_VDDA_3P3	D4	Analog Power	—	—
SATA_VDDA_1P2	C5, D1, E2	Analog Power	—	—
SATA_VDDA_VREG	D5	Analog Power	—	—
SATA_PLL_VDDA1P2	E3	Analog Power	—	—
SATA_PLL_VSSA	D3	Analog Ground	—	—
SATA_RX_VSSA	A6, B4	Analog Ground	—	—
SATA_TX_VSSA	G1	Analog Ground	—	—

1 This pins should have an external pull-up resistor. Follow PCI specification and see System Design Information.

2 This pin contains an enabled internal Schmitt trigger.

3 These JTAG pins have internal pull-up P-FETs. This pin can not be configured.

4 This pin is an input only. This pin can not be configured.

5 This test pin must be tied to V_{SS}.

6 This pin is an input or open-drain output. This pin can not be configured. There is an internal pull-up resistor implemented.

NOTE

This table indicates only the pins with permananently enabled internal pull-up, pull-down, or Schmitt trigger. Most of the digital I/O pins can be configured to enable internal pull-up, pull-down, or Schmitt trigger. See the *MPC5121e Microcontroller Reference Manual*, IO Control chapter.

3 Electrical and Thermal Characteristics

3.1 DC Electrical Characteristics

3.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC5121e/MPC5123 DC Electrical characteristics. Table 4 gives the absolute maximum ratings.

Table 4. Absolute Maximum Ratings[1]

Characteristic	Symbol	Min	Max	Unit	SpecID
Supply voltage – e300 core and peripheral logic	V_{DD_CORE}	–0.3	1.47	V	D1.1
Supply voltage – I/O buffers	V_{DD_IO}, $V_{DD\_MEM\_IO}$	–0.3	3.6	V	D1.2
Input reference voltage (DDR/DDR2)	MVREF	–0.3	3.6	V	
Termination Voltage (DDR2)	MVTT	–0.3	3.6	V	
Supply voltage – System APLL, System Oscillator	SYS_PLL_AVDD	–0.3	3.6	V	D1.3
Supply voltage – e300 APLL	CORE_PLL_AVDD	–0.3	3.6	V	D1.4
Supply voltage – RTC (Hibernation)	VBAT_RTC	–0.3	3.6	V	D1.5
Supply voltage – FUSE Programming	AVDD_FUSEWR	–0.3	3.6	V	D1.6
Supply voltage – SATA PHY analog	SATA_VDDA_3P3	–0.3	3.6	V	D1.8
Supply voltage – SATA PHY voltage regulator	SATA_VDDA_VREG	–0.3	2.6	V	D1.9
Supply voltage – SATA PHY Tx/Rx	SATA_VDDA_1P2	–0.3	1.47	V	D1.10
Supply voltage – SATA PHY PLL	SATA_PLL_VDDA1P2	–0.3	1.47	V	D1.11
Supply voltage – USB PHY PLL and OSC	USB_PLL_PWR3	–0.3	3.6	V	D1.12
Supply voltage – USB PHY transceiver	USB_VDDA	–0.3	3.6	V	D1.13
Supply voltage – USB PHY bandgap bias	USB_VDDA_BIAS	–0.3	3.6	V	D1.14
Input voltage – USB PHY cable	USB_VBUS	–0.3	3.6	V	D1.15
Input voltage (V_{DD_IO})	Vin	–0.3	V_{DD_IO} + 0.3	V	D1.16
Input voltage ($V_{DD\_MEM\_IO}$)	Vin	–0.3	$V_{DD\_MEM\_IO}$ + 0.3	V	D1.17
Input voltage (VBAT_RTC)	Vin	–0.3	VBAT_RTC + 0.3	V	D1.18
Input voltage overshoot	Vinos	—	1	V	D1.19
Input voltage undershoot	Vinus	—	1	V	D1.20
Storage temperature range	Tstg	–55	150	^{o}C	D1.21

1 Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage.

3.1.2 Recommended Operating Conditions

Table 5 gives the recommended operating conditions.

Table 5. Recommended Operating Conditions

Characteristic	Symbol	Min[1]	Typ	Max[1]	Unit	SpecID
Supply voltage – e300 core and peripheral logic	V_{DD_CORE}	1.33	1.4	1.47	V	D2.1
State Retention voltage – e300 core and peripheral logic [2]		1.08	—	—	V	D2.2
Supply voltage – standard I/O buffers	V_{DD_IO}	3.0	3.3	3.6	V	D2.3
Supply voltage – memory I/O buffers (DDR)	$V_{DD\_MEM\_IO\_DDR}$	2.3	2.5	2.7	V	D2.4
Supply voltage – memory I/O buffers (DDR2, LPDDR)	$V_{DD\_MEM\_IO\_DDR2}$ $V_{DD\_MEM\_IO\_LPDDR}$	1.7	1.8	1.9	V	D2.5
Input Reference Voltage (DDR/DDR2)	MVREF	0.49 × $V_{DD\_MEM\_IO}$	0.50 × $V_{DD\_MEM\_IO}$	0.51 × $V_{DD\_MEM\_IO}$	V	D2.6
Termination Voltage (DDR2)	MVTT	MVREF – 0.04	MVREF	MVREF + 0.04	V	D2.7
Supply voltage – System APLL, System Oscillator	SYS_PLL_AVDD	3.0	3.3	3.6	V	D2.8
Supply voltage – e300 APLL	CORE_PLL_AVDD	3.0	3.3	3.6	V	D2.9
Supply voltage – RTC (Hibernation)[3]	VBAT_RTC	3.0	3.3	3.6	V	D2.10
Supply voltage – FUSE Programming	AVDD_FUSEWR	3.3		3.6	V	D2.11
Supply voltage – SATA PHY analog and OSC	SATA_VDDA_3P3	3.0	3.3	3.6	V	D2.13
Supply voltage – SATA PHY voltage regulator	SATA_VDDA_VREG	1.7		2.6	V	D2.14
Supply voltage – SATA PHY Tx/Rx	SATA_VDDA_1P2	1.14	1.2	1.47	V	D2.15
Supply voltage – SATA PHY PLL	SATA_PLL_VDDA1P2	1.33	1.4	1.47	V	D2.16
Supply voltage – USB PHY PLL and OSC	USB_PLL_PWR3	3.0	3.3	3.6	V	D2.17
Supply voltage – USB PHY transceiver	USB_VDDA	3.0	3.3	3.6	V	D2.18
Supply voltage – USB PHY bandgap bias	USB_VDDA_BIAS	3.0	3.3	3.6	V	D2.19
Input voltage – USB PHY cable	USB_VBUS	1.4	—	3.6	V	D2.20
Input voltage – standard I/O buffers	Vin	0	—	V_{DD_IO}	V	D2.21
Input voltage – memory I/O buffers (DDR)	Vin_{DDR}	0	—	$V_{DD\_MEM\_IO\_DDR}$	V	D2.22
Input voltage – memory I/O buffers (DDR2)	Vin_{DDR2}	0	—	$V_{DD\_MEM\_IO\_DDR2}$	V	D2.23
Input voltage – memory I/O buffers (LPDDR)	Vin_{LPDDR}	0	—	$V_{DD\_MEM\_IO\_LPDR}$	V	D2.24
Ambient operating temperature range	TA	–40	—	+85	°C	D2.25
Junction operating temperature range	TJ	–40	—	+125	°C	D2.26

1 These are recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

2 The State Retention voltage can be applied to V_{DD_CORE} after the device is placed in Deep-Sleep mode.

3 VBAT_RTC should not be supplied by a battery of voltage less than 3.0 V.

3.1.3 DC Electrical Specifications

Table 6 gives the DC Electrical characteristics for the MPC5121e/MPC5123 at recommended operating conditions.

Table 6. DC Electrical Specifications

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input high voltage	Input type = TTL V_{DD_IO}	V_{IH}	0.51 × V_{DD_IO}	—	V	D3.1
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR}$	V_{IH}	MVREF + 0.15	—	V	D3.2
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR2}$	V_{IH}	MVREF + 0.125	—	V	D3.3
Input high voltage	Input type = TTL $V_{DD\_MEM\_IO\_LPDDR}$	V_{IH}	0.7 × $V_{DD\_MEM\_IO\_LPDDR}$	—	V	D3.4
Input high voltage	Input type = PCI V_{DD_IO}	V_{IH}	0.5 × V_{DD_IO}	—	V	D3.5
Input high voltage	Input type = Schmitt V_{DD_IO}	V_{IH}	0.65 × V_{DD_IO}	—	V	D3.6
Input high voltage	SYS_XTALI crystal mode[1] Bypass mode[2]	CV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.7
Input high voltage	SATA_XTALI crystal mode Bypass mode	SV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.8
Input high voltage	USB_XTALI crystal mode Bypass mode	UV_{IH}	Vxtal + 0.4V (V_{DD_IO}/2) + 0.4V	—	V	D3.9
Input high voltage	RTC_XTALI crystal mode[3] Bypass mode[4]	RV_{IH}	(VBAT_RTC/5) + 0.5V (VBAT_RTC/2) + 0.4V	—	V	D3.10
Input low voltage	Input type = TTL V_{DD_IO}	V_{IL}	—	0.42 × V_{DD_IO}	V	D3.11
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR}$	V_{IL}	—	MVREF – 0.15	V	D3.12
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_DDR2}$	V_{IL}	—	MVREF – 0.125	V	D3.13
Input low voltage	Input type = TTL $V_{DD\_MEM\_IO\_LPDDR}$	V_{IL}	—	0.3 × $V_{DD\_MEM\_IO\_LPDDR}$	V	D3.14
Input low voltage	Input type = PCI V_{DD_IO}	V_{IL}	—	0.3 × V_{DD_IO}	V	D3.15
Input low voltage	Input type = Schmitt V_{DD_IO}	V_{IL}	—	0.35 × V_{DD_IO}	V	D3.16
Input low voltage	SYS_XTALI crystal mode Bypass mode	CV_{IL}	—	Vxtal – 0.4 (V_{DD_IO}/2) – 0.4	V	D3.17
Input low voltage	SATA_XTALI crystal mode Bypass mode	SV_{IL}	—	Vxtal – 0.4 V (V_{DD_IO}/2) – 0.4	V	D3.18
Input low voltage	USB_XTALI crystal mode Bypass mode	UV_{IL}	—	Vxtal – 0.4 (V_{DD_IO}/2) – 0.4	V	D3.19
Input low voltage	RTC_XTALI crystal mode Bypass mode	RV_{IL}	—	(VBAT_RTC/5) – 0.5 (VBAT_RTC/2) – 0.4	V	D3.20
Input leakage current	Vin = 0 or V_{DD_IO}/$V_{DD\_MEM\_IO\_DDR/2}$ (depending on input type)[5]	I_{IN}	–2.5	2.5	µA	D3.21
Input leakage current	SYS_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	20	µA	D3.22

Table 6. DC Electrical Specifications (continued)

Characteristic	Condition	Symbol	Min	Max	Unit	SpecID
Input leakage current	RTC_XTALI Vin = 0 or V_{DD_IO}	I_{IN}	—	1.0	µA	D3.23
Input current, pullup resistor[6]	Pullup V_{DD_IO} Vin = VIL	I_{INpu}	25	150	µA	D3.24
Input current, pulldown resistor [8]	Pulldown V_{DD_IO} Vin = VIH	I_{INpd}	25	150	µA	D3.25
Output high voltage	IOH is driver dependent[7] V_{DD_IO}	V_{OH}	0.8 × V_{DD_IO}	—	V	D3.26
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OHDDR}	1.90	—	V	D3.27
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OHDDR2}	1.396	—	V	D3.28
Output high voltage	IOH is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OHLPDDR}$	$V_{DD\_MEM\_IO}$ – 0.28	—	V	D3.28
Output low voltage	IOL is driver dependent[7] V_{DD_IO}	V_{OL}	—	0.2 × V_{DD_IO}	V	D3.30
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR}$	V_{OLDDR}	—	0.36	V	D3.31
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_DDR2}$	V_{OLDDR2}	—	0.28	V	D3.32
Output low voltage	IOL is driver dependent[7] $V_{DD\_MEM\_IO\_LPDDR}$	$V_{OLLPDDR}$	—	0.28	V	D3.33
Differential cross point voltage (DDR MCK/$\overline{\text{MCK}}$)	—	V_{OXMCK}	0.5 × $V_{DD\_MEM\_IO}$ – 0.125	0.5 × $V_{DD\_MEM\_IO}$ + 0.125	V	D3.34
DC Injection Current Per Pin[8]	—	I_{CS}	–1.0	1.0	mA	D3.35
Input Capacitance (digital pins)	—	C_{in}	—	7	pF	D3.36
Input Capacitance (analog pins)	—	C_{in}	—	10	pF	D3.37
On Die Termination (DDR2)	—	R_{ODT}	120	180	Ω	D3.38

1 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, Vextal – Vxtal - 400mV criteria has to be met for oscillator's comparator to produce output clock.

2 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the EXTAL pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

3 This parameter is meant for those who do not use quartz crystals or resonators, but CAN osc, in crystal mode. In that case, drive one of the XTAL_IN or XTAL_OUT pins not connecting anything to other pin for the oscillator's comparator to produce output clock.

4 This parameter is meant for those who do not use quartz crystals or resonators, but signal generator clock to drive, in bypass mode. In that case, drive only the xtal_in pin not connecting anything to other pin for the oscillator's comparator to produce output clock.

5 Leakage current is measured with output drivers disabled and pull-up/pull-downs inactive.

6 Pullup current is measured at VIL and pulldown current is measured at VIH.

7 See Table 7 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 3.

8 All injection current is transferred to $V_{DD\_IO}/V_{DD\_MEM\_IO}$. An external load is required to dissipate this current to maintain the power supply within the specified voltage range.
Total injection current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.

Table 7. I/O Pads—Drive Current, Slew Rate

Pad Type	Supply Voltage	Drive Select/Slew Rate Control	Rise time max (ns)	Fall time max (ns)	Current Ioh (mA)	Current Iol (mA)	SpecID
General IO	V_{DD_IO} = 3.3V	configuration 3 (11)	1.4	1.6	35	35	D3.41
		configuration 2 (10)	9.8	12			D3.42
		configuration 1 (01)	19	24			D3.43
		configuration 0 (00)	140	183			D3.44
DDR	$V_{DD\_MEM\_IO}$ = 2.5V (DDR)	configuration 3 (011)	2	2	16.2	16.2	D3.45
	$V_{DD\_MEM\_IO}$ = 1.8V (LPDDR)	configuration 0 (000)	1	1	4.6	4.6	D3.46
		configuration 1 (001)			8.1	8.1	D3.47
	$V_{DD\_MEM\_IO}$ = 1.8V (DDR2)	configuration 2 (010)	1	1	5.3	5.3	D3.48
		configuration 6 (110)			13.4	13.4	D3.49
PCI	V_{DD_IO} = 3.3V	configuration 1 (1)	1.4	1.4	11	17	D3.50
		configuration 0 (0)	2	2			D3.51

Notes:
1. General IO – Rise and Fall Times at Drive load 50pF.
2. PCI – Rise and Fall Times at Drive load 10pF.
3. DDR – for LPDDR/Mobile-DDR, slew rate is measured between 20% of $V_{DD\_MEM\_IO}$ and 80% of $V_{DD\_MEM\_IO}$.
4. DDR – for DDR, DDR2, rising signals, slew rate is measured between $V_{DD\_MEM\_IO}$ × 0.5 and ViH_{AC}. For falling signals, slew rate is measured between $V_{DD\_MEM\_IO}$ × 0.5 and ViL_{AC}.
5. DDR – Rise and Fall Times terminated at the destination with 50 ohm to MVTT (0.5 × $V_{DD\_MEM\_IO}$), with 4 pF representing the DDR input capacitance.

3.1.4 Electrostatic Discharge

CAUTION

This device contains circuitry that protects against damage due to high-static voltage or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages. Operational reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (GND or VDD). Table 10 gives package thermal characteristics for this device.

Table 8. ESD and Latch-Up Protection Characteristics

Symbol	Rating	Min	Max	Unit	SpecID
V_{HBM}	Human Body Model (HBM) – JEDEC JESD22-A114-B	2000	—	V	D4.1
V_{MM}	Machine Model (MM) – JEDEC JESD22-A115	200	—	V	D4.2
V_{CDM}	Charge Device Model (CDM) – JEDEC JESD22-C101	500	—	V	D4.3

3.1.5 Power Dissipation

Power dissipation of the MPC5121e/MPC5123 is caused by 4 different components: the dissipation of the internal or core digital logic (supplied by $V_{DD\_CORE)}$, the dissipation of the analog circuitry (supplied by SYS_PLL_AVDD and CORE_PLL_AVDD), the dissipation of the IO logic (supplied by $V_{DD\_MEM\_IO}$ and V_{DD_IO}) and the dissipation of the PHYs (supplied by own supplies). Table 9 details typical measured core and analog power dissipation figures for a range of operating modes. However, the dissipation due to the switching of the IO pins can not be given in general, but must be calculated for each application case using the following formula:

$$P_{IO} = P_{IOint} + \sum_{M} N \times C \times VDD\_IO^2 \times f \qquad \textit{Eqn. 1}$$

where N is the number of output pins switching in a group M, C is the capacitance per pin, V_{DD_IO} is the IO voltage swing, f is the switching frequency and P_{IOint} is the power consumed by the unloaded IO stage. The total power consumption of the device must not exceed the value that would cause the maximum junction temperature to be exceeded.

$$P_{total} = P_{core} + P_{analog} + P_{IO} + PPHYs \qquad \textit{Eqn. 2}$$

Table 9. Power Dissipation

Core Power Supply (V_{DD_CORE})			SpecID
Mode	High-Performance	Unit	
	e300 = 300 MHz, CSB = 200 MHz		
Operational[1]	800	mW	D5.1
Deep-Sleep[1]	1	mW	D5.2
Hibernation	20	uW	D5.3
PLL/OSC Power Supplies (SYS_PLL_AVDD, CORE_PLL_AVDD)			
Typical	25	mW	D5.4
Unloaded I/O Power Supplies (V_{DD_IO}, $V_{DD\_MEM\_IO}$)			

Table 9. Power Dissipation (continued)

Core Power Supply (V_{DD_CORE})			SpecID
Mode	High-Performance	Unit	
	e300 = 300 MHz, CSB = 200 MHz		
Typical	300	mW	D5.5
PHY Power Supplies (USB_VDDA, SATA_VDDA)			
Typical	200	mW	D5.6

1 Typical core power is measured at V_{DD_CORE} = 1.4 V, T_j = 25 °C.

NOTE

The maximum power depends on the supply voltage, process corner, junction temperature, and the concrete application and clock configurations.
The worst case power consumption could reach a maximum of 2000 mW.

3.1.6 Thermal Characteristics

Table 10. Thermal Resistance Data

Rating	Board Layers	Symbol	TEPBGA	TEPBGA 2	Value	Unit	SpecID
Junction to Ambient Natural Convection[1,2]	Single layer board (1s)	$R_{\theta JA}$	31	24	30	°C/W	D6.1
Junction to Ambient Natural Convection[1,3]	Four layer board (2s2p)	$R_{\theta JMA}$	22	17	22	°C/W	D6.2
Junction to Ambient (@200 ft/min)[1,3]	Single layer board (1s)	$R_{\theta JMA}$	25	19	24	°C/W	D6.3
Junction to Ambient (@200 ft/min)[1,3]	Four layer board (2s2p)	$R_{\theta JMA}$	19	14	19	°C/W	D6.4
Junction to Board[4]	—	$R_{\theta JB}$	14	9	14	°C/W	D6.5
Junction to Case[5]	—	$R_{\theta JC}$	9	7	8	°C/W	D6.6
Junction to Package Top[6]	Natural Convection	Ψ_{JT}	2	7	2	°C/W	D6.7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.1.6.1 Heat Dissipation

An estimation of the chip-junction temperature, T_J, can be obtained from the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \text{Eqn. 3}$$

where:

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
P_D = power dissipation in package (W)

The junction to ambient thermal resistance is an industry standard value, which provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board, and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is correct depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

Historically, the thermal resistance has frequently been expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 4}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction to case thermal resistance (°C/W)
$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the air flow around the device, add a heat sink, change the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for ceramic packages with heat sinks where some 90% of the heat flow is through the case to the heat sink to ambient. For most packages, a better model is required.

A more accurate thermal model can be constructed from the junction to board thermal resistance and the junction to case thermal resistance. The junction to case covers the situation where a heat sink is used or where a substantial amount of heat is dissipated from the top of the package. The junction to board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used for hand estimations or for a computational fluid dynamics (CFD) thermal model.

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \text{Eqn. 5}$$

where:

T_T = thermocouple temperature on top of package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned, so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over approximately one mm of wire extending

from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.2 Oscillator and PLL Electrical Characteristics

The MPC5121e/MPC5123 System requires a system-level clock input SYS_XTALI. This clock input may be driven directly from an external oscillator or with a crystal using the internal oscillator.

There is a separate oscillator for the independent Real Time Clock (RTC) system.

The MPC5121e/MPC5123 clock generation uses two phase locked loop (PLL) blocks.

- The system PLL (SYS_PLL) takes an external reference frequency and generates the internal system clock. The system clock frequency is determined by the external reference frequency and the settings of the SYS_PLL configuration.
- The e300 core PLL (CORE_PLL) generates a master clock for all of the CPU circuitry. The e300 core clock frequency is determined by the system clock frequency and the settings of the CORE_PLL configuration.

The USB PHY contains its own oscillator with the input USB_XTALI and an embedded PLL.

The SATA PHY contains its own oscillator with the input SATA_XTALI and an embedded PLL.

3.2.1 System Oscillator Electrical Characteristics

Table 11. System Oscillator Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
SYS_XTALI frequency	f_{sys_xtal}	15.6	33.3	35.0	MHz	O1.1

The system oscillator can work in oscillator mode or in bypass mode to support an external input clock as clock reference.

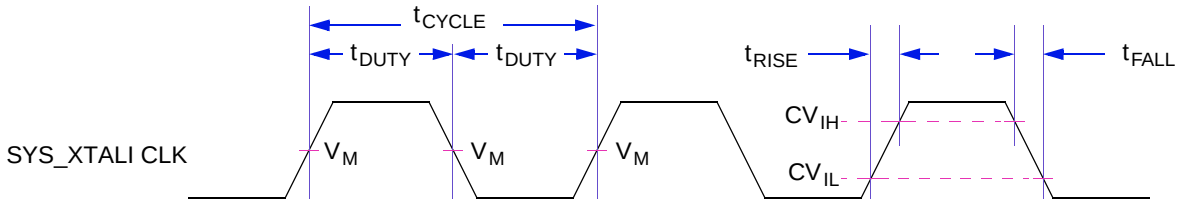

Figure 3. Timing Diagram—SYS_XTALI

Table 12. SYS_XTALI Timing

Sym	Description	Min	Max	Units	SpecID
t_{CYCLE}	SYS_XTALI cycle time[1, 2]	64.1	28.57	ns	O.1.2
t_{RISE}	SYS_XTALI rise time[3]	1	4	ns	O.1.3
t_{FALL}	SYS_XTALI fall time[4]	1	4	ns	O.1.4
t_{DUTY}	SYS_XTALI duty cycle[5]	40	60	%	O.1.5

1 The SYS_XTALI frequency and system PLL settings must be chosen such that the resulting system frequencies do not exceed their respective maximum or minimum operating frequencies. See the *MPC5121e Microcontroller Reference Manual*.

2 The MIN/Max cycle times are calculated using $1/f_{sys\_xtal\ (MIN/MAX)}$ where the $f_{sys\_xtal\ (MIN/MAX)}$ (15.6/35 MHz) are taken from Table 11.

3 Rise time is measured from 20% of vdd to 80% of V_{DD}.

4 Fall time is measured from 20% of vdd to 80% of V_{DD}.
5 SYS_XTALI duty cycle is measured at V_M.

3.2.2 RTC Oscillator Electrical Characteristics

Table 13. RTC Oscillator Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
RTC_XTALI frequency	f_{rtc_xtal}	—	32.768	—	kHz	O2.1

3.2.3 System PLL Electrical Characteristics

Table 14. System PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
Sys PLL input clock frequency[1]	f_{sys_xtal}	16	33.3	67	MHz	O3.1
Sys PLL input clock jitter[2]	t_{jitter}	—	—	10	ps	O3.2
Sys PLL VCO frequency[1]	f_{VCOsys}	400	—	800	MHz	O3.3
Sys PLL VCO output jitter (Dj), peak to peak / cycle	$f_{VCOjitterDj}$	—	—	40	ps	O3.4
Sys PLL VCO output jitter (Rj), RMS 1 sigma	$f_{VCOjitterRj}$	—	—	12	ps	O3.5
Sys PLL relock time—after power up[3]	t_{lock1}	—	—	200	µs	O3.6
Sys PLL relock time—when power was on[4]	t_{lock2}	—	—	170	µs	O3.7

1 The SYS_XTALI frequency and PLL Configuration bits must be chosen such that the resulting system frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.
2 This represents total input jitter—short term and long term combined. Two different types of jitter can exist on the input to CORE_SYSCLK, systemic and true random jitter. True random jitter is rejected. Systemic jitter is passed into and through the PLL to the internal clock circuitry.
3 PLL relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence.
4 PLL relock time is the maximum amount of time required for the PLL lock after the PLL has been disabled and subsequently re-enabled during sleep modes.

3.2.4 e300 Core PLL Electrical Characteristics

The internal clocking of the e300 core is generated from and synchronized to the system clock by means of a voltage-controlled core PLL.

Table 15. e300 PLL Specifications

Characteristic	Symbol	Min	Typical	Max	Unit	SpecID
e300 frequency[1]	f_{core}	200	—	400	MHz	O4.1
e300 PLL VCO frequency[1]	$f_{VCOcore}$	400	—	800	MHz	O4.3
e300 PLL input clock frequency	f_{CSB_CLK}	50	—	200	MHz	O4.4
e300 PLL input clock cycle time	t_{CSB_CLK}	5	—	20	ns	O4.5
e300 PLL relock time[2]	t_{lock}	—	—	200	µs	O4.6

1 The frequency and e300 PLL Configuration bits must be chosen such that the resulting system frequencies, CPU (core) frequency, and e300 PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies in Table 16. There is a hard coded relationship between f_{core} and $f_{VCOcore}$ ($f_{core} = f_{VCOcore}/2$).

2 PLL relock time is the maximum amount of time required for the PLL lock after a stable VDD and CORE_SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep modes.

3.3 AC Electrical Characteristics

3.3.1 Overview

Hyperlinks to the indicated timing specification sections are provided in the following:

- AC Operating Frequency Data
- Resets
- External Interrupts
- SDRAM (DDR)
- PCI
- LPC
- NFC
- PATA
- SATA PHY
- FEC
- USB ULPI
- On-Chip USB PHY
- SDHC
- DIU
- SPDIF
- CAN
- I^2C
- J1850
- PSC
- GPIOs and Timers
- Fusebox
- IEEE 1149.1 (JTAG)
- VIU

AC Test Timing Conditions:

Unless otherwise noted, all test conditions are as follows:

- T_A = –40 to 85 ^oC
- V_{DD_CORE} = 1.33 to 1.47 V
  V_{DD_IO} = 3.0 to 3.6 V
- Input conditions:
  All Inputs: tr, tf ≤ 1 ns
- Output Loading:
  All Outputs: 50 pF

3.3.2 AC Operating Frequency Data

Table 16 provides the operating frequency information for the MPC5121e/MPC5123.

Table 16. Clock Frequencies

	Min	Max	Units	SpecID
e300 Processor Core	200	400	MHz	A1.1
SDRAM Clock	28.6	200	MHz	A1.2
CSB Bus Clock	50.0	200	MHz	A1.3
IP Bus Clock	8.3	83	MHz	A1.4
PCI Clock	4.43	66	MHz	A1.5
LPC Clock	2.08	83	MHz	A1.6

Table 16. Clock Frequencies (continued)

	Min	Max	Units	SpecID
NFC Clock	2.08	83	MHz	A1.7
DIU Clock	0.78	100	MHz	A1.8
SDHC Clock	0.78	66.6	MHz	A1.9
MBX Clock	6.25	100	MHz	A1.10

NOTES:

1. The SYS_XTALI frequency, Sys PLL, and CORE PLL settings must be chosen so that the resulting e300 clk, csb_clk, MCK, frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The values are valid for the user operation mode. There can be deviations for test modes.
3. The selection of the peripheral clock frequencies needs to take care about requirements for baud rates and minimum frequency limitation.

4.The DDR data rate is 2× the DDR memory bus frequency.

See the *MPC5121e Microcontroller Reference Manual* for more information on the clock subsystem.

3.3.3 Resets

The MPC5121e/MPC5123 has three reset pins:

- $\overline{\text{PORESET}}$—Power on Reset
- $\overline{\text{HRESET}}$—Hard Reset
- $\overline{\text{SRESET}}$—Software Reset

These signals are asynchronous I/O signals and can be asserted at any time. The input side uses a Schmitt trigger and requires the same input characteristics as other MPC5121e/MPC5123 inputs, as specified in Section 3.1, "DC Electrical Characteristics."

As long as V_{DD} is not stable the $\overline{\text{HRESET}}$ output is not stable.

Table 17. Reset Rise / Fall Timing

Description	Min	Max	Unit	SpecID
$\overline{\text{PORESET}}$[1] fall time	—	1	ms	A3.4
$\overline{\text{PORESET}}$ rise time	—	1	ms	A3.5
$\overline{\text{HRESET}}$[2,3] fall time	—	1	ms	A3.6
$\overline{\text{HRESET}}$ rise time	—	1	ms	A3.7
$\overline{\text{SRESET}}$ fall time	—	1	ms	A3.8
$\overline{\text{SRESET}}$ rise time	—	1	ms	A3.9

1 Make sure that the $\overline{\text{PORESET}}$ does not carry any glitches. The MPC5121e/MPC5123 has no filter to prevent them from getting into the chip.

2 $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ must have a monotonous rise time.

3 The assertion of $\overline{\text{HRESET}}$ becomes active at Power on Reset without any SYS_XTALI clock.

The timing relationship is shown in Figure 4.

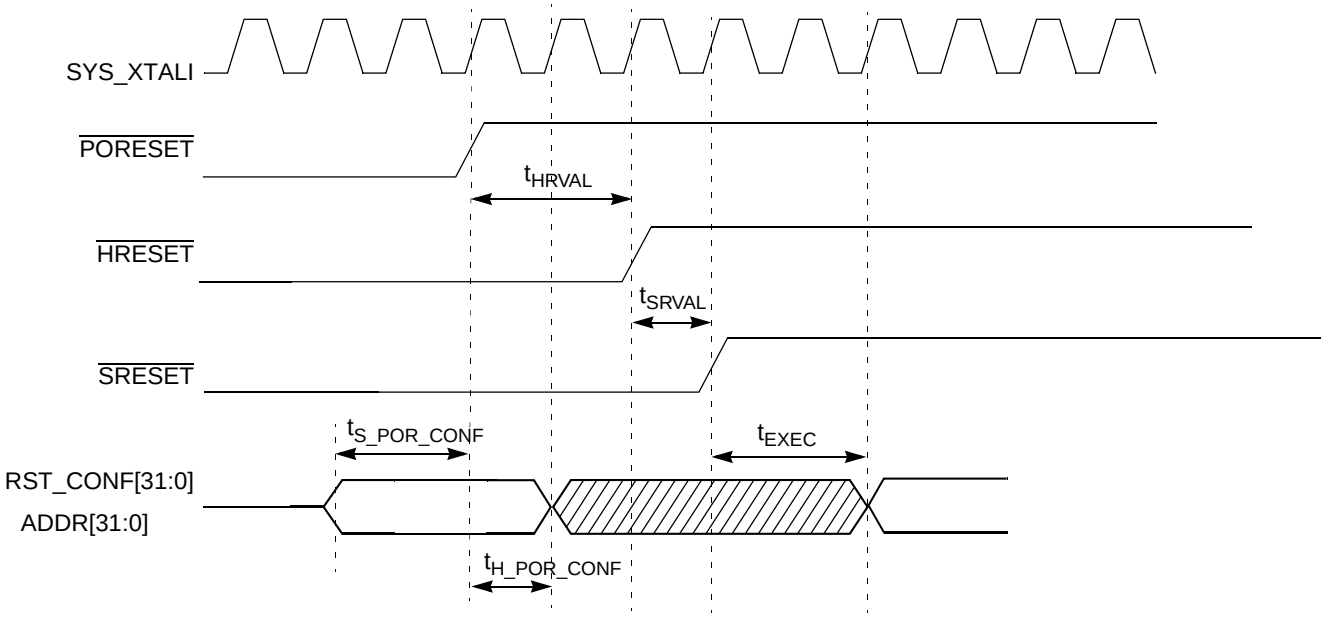

Figure 4. Power-Up Behavior

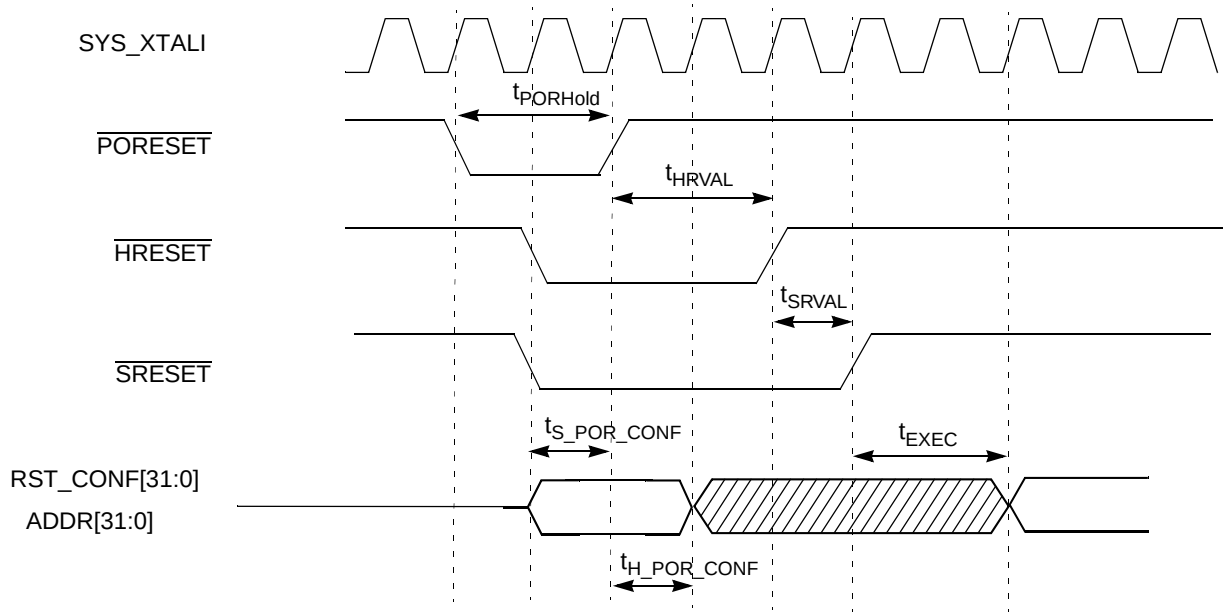

Figure 5. Power-On Reset Behavior

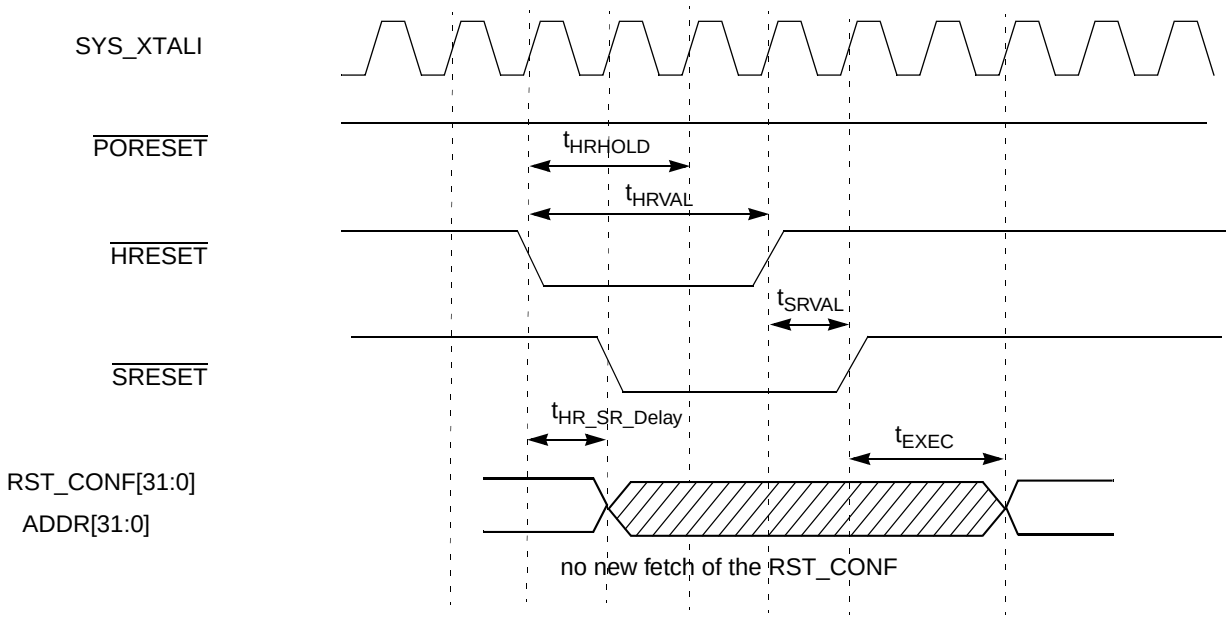

Figure 6. HRESET Behavior

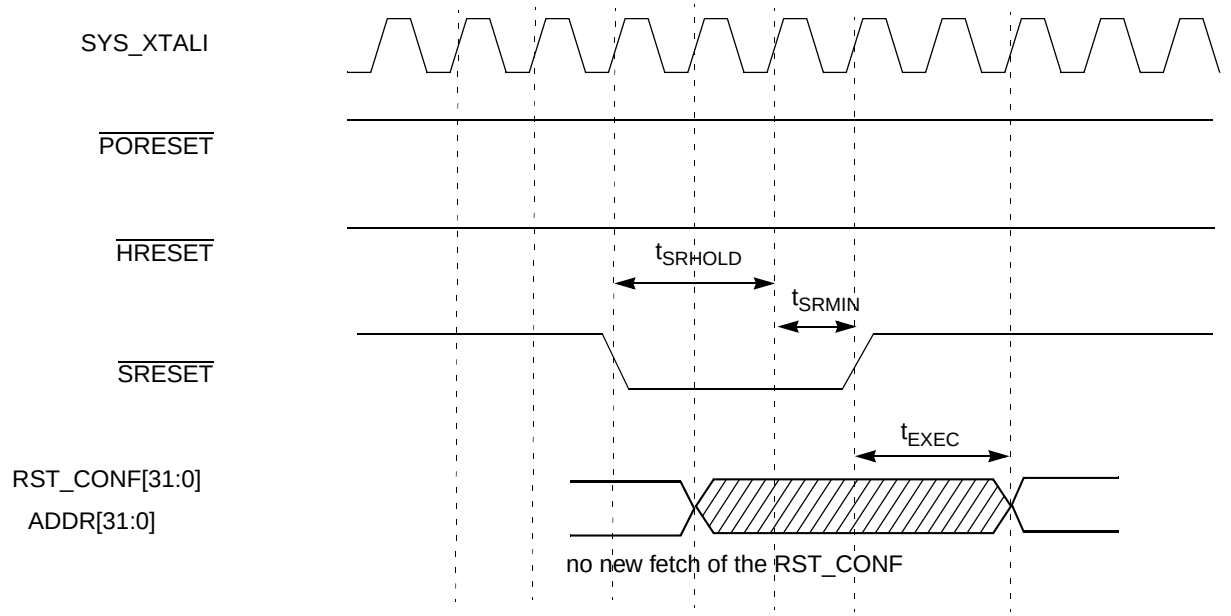

Figure 7. SRESET Behavior

Table 18. Reset Timing

Symbol	Description	Value SYS_XTALI	SpecID
$t_{PORHOLD}$	Time $\overline{\text{PORESET}}$ must be held low before a qualified reset occurs	4 cycles	A3.10
t_{HRVAL}	Time $\overline{\text{HRESET}}$ is asserted after a qualified reset occurs	26810 cycles	A3.11
t_{SRVAL}	Time $\overline{\text{SRESET}}$ is asserted after assertion of $\overline{\text{HRESET}}$	32 cycles	A3.12
t_{EXEC}	Time between $\overline{\text{SRESET}}$ assertion and first core instruction fetch	4 cycles	A3.13

Table 18. Reset Timing (continued)

Symbol	Description	Value SYS_XTALI	SpecID
$t_{S\_POR\_CONF}$	Reset configuration setup time before assertion of $\overline{\text{PORESET}}$	1 cycle	A3.14
$t_{H\_POR\_CONF}$	Reset configuration hold time after assertion of $\overline{\text{PORESET}}$	1 cycle	A3.15
$t_{HR\_SR\_DELAY}$	Time from falling edge of HRESET to falling edge of SRESET	4 cycles	A3.16
t_{HRHOLD}	Time $\overline{\text{HRESET}}$ must be held low before a qualified reset occurs	4 cycles	A3.17
t_{SRHOLD}	Time $\overline{\text{SRESET}}$ must be held low before a qualified reset occurs	4 cycles	A3.18
t_{SRMIN}	Time $\overline{\text{SRESET}}$ is asserted after it has been qualified	1 cycles	A3.19

3.3.4 External Interrupts

The MPC5121e/MPC5123 provides three different kinds of external interrupts:

- IRQ interrupts
- GPIO interrupts with simple interrupt capability (not available in power-down mode)
- WakeUp interrupts

Table 19. IPIC Input AC Timing Specifications[1]

Description	Symbol	Min	Unit	SpecID
IPIC inputs—minimum pulse witdh	t_{PICWID}	2T	ns	A4.1

1 T is the IP bus clock cycle. T = 12 ns is the minimum value (for the maximum IP bus freqency of 83 MHz).

IPIC inputs must be valid for at least tPICWID to ensure proper operation in edge triggered mode.

3.3.5 SDRAM (DDR)

The MPC5121e/MPC5123 memory controller supports three types of DDR devices:

- DDR-1 (SSTL_2 class II interface)
- DDR-2 (SSTL_18 interface)
- LPDDR/Mobile-DDR (1.8V I/O supply voltage)

JEDEC standards define the minimum set of requirements for complient memory devices:

- JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2C, May 2006
- JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79E, May 2005
- JEDEC STANDARD, Low Power Double Data Rate (LPDDR) SDRAM Specification, JESD79-4, May 2006

The MPC5121e/MPC5123 supports the configuration of two output drive strengths for DDR2 and LPDDR:

- Full drive strength
- Half drive strengh (intended for ligther loads or point-to-point environments)

The MPC5121e/MPC5123 memory controller supports dynamic on-die termination in the host device and in the DDR2 memory device.

This section includes AC specifications for all DDR SDRAM pins. The DC parameters are specified in the DC Electrical Characteristics.

3.3.5.1 DDR and DDR2 SDRAM AC Timing Specifications

Table 20. DDR and DDR2 (DDR2-400) SDRAM Timing Specifications

At recommended operating conditions with $V_{DD\_MEM\_IO}$ of ±5%

Parameter	Symbol	Min	Max	Unit	Notes	SpecID
Clock cycle time, CL=x	t_{CK}	5000	—	ps		A5.1
CK HIGH pulse width	t_{CH}	0.47	0.53	t_{CK}	1,2	A5.3
CK LOW pulse width	t_{CL}	0.47	0.53	t_{CK}	1,2	A5.4
Skew between MCK and DQS transitions	t_{DQSS}	–0.25	0.25	t_{CK}	2, 3	A5.5
Address and control output setup time relative to MCK rising edge	$t_{OS(base)}$	(t_{CK}/2 – 750)	—	ps	2, 3	A5.6
Address and control output hold time relative to MCK rising edge	$t_{OH(base)}$	(t_{CK}/2 – 750)	—	ps	2, 3	A5.7
DQ and DM output setup time relative to DQS	$t_{DS1(base)}$	(t_{CK}/4 – 500)	—	ps	2, 3	A5.8
DQ and DM output hold time relative to DQS	$t_{DH1(base)}$	(t_{CK}/4 – 500)	—	ps	2, 3	A5.9
DQS-DQ skew for DQS and associated DQ inputs	t_{DQSQ}	–(t_{CK}/4 – 600)	(t_{CK}/4 – 600)	ps	2	A5.10
DQS window start position related to CAS read command	t_{DQSEN}	TBD	TBD	ps	1,2,3,4,5	A5.11

1 Measured with clock pin loaded with differential 100 termination resistor.

2 All transitions measured at mid-supply (VDD_MEM_IO/2).

3 Measured with all outputs except the clock loaded with 50 Ω termination resistor to $V_{DD\_MEM\_IO}$/2.

4 In this window, the first rising edge of DQS should occur. From the start of the window to DQS rising edge, DQS should be low.

5 Window position is given for t_{DQSEN} = 2.0 t_{CK}. For other values of t_{DQSEN}, window position is shifted accordingly.

Figure 8 shows the DDR SDRAM write timing.

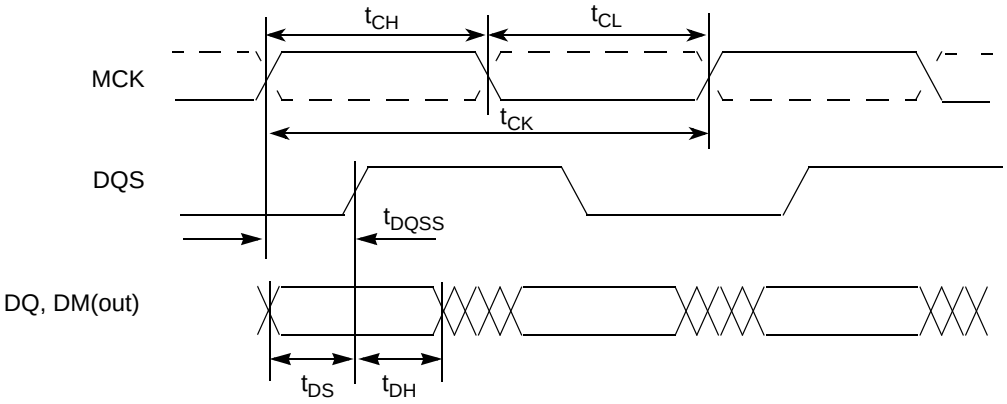

Figure 8. DDR Write Timing

Figure 9 and Figure 10 shows the DDR SDRAM read timing.

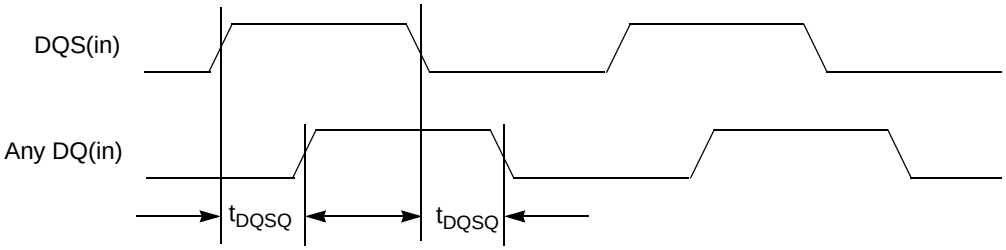

Figure 9. DDR Read Timing, DQ vs DQS

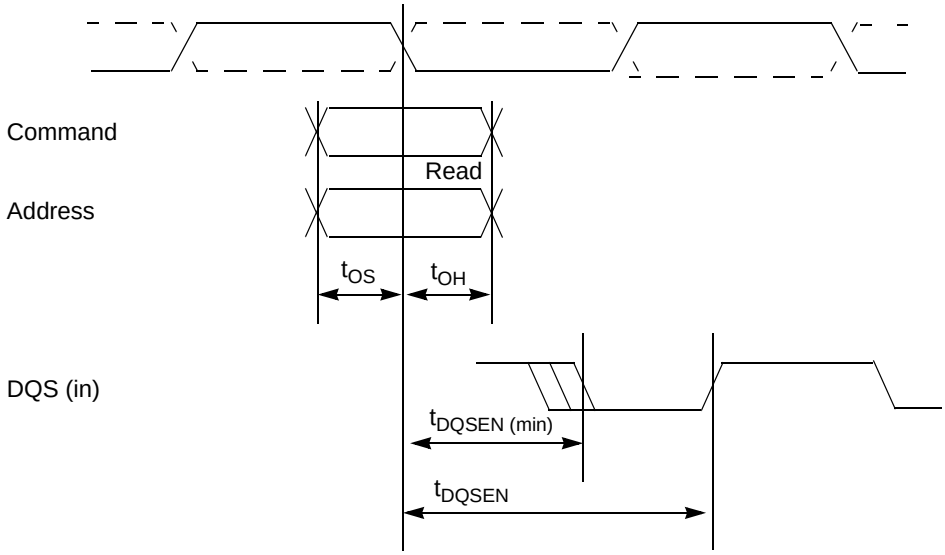

Figure 10. DDR Read Timing, DQSEN

Figure 11 provides the AC test load for the DDR bus.

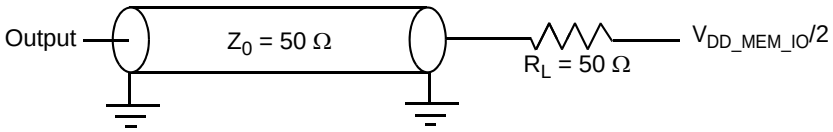

Figure 11. DDR AC Test Load

3.3.6 PCI

The PCI interface on the MPC5121e/MPC5123 is designed to PCI Version 2.3 and supports 33 and 66 MHz PCI operations. See the PCI Local Bus Specification; the component section specifies the electrical and timing parameters for PCI components with the intent that components connect directly together whether on the planar or an expansion board, without any external buffers or other glue logic. Parameters apply at the package pins, not at expansion board edge connectors.

The PCI_CLK is used as output clock, the MPC5121e/MPC5123 is a PCI host device only.

Figure 12 shows the clock waveform and required measurement points for 3.3 V signaling environments. Table 21 summarizes the clock specifications.

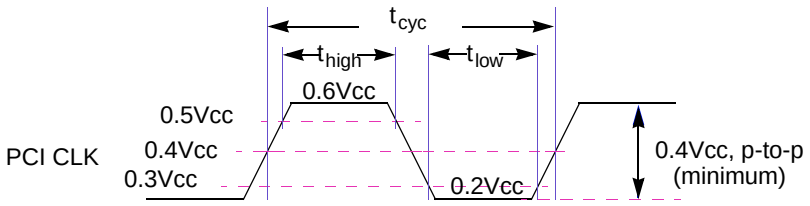

Figure 12. PCI CLK Waveform

Table 21. PCI CLK Specifications

Sym	Description	66 MHz[1]		33 MHz		Units	SpecID
		Min[2]	Max	Min	Max		
t_{cyc}	PCI CLK Cycle Time[1,3]	15	30	30	—	ns	A6.1
t_{high}	PCI CLK High Time	6	—	11	—	ns	A6.2
t_{low}	PCI CLK Low Time	6	—	11	—	ns	A6.3
—	PCI CLK Slew Rate[2]	1.5	4	1	4	V/ns	A6.4

1 In general, all 66 MHz PCI components must work with any clock frequency up to 66 MHz. CLK requirements vary depending upon whether the clock frequency is above 33 MHz.

2 Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 12.

3 The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

Table 22. PCI Timing Parameters[1]

Sym	Description	66 MHz		33 MHz		Units	SpecID
		Min[2]	Max	Min	Max		
t_{val}	CLK to Signal Valid Delay – bused signals[1,2,3]	2	6	2	11	ns	A6.5
t_{val}(ptp)	CLK to Signal Valid Delay – point to point[1,2,3]	2	6	2	12	ns	A6.6
t_{on}	Float to Active Delay[1]	2	—	2	—	ns	A6.7
t_{off}	Active to Float Delay[1]		14		28	ns	A6.8
t_{su}	Input Setup Time to CLK – bused signals[3,4]	3	—	7	—	ns	A6.9
t_{su}(ptp)	Input Setup Time to CLK – point to point[3,4]	5	—	10,12	—	ns	A6.10
t_h	Input Hold Time from CLK[4]	0	—	0	—	ns	A6.11

1 See the timing measurement conditions in the PCI Local Bus Specification. It is important that all driven signal transitions drive to their Voh or Vol level within one Tcyc.

2 Minimum times are measured at the package pin with the load circuit, and maximum times are measured with the load circuit as shown in the PCI Local Bus Specification.

3 REQ# and GNT# are point-to-point signals and have different input setup times than do bused signals. GNT# and REQ# have a setup of 5 ns at 66 MHz. All other signals are bused.

[4] See the timing measurement conditions in the PCI Local Bus Specification.

For Measurement and Test Conditions, see the PCI Local Bus Specification.

3.3.7 LPC

The Local Plus Bus is the external bus interface of the MPC5121e/MPC5123. A maximum of eight configurable chip selects (CS) are provided. There are two main modes of operation: non-MUXed and MUXED. The reference clock is the LPC CLK. The maximum bus frequency is 83 MHz.

Definition of Acronyms and Terms:

WS = Wait State
DC = Dead Cycle
HC = Hold Cycle
DS = Data Size in Bytes
BBT = Burst Bytes per Transfer
AL = Address latch enable Length
ALT = Chip select/Address Latch Timing
t_{LPCck} = LPC clock period

Table 23. LPC Timing

Sym	Description	Min	Max	Units	SpecID
t_{OD}	$\overline{CS}$[x], ADDR, R/$\overline{W}$, TSIZ, DATA (wr), $\overline{TS}$, $\overline{OE}$ valid after LPC CLK (Output Delay related to LPC CLK)	0	5	ns	A7.1
t_1	Non-MUXed non-Burst $\overline{CS}$[x] pulse width	(2 + WS) × t_{LPCck}	(2 + WS) × t_{LPCck}	ns	A7.2
t_2	ADDR, R/$\overline{W}$, TSIZ, DATA (wr) valid before $\overline{CS}$[x] assertion	$t_{LPCck} - t_{OD}$	$t_{LPCck} + t_{OD}$	ns	A7.3
t_3	$\overline{OE}$ assertion after $\overline{CS}$[x] assertion	$t_{LPCck} - t_{OD}$	$t_{LPCck} + t_{OD}$	ns	A7.4
t_4	ADDR, R/$\overline{W}$, TSIZ, Data (wr) hold after $\overline{CS}$[x] negation	$t_{LPCck} - t_{OD}$	(HC + 1) × t_{LPCck} + t_{OD}	ns	A7.5
t_5	$\overline{TS}$ pulse width	t_{LPCck}	t_{LPCck}	ns	A7.6
t_6	DATA (rd) setup before LPC CLK	4	—	ns	A7.7
t_7	DATA (rd) input hold	0	(DC + 1) × t_{LPCck}	ns	A7.8
t_8	Non-MUXed read Burst $\overline{CS}$[x] pulse width	(2 + WS + BBT/DS) × t_{LPCck}	(2 + WS + BBT/DS) × t_{LPCck}	ns	A7.9
t_9	Burst $\overline{ACK}$ pulse width	(BBT/DS) × t_{LPCck}	(BBT/DS) × t_{LPCck}	ns	A7.10
t_{10}	Burst DATA (rd) input hold	0	—	ns	A7.11
t_{11}	Read Burst $\overline{ACK}$ assertion after $\overline{CS}$[x] assertion	(2 + WS) × t_{LPCck}	(2 + WS) × t_{LPCck}	ns	A7.12
t_{12}	Non-muxed write Burst $\overline{CS}$[x] pulse width	(2.5 + WS + BBT/DS) × t_{LPCck}	(2.5 + WS + BBT/DS) × t_{LPCck}	ns	A7.13
t_{13}	Write Burst ADDR, R/$\overline{W}$, TSIZ, DATA (wr) hold after $\overline{CS}$[x] negation	0.5 × t_{LPCck} – t_{OD}	(HC + 0.5) × t_{LPCck} + t_{OD}	ns	A7.14

Table 23. LPC Timing (continued)

Sym	Description	Min	Max	Units	SpecID
t_{14}	Write Burst $\overline{ACK}$ assertion after $\overline{CS}$[x] assertion	(2.5 + WS) × t_{LPCck} – t_{OD}	(2.5 + WS) × t_{LPCck} + t_{OD}	ns	A7.15
t_{15}	Write Burst DATA valid	t_{LPCck} – t_{OD}	—	ns	A7.16
t_{16}	Non-MUXed Mode: asynchronous write Burst ADDR valid before write DATA valid	0.5 × t_{LPCck} – t_{OD}	0.5 × t_{LPCck} + t_{OD}	ns	A7.17
t_{17}	MUXed Mode: ADDR cycle	AL × 2 × t_{LPCck} – t_{OD}	AL × 2 × t_{LPCck}	ns	A7.18
t_{18}	MUXed Mode: $\overline{ALE}$ cycle	AL × t_{LPCck}	AL × t_{LPCck}	ns	A7.19
t_{19}	Non-MUXed Mode Page Burst: ADDR cycle	t_{LPCck} – t_{OD}	t_{LPCck}	ns	A7.20
t_{20}	Non-MUXed Mode Page Burst: Burst DATA (rd) input setup before next ADDR cycle	t_{OD} + t_6	—	ns	A7.21
t_{21}	Non-MUXed Mode Page Burst: Burst DATA (rd) input hold after next ADDR cycle	0	—	ns	A7.22
t_{22}	MUXed Mode: non-Burst $\overline{CS}$[x] pulse width	(ALT × (AL × 2) + 2 + WS) × t_{LPCck}	(ALT × (AL × 2) + 2 + WS) × t_{LPCck}	ns	A7.23
t_{23}	MUXed Mode: read Burst $\overline{CS}$[x] pulse width	[ALT (AL × 2) + 2 + WS + BBT/DS] × t_{LPCck}	[ALT × (AL × 2)+2+WS +BBT/DS] × t_{LPCck}	ns	A7.24
t_{24}	MUXed Mode: write Burst $\overline{CS}$[x] pulse width	[ALT × (AL × 2) + 2.5 + WS + BBT/DS] × t_{LPCck}	[ALT × (AL × 2)+2.5+WS +BBT/DS] × t_{LPCck}	ns	A7.25

3.3.7.1 Non-MUXed Mode

3.3.7.1.1 Non-MUXed Non-Burst Mode

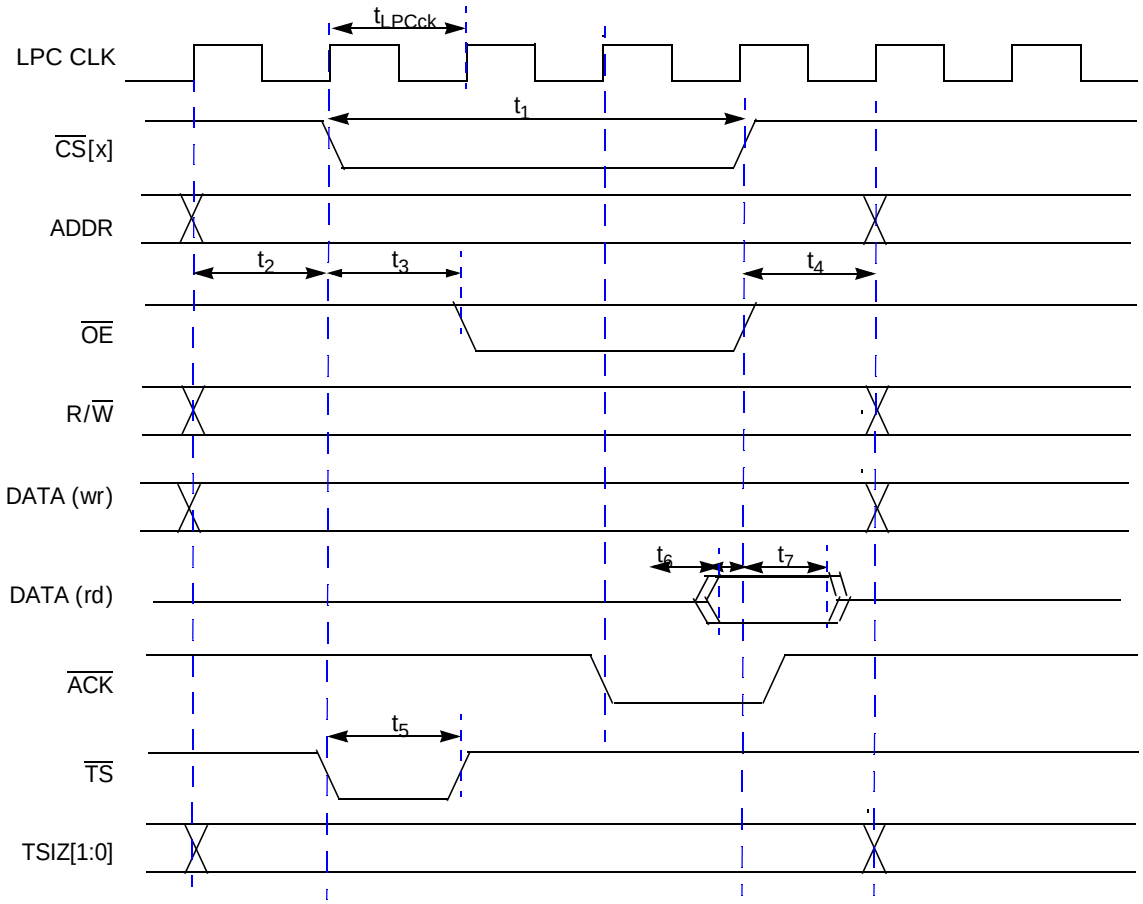

Figure 13. Timing Diagram – Non-MUXed Non-Burst Mode

NOTE

ACK is asynchonous input signal and has no timing requirements. ACK needs to be deasserted after CS[x] is deasserted.

3.3.7.1.2 Non-MUXed Synchronous Read Burst Mode

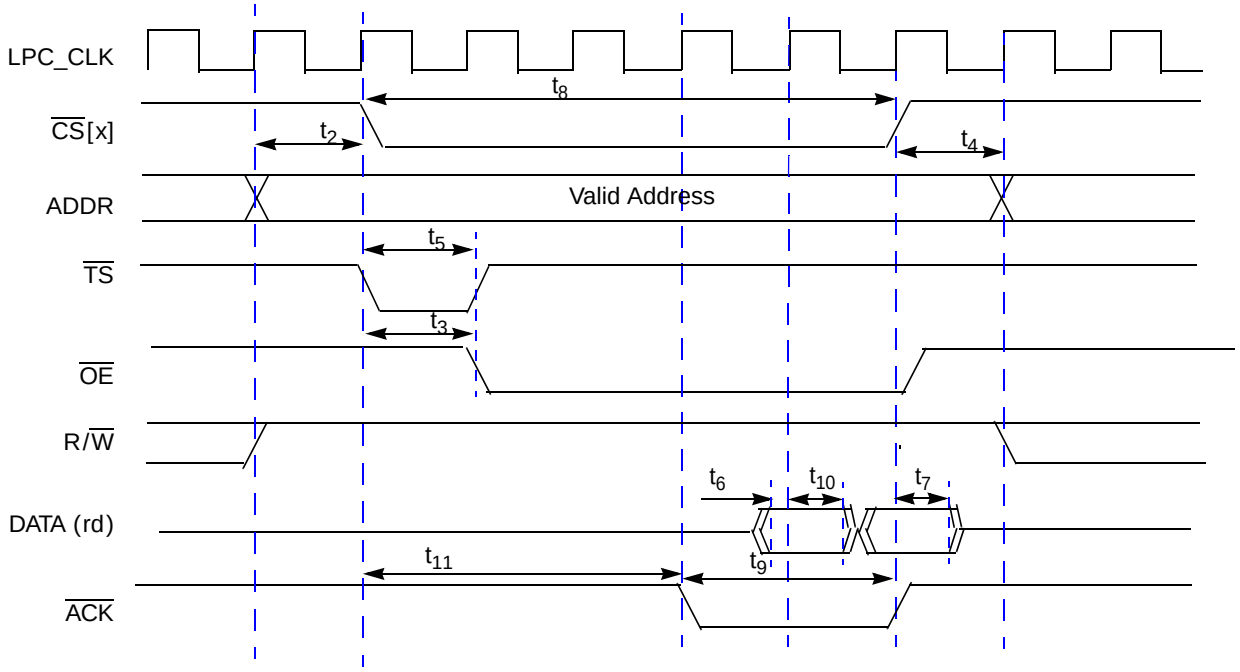

Figure 14. Timing Diagram – Non-MUXed Synchronous Read Burst Mode

3.3.7.1.3 Non-MUXed Synchronous Write Burst Mode

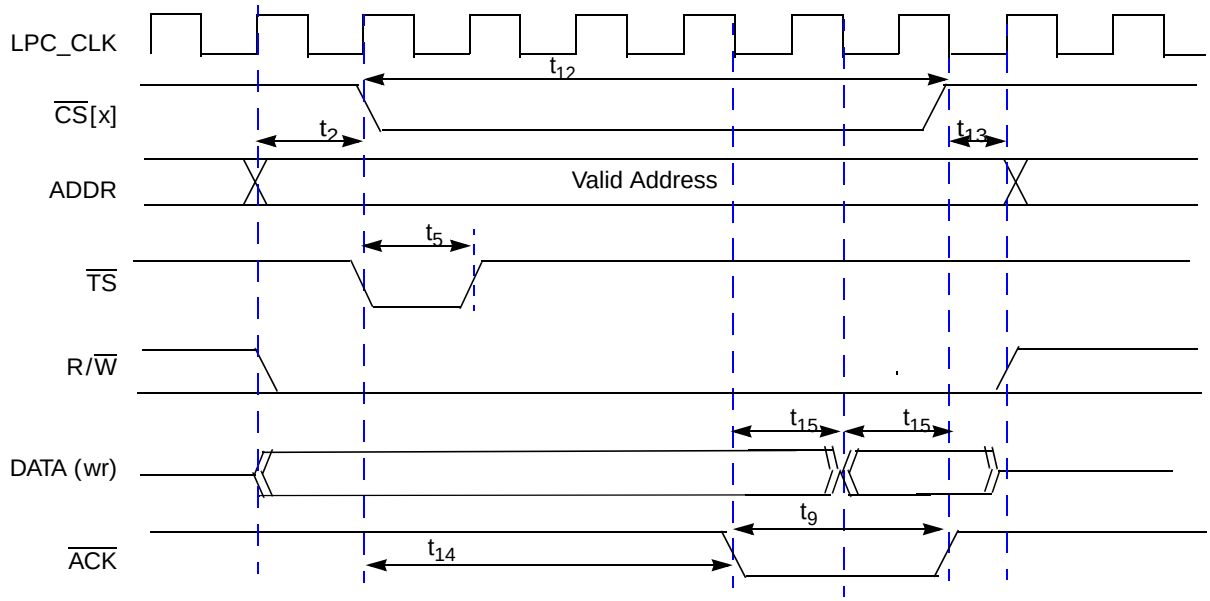

Figure 15. Timing Diagram – Non-MUXed Synchronous Write Burst

3.3.7.1.4 Non-MUXed Asynchronous Read Burst Mode (Page Mode)

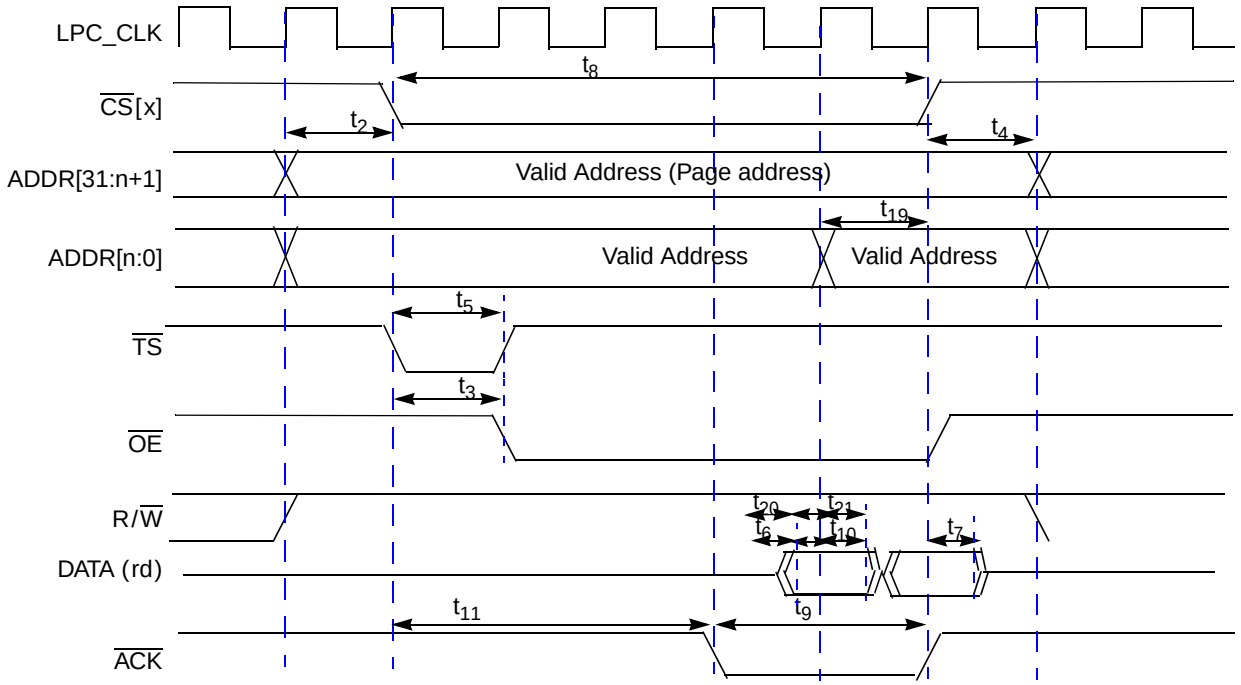

Figure 16. Timing Diagram – Non-MUXed Asynchronous Read Burst

3.3.7.1.5 Non-MUXed Aynchronous Write Burst Mode

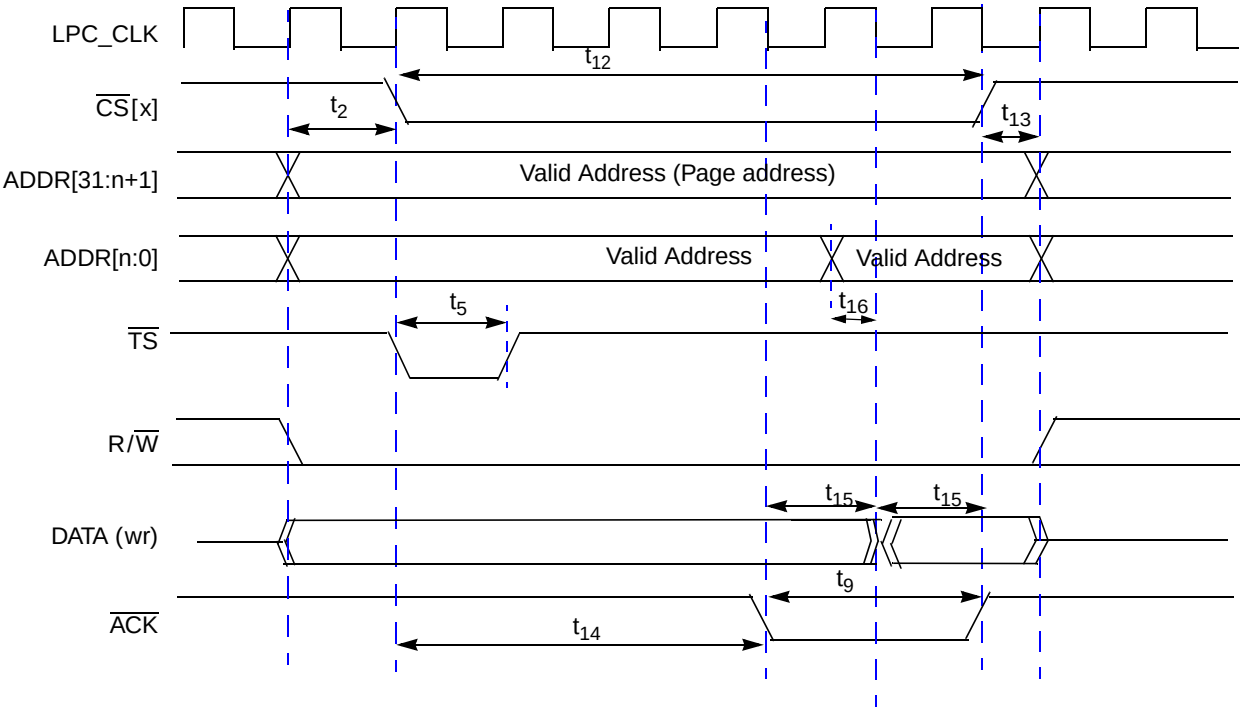

Figure 17. Timing Diagram – Non-MUXed Aynchronous Write Burst

3.3.7.2 MUXed Mode

3.3.7.2.1 MUXed Non-Burst Mode

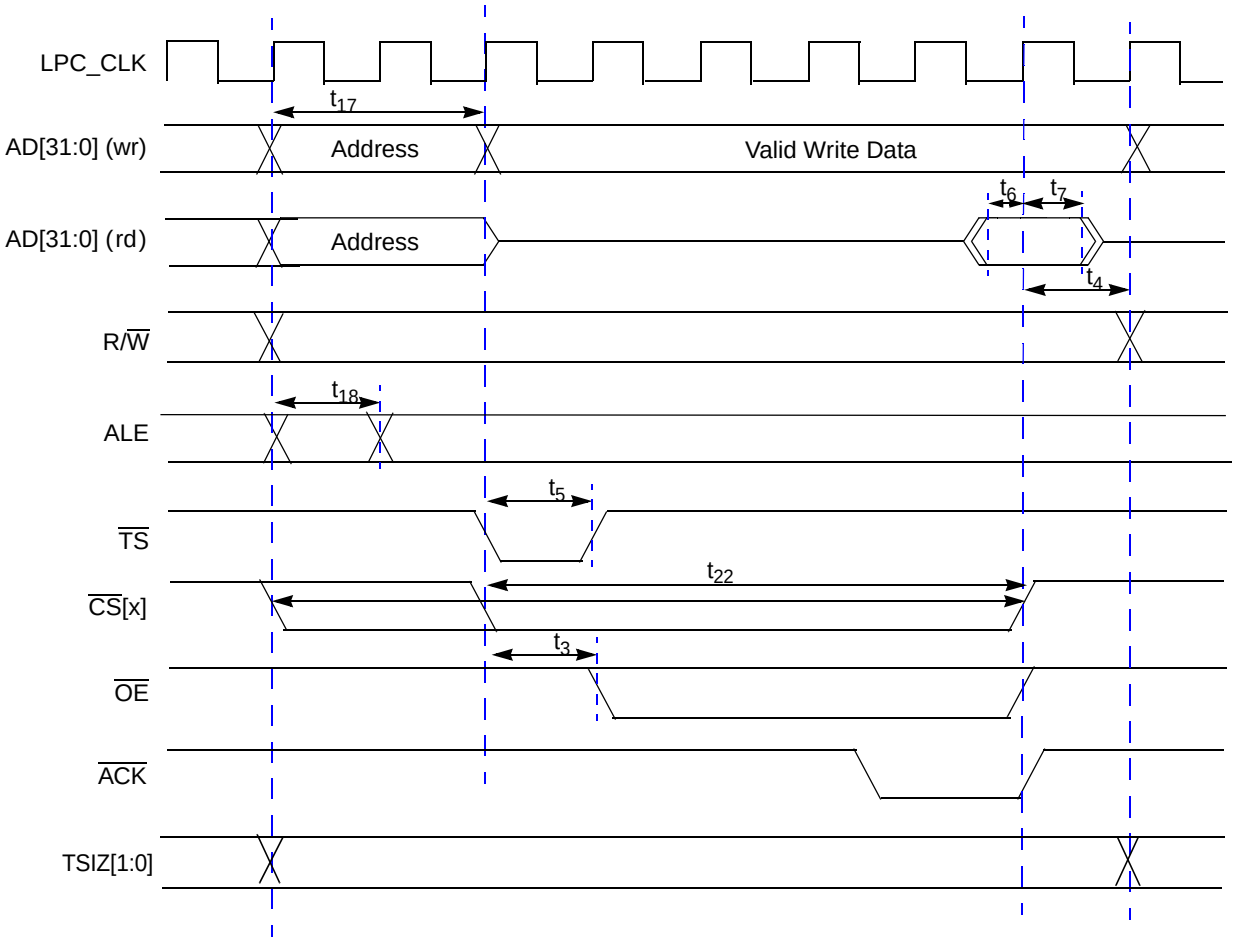

Figure 18. Timing Diagram – MUXed Non-Burst Mode

NOTE

ACK is asynchonous input signal and has no timing requirements. ACK needs to be deasserted after CS[x] is deasserted.

3.3.7.2.2 MUXed Synchronous Read Burst Mode

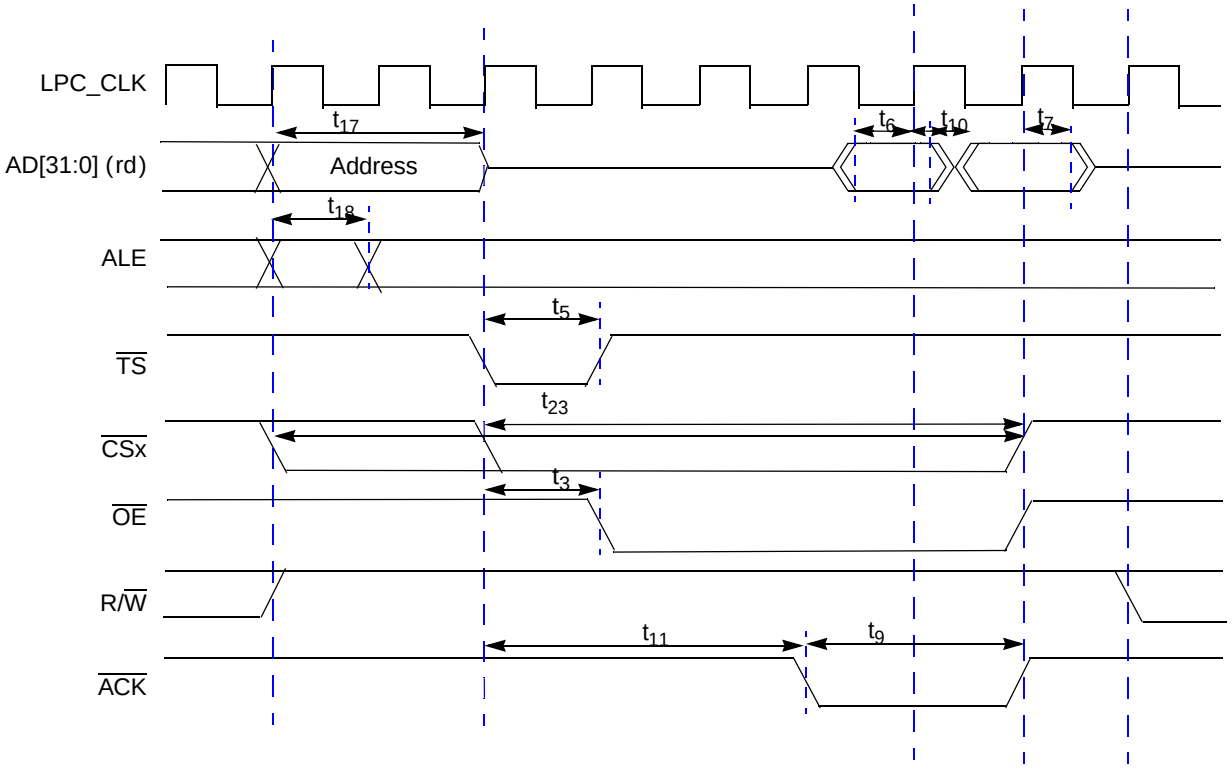

Figure 19. Timing Diagram – MUXed Synchronous Read Burst

3.3.7.2.3 MUXed Synchronous Write Burst Mode

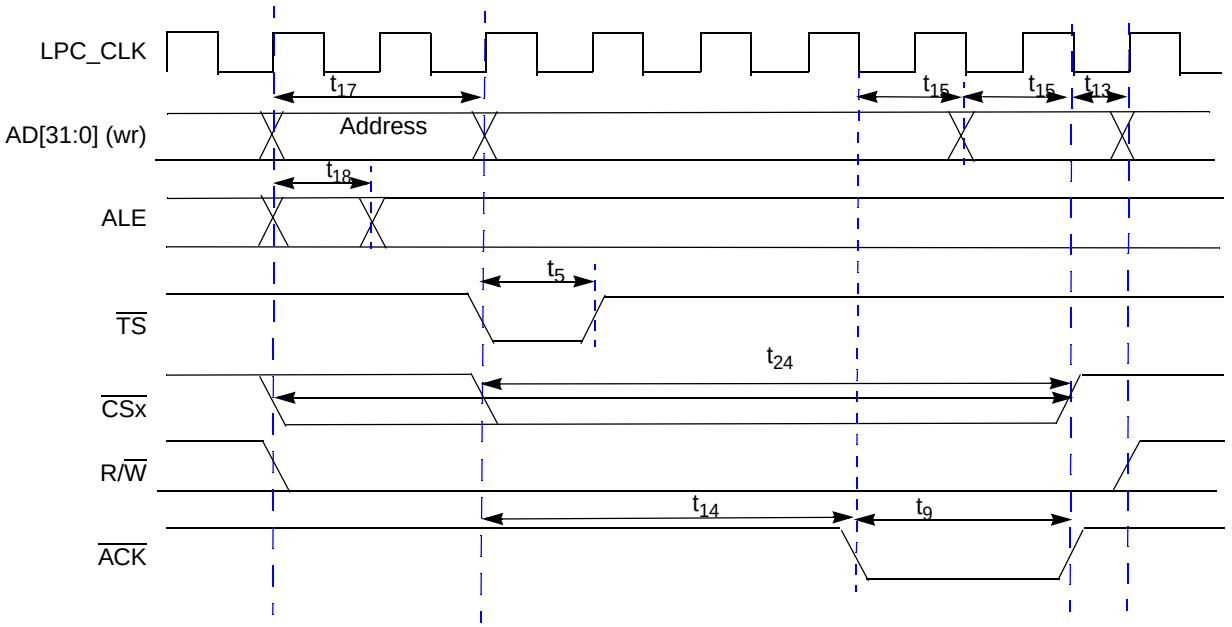

Figure 20. Timing Diagram – MUXed Synchronous Write Burst

3.3.8 NFC

The NAND flash controller (NFC) implements the interface to standard NAND Flash memory devices. This section describes the timing parameters of the NFC.

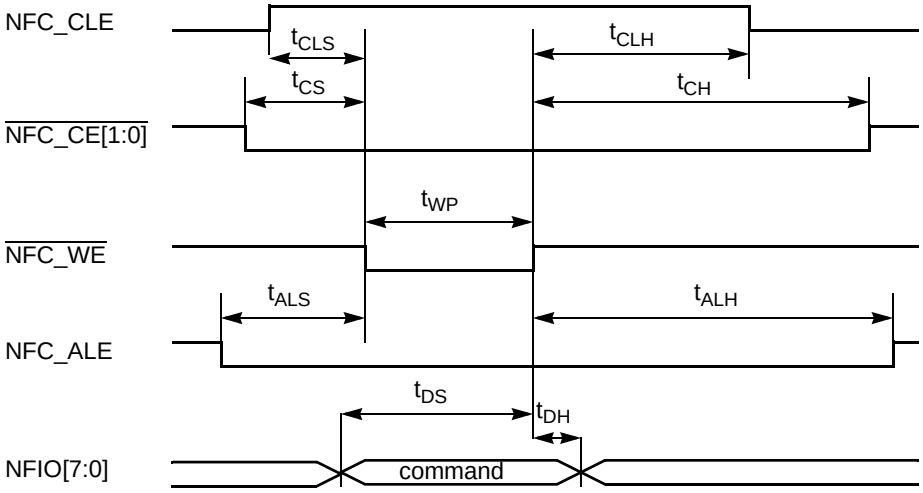

Figure 21. Command Latch Cycle Timing

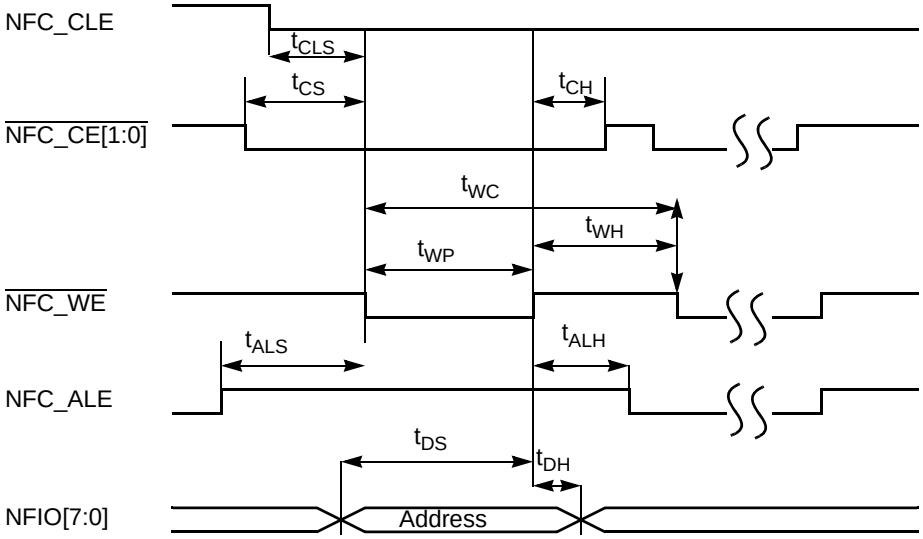

Figure 22. Address Latch Cycle Timing

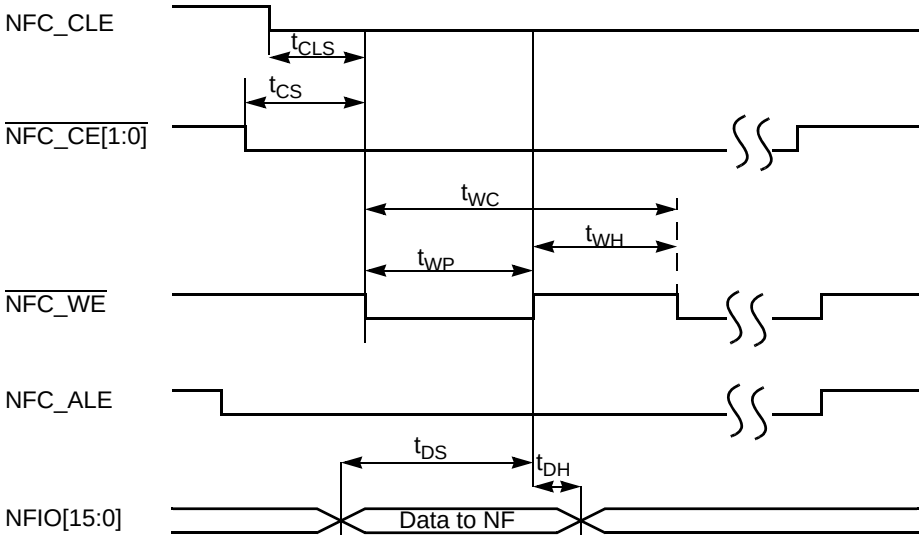

Figure 23. Write Data Latch Timing

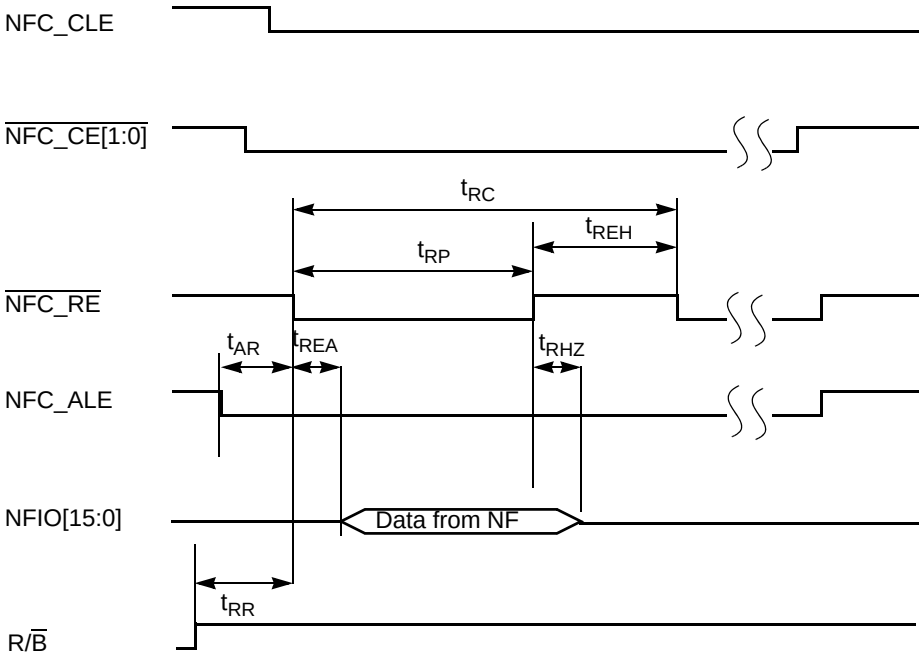

Figure 24. Read Data Latch Timing

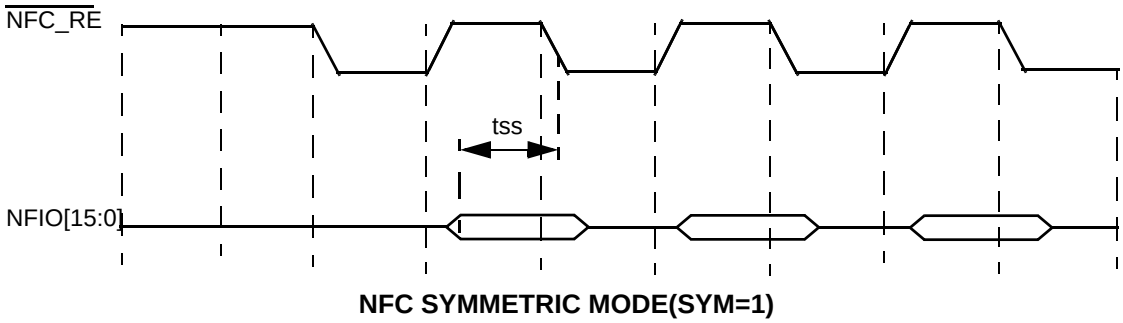

Figure 25. Read Data Latch Timing in Symmetric Mode

Table 24. NFC Timing Characteristics in asymmetric mode(SYM=0)[1]

Timing parameter	Description	Min. value	Max. value	Unit	SpecID
t_{CLS}	NFC_CLE setup Time	T + 1	—	ns	A8.1
t_{CLH}	NFC_CLE Hold Time	T – 1	—	ns	A8.2
t_{CS}	$\overline{\text{NFC\_CE}}$[1:0] Setup Time	2T – 1	—	ns	A8.3
t_{CH}	$\overline{\text{NFC\_CE}}$[1:0] Hold Time	3T	—	ns	A8.4
t_{WP}	$\overline{\text{NFC\_WP}}$ Pulse Width	T – 1	—	ns	A8.5
t_{ALS}	NFC_ALE Setup Time	T – 1	—	ns	A8.6
t_{ALH}	NFC_ALE Hold Time	T – 1	—	ns	A8.7
t_{DS}	Data Setup Time	T – 2	—	ns	A8.8
t_{DH}	Data Hold Time	T – 1	—	ns	A8.9
t_{WC}	Write Cycle Time	2T	—	ns	A8.10
t_{WH}	$\overline{\text{NFC\_WE}}$ Hold Time	T – 1	—	ns	A8.11
t_{RR}	Ready to $\overline{\text{NFC\_RE}}$ Low	5T + 2	—	ns	A8.12
t_{RP}	$\overline{\text{NFC\_RE}}$ Pulse Width	1.5T – 1	—	ns	A8.13
t_{RC}	READ Cycle Time	2T	—	ns	A8.14
t_{REH}	$\overline{\text{NFC\_RE}}$ High Hold Time	0.5T	—	ns	A8.15

1 T is the flash clock cycle.
T = 45 ns, frequency = 22 MHz (boot configuration, IP bus = 66 MHz)
T = 36 ns, frequency = 27 MHz (maximum configurable frequency, IP bus = 83 MHz)

Table 25. NFC Timing Characteristics in Symmetric mode(SYM=1)[1]

Timing Parameter	Description	Min. value	Max. value	Unit	SpecID
t_{CLS}	NFC_CLE Setup time	T	—	ns	A8.21
t_{CLH}	NFC_CLE Hold time	T	—	ns	A8.22
t_{CS}	NFC_CE[1:0] Setup time	T-2	—	ns	A8.23
t_{CH}	NFC_CE[1:0] Hold time	1.5T-1	—	ns	A8.24
t_{WP}	NFC_WE Pulse width	0.5T+1	—	ns	A8.25
t_{ALS}	NFC_ALE Setup time	T	—	ns	A8.26
t_{ALH}	NFC_ALE Hold time	T	—	ns	A8.27
t_{DS}	Data Setup time	0.5T-3	—	ns	A8.28
t_{DH}	Data Hold time	0.5T	—	ns	A8.29
t_{WC}	Write Cycle time	T	—	ns	A8.30
t_{WH}	NFC_WE Hold time	0.5T-1	—	ns	A8.31
t_{RR}	Ready to NFC_RE low	5T+2	—	ns	A8.32
t_{RP}	NFC_RE pulse width	0.5T	—	ns	A8.33
t_{RC}	Read Cycle time	T	—	ns	A8.34
t_{REH}	NFC_RE High hold time	0.5T	—	ns	A8.35
t_{SS}	NFC Read Data setup time	9.6	—	ns	A8.36

1 T is the flash clock cycle.
T = 45 ns, frequency = 22 MHz (boot configuration, IP bus = 66 MHz)
T = 36 ns, frequency = 27 MHz (maximum configurable frequency, IP bus = 83 MHz)

3.3.9 PATA

The MPC5121e/MPC5123 ATA Controller (PATA) is completely software programmable. It can be programmed to operate with ATA protocols using their respective timing, as described in the ANSI ATA-4 specification. The ATA interface is completely asynchronous in nature. Signal relationships are based on specific fixed timing in terms of timing units (nanoseconds).

ATA data setup and hold times, with respect to Read/Write strobes, are software programmable inside the ATA Controller. Data setup and hold times are implemented using counters. The counters count the number of ATA clock cycles needed to meet the ANSI ATA-4 timing specifications. For details, see the ANSI ATA-4 specification and how to program an ATA Controller and ATA drive for different ATA protocols and their respective timing. See the *MPC5121e Microcontroller Reference Manual*.

The MPC5121e/MPC5123 ATA Host Controller design makes data available coincidentally with the active edge of the WRITE strobe in PIO and Multiword DMA modes.

- Write data is latched by the drive at the inactive edge of the WRITE strobe. This gives ample setup-time beyond that required by the ATA-4 specification.
- Data is held unchanged until the next active edge of the WRITE strobe. This gives ample hold-time beyond that required by the ATA-4 specification.

All ATA transfers are programmed in terms of system clock cycles (IP bus clocks) in the ATA Host Controller timing registers. This puts constraints on the ATA protocols and their respective timing modes in which the ATA Controller can communicate with the drive.

Faster ATA modes (i.e., UDMA 0, 1, 2) are supported when the system is running at a sufficient frequency to provide adequate data transfer rates. Adequate data transfer rates are a function of the following:

- The MPC5121e/MPC5123 operating frequency (IP bus clock frequency)
- Internal MPC5121e/MPC5123 bus latencies
- Other system load dependent variables

The ATA clock is the same frequency as the IP bus clock in MPC5121e/MPC5123. See the *MPC5121e Microcontroller Reference Manual*.

NOTE

All output timing numbers are specified for nominal 50 pF loads.

3.3.9.1 PATA Timing Parameters

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the ATA interface in silicon, the bus transceiver used, the cable delay and cable skew. The parameters shown in Table 3-26 specify the ATA timing.

Table 3-26. PATA Timing Parameters

Name	Meaning	Controlled by	Value	SpecID
T	PATA Bus clock period	MPC5121E/MPC5123	15 ns	A9.1
t_{i_ds}	Set-up time ATA_DATA to ATA_IORDY edge (UDMA-in only)	MPC5121E/MPC5123	2 ns	A9.2
t_{i_dh}	Hold time ATA_IORDY edge to ATA_DATA (UDMA-in only)	MPC5121E/MPC5123	5 ns	A9.3
t_{co}	Propagation delay bus clock L-to-H to: ATA_CS0, ATA_CS1, ATA_DA2, ATA_DA1, ATA_DA0, ATA_DIOR, ATA_DIOW, ATA_DMACK, ATA_DATA, ATA_BUFFER_EN	MPC5121E/MPC5123	2 ns	A9.4
t_{su}	Set-up time ATA_DATA to bus clock L-to-H	MPC5121E/MPC5123	2 ns	A9.5
t_{sui}	Set-up time ATA_IORDY to bus clock H-to-L	MPC5121E/MPC5123	2 ns	A9.6
t_{hi}	Hold time ATA_IORDY to bus clock H to L	MPC5121E/MPC5123	2 ns	A9.7
t_{skew1}	Max difference in propagation delay bus clock L-to-H to any of following signals: ATA_CS0, ATA_CS1, ATA_DA2, ATA_DA1, ATA_DA0, ATA_DIOR, ATA_DIOW, ATA_DMACK, ATA_DATA (WRITE), ATA_BUFFER_EN	MPC5121E/MPC5123	1.7 ns	A9.8
t_{skew2}	Max difference in buffer propagation delay for any of following signals: ATA_CS0, ATA_CS1, ATA_DA2, ATA_DA1, ATA_DA0, ATA_DIOR, ATA_DIOW, ATA_DMACK, ATA_DATA (WRITE), ATA_BUFFER_EN	Transceiver		A9.9
t_{skew3}	Max difference in buffer propagation delay for any of following signals: ATA_IORDY, ATA_DATA (read)	Transceiver		A9.10
t_{buf}	Max buffer propagation delay	Transceiver		A9.11
t_{cable1}	Cable propagation delay for ata_data	Cable		A9.12
t_{cable2}	Cable propagation delay for control signals: ATA_DIOR, ATA_DIOW, ATA_IORDY, ATA_DMACK	Cable		A9.13

Table 3-26. PATA Timing Parameters (continued)

Name	Meaning	Controlled by	Value	SpecID
t_{skew4}	Max difference in cable propagation delay between: ATA_IORDY and ATA_DATA (read)	Cable		A9.14
t_{skew5}	Max difference in cable propagation delay between: ATA_DIOR, ATA_DIOW, ATA_DMACK and ATA_CS0, ATA_CS1, ATA_DA2, ATA_DA1, ATA_DA0, ATA_DATA (write)	Cable		A9.15
tskew6	Max difference in cable propagation delay without accounting for ground bounce	Cable		A9.16

3.3.9.2 PIO Mode Timing

A timing diagram for the PIO read mode is given in Figure 26.

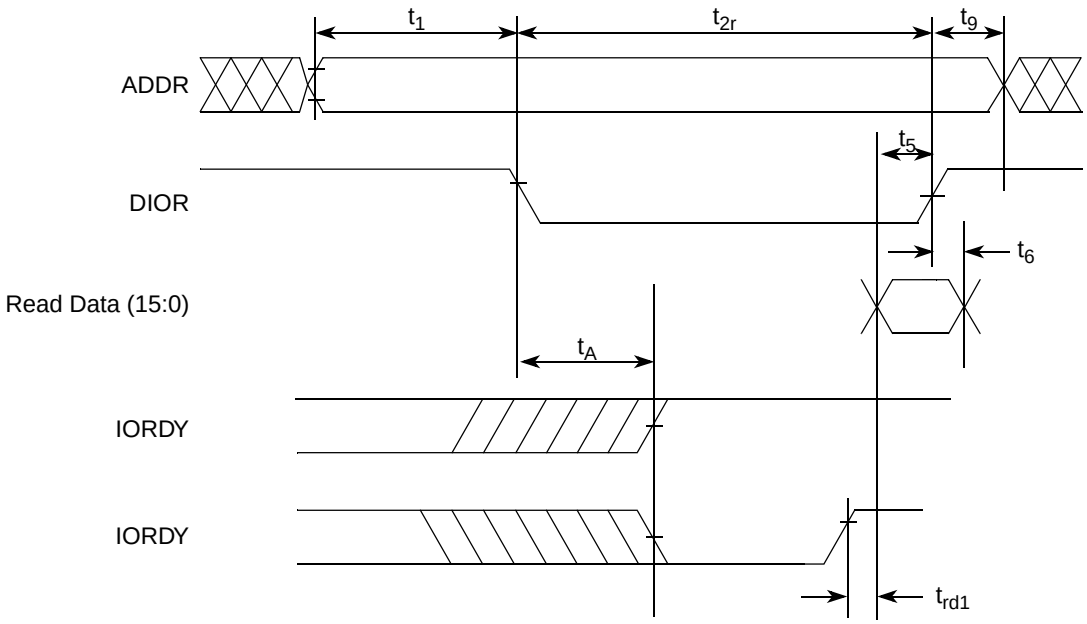

Figure 26. PIO Read Mode Timing

To fulfill read mode timing, the different timing parameters given in Table 3-27 must be observed.

Table 3-27. Timing Parameters PIO Read

ATA Parameter	PIO Read Mode Timing Parameter	Value	How to meet	SpecID
t_1	t_1	$t_1(min) = (time\_1 \times T) - (t_{skew1} + t_{skew2} + t_{skew5})$	calculate and programming time_1. [1]	A9.20
t_2	t_2r	$t_2(min) = (time\_2r \times T) - (t_{skew1} + t_{skew2} + t_{skew5})$	calculate and programming time_2r. [1]	A9.21
t_9	t_9	$t_9(min) = (time\_9 \times T) - (t_{skew1} + t_{skew2} + t_{skew6})$	calculate and programming time_9. [1]	A9.22

Table 3-27. Timing Parameters PIO Read (continued)

ATA Parameter	PIO Read Mode Timing Parameter	Value	How to meet	SpecID
t_5	t_5	$t_5(min) = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable2}$	If not met, increase time_2r	A9.23
t_6	t_6	0	—	A9.24
t_A	t_A	$t_{A(min)} = (1.5 + time\_ax) \times T - (t_{co} + t_{sui} + t_{cable2} + t_{cable2} + 2 \times t_{buf})$	calculate and programming time_ax. [1]	A9.25
t_{rd}	t_{rd1}	$t_{rd1(max)} = (-t_{rd}) + (t_{skew3} + t_{skew4})$ $t_{rd1(min)} = (time\_pio\_rdx - 0.5) \times T - (t_{su} + t_{hi})$ $(time\_pio\_rdx - 0.5) \times T > t_{su} + t_{hi} + t_{skew3} + t_{skew4}$	calculate and programming time_pio_rdx. [1]	A9.26
t_0	—	$t_{0(min)} = (time\_1 + time\_2 + time\_9) \times T$	time_1, time_2r, time_9	A9.27

1 See the *MPC5121e Microcontroller Reference Manual.*

In PIO write mode, timing waveforms are somewhat different as shown in Figure 27.

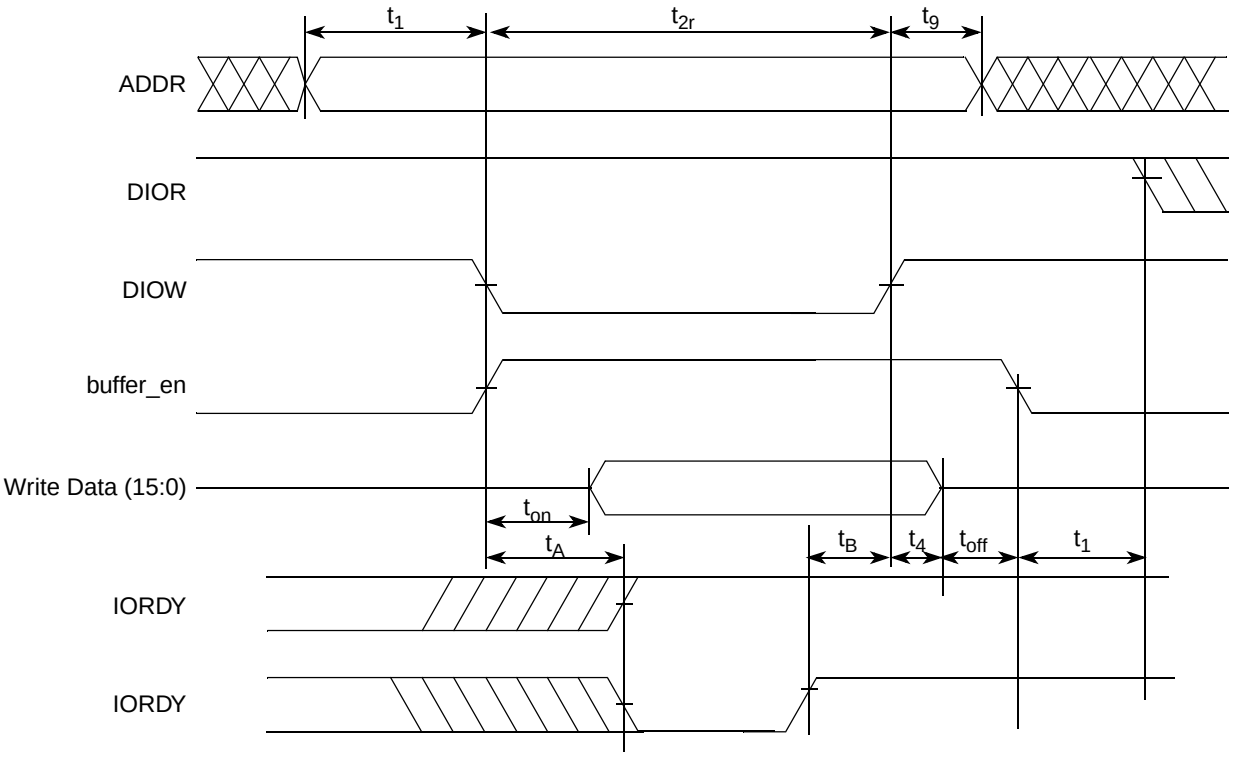

Figure 27. PIO Write Mode Timing

To fulfill this timing, several parameters need to be observed as shown in Table 3-28.

Table 3-28. Timing Parameters PIO Write

ATA Parameter	PIO Write Mode Timing Parameter	Value	How to meet	SpecID
t1	t1	t1(min) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1. [1]	A9.30
t2	t2r	t2(min) = time_2w × T – (tskew1 + tskew2 + tskew5)	calculate and programming time_2w. [1]	A9.31
t9	t9	t9(min) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9. [1]	A9.32
t3	—	t3(min) = (time_2w – time_on) × T – (tskew1 + tskew2 + tskew5)	If not met, increase time_2w	A9.33
t4	t4	t4(min) = time_4 × T – tskew1	calculate and programming time_4. [1]	A9.34
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2 × tbuf)	calculate and programming time_ax. [1]	A9.35
t0	—	t0(min) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9	A9.36
—	—	Avoid bus contention when switching buffer on by making ton long enough	—	A9.37
—	—	Avoid bus contention when switching buffer off by making toff long enough	—	A9.38

1 See the *MPC5121e Microcontroller Reference Manual.*

3.3.9.3 Timing in Multiword DMA Mode

Timing in multiword DMA mode is given in Figure 28 and Figure 29.

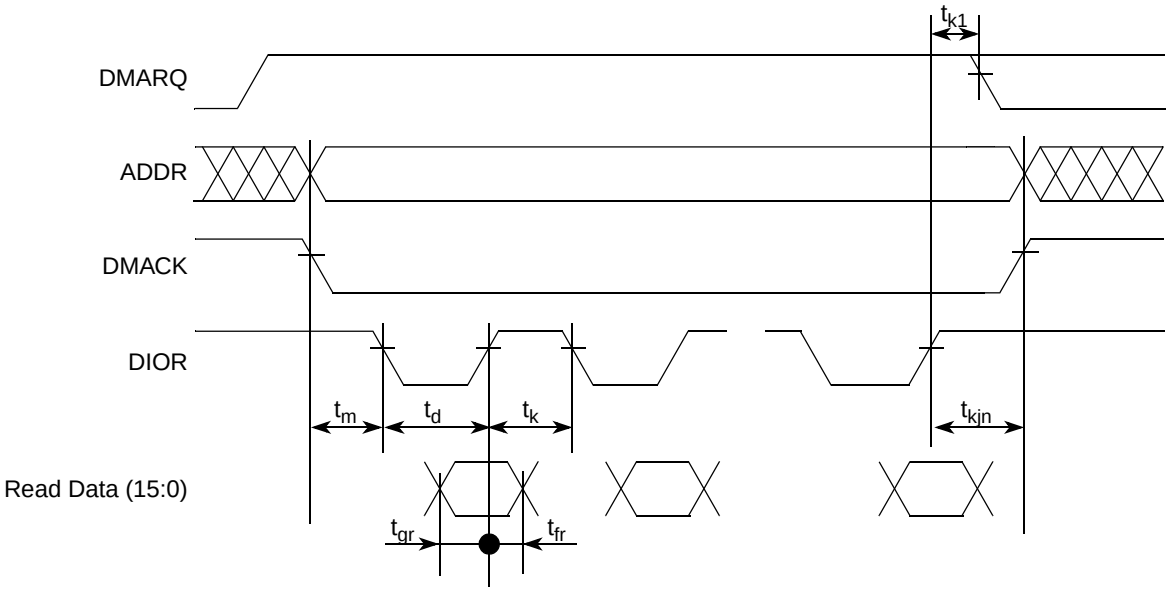

Figure 28. MDMA Read Timing

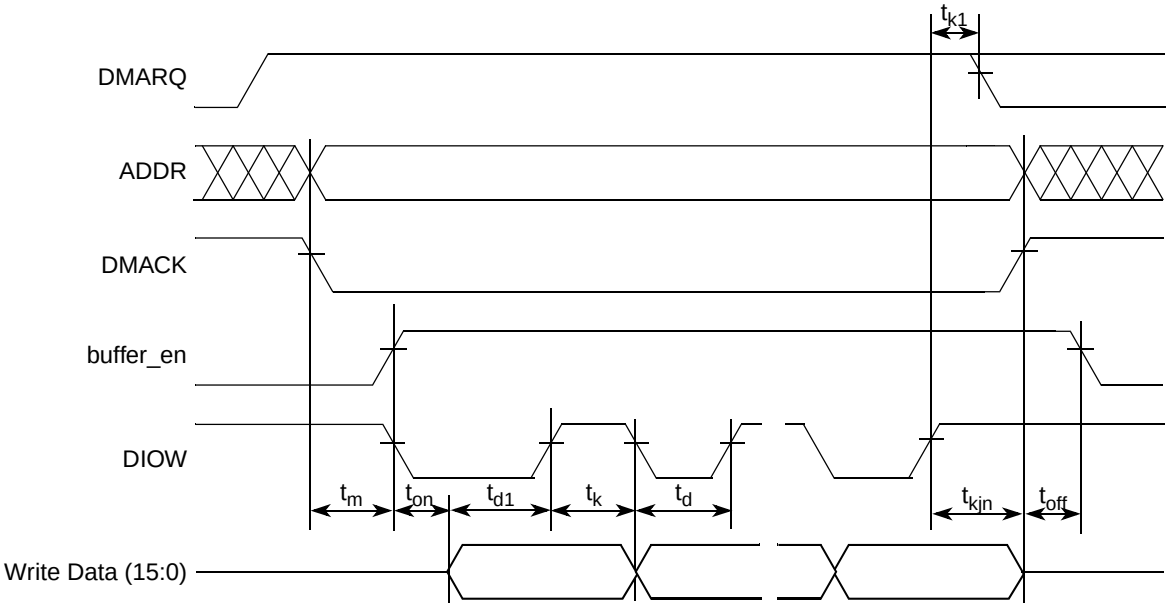

Figure 29. MDMA Write Timing

To meet this timing, a number of timing parameters must be controlled as shown in Table 3-29.

Table 3-29. Timing Parameters MDMA Read and Write

ATA Parameter	MDMA Read/Write Timing Parameter	Value	How to meet	SpecID
t_m, t_i	t_m	$t_{m(min)} = t_{i(min)} = (time\_m \times T) - (t_{skew1} + t_{skew2} + t_{skew5})$	calculate and programming time_m. [1]	A9.40
t_d	t_d, t_{d1}	$t_{d1(min)} = t_{d(min)} = (time\_d \times T) - (t_{skew1} + t_{skew2} + t_{skew6})$	calculate and programming time_d. [1]	A9.41
t_k	t_k	$t_{k(min)} = (time\_k \times T) - (t_{skew1} + t_{skew2} + t_{skew6})$	calculate and programming time_k. [1]	A9.42
t_0	—	$t_{0(min)} = (time\_d + time\_k) \times T$	time_d, time_k	A9.43
$t_{g(read)}$	t_{gr}	$t_{gr(min\text{-}read)} = t_{co} + t_{su} + t_{buf} + t_{buf} + t_{cable1} + t_{cable}2$ $t_{gr(min\text{-}drive)} = td - te(drive)$	time_d. [1]	A9.44
$t_{f(read)}$	t_{fr}	$t_{fr(min\text{-}drive)} = 0$	—	A9.45
$t_{g(write)}$	—	$t_{g(min\text{-}write)} = time\_d \times T - (t_{skew1} + t_{skew2} + t_{skew5})$	time_d	A9.46
$t_{f(write)}$	—	$t_{f(min\text{-}write)} = time\_k \times T - (t_{skew1} + t_{skew2} + t_{skew6})$	time_k	A9.47
t_L	—	$t_{L(max)} = [(time\_d + time\_k - 2) \times T] - [t_{su} + t_{co} + (2 \times t_{buf}) + (2 \times t_{cable2})]$	time_d, time_k	A9.48
t_n, t_j	t_{kjn}	$t_n = t_j = t_{kjn} = [max(time\_k,.\ time\_jn) \times T] - (t_{skew1} + t_{skew2} + t_{skew6})$	calculate and programming time_jn. [1]	A9.49
—	t_{on} t_{off}	$t_{on} = (time\_on \times T) - t_{skew1}$ $t_{off} = (time\_off \times T) - t_{skew1}$	—	A9.50

[1] See the *MPC5121e Microcontroller Reference Manual.*

3.3.9.4 UDMA In Timing Diagrams

UDMA mode timing is more complicated than PIO mode or MDMA mode. In this section, timing diagrams for UDMA in are given:

- Figure 30 gives timing for UDMA in transfer start
- Figure 31 gives timing for host terminating UDMA in transfer
- Figure 32 gives timing for device terminating UDMA in transfer.

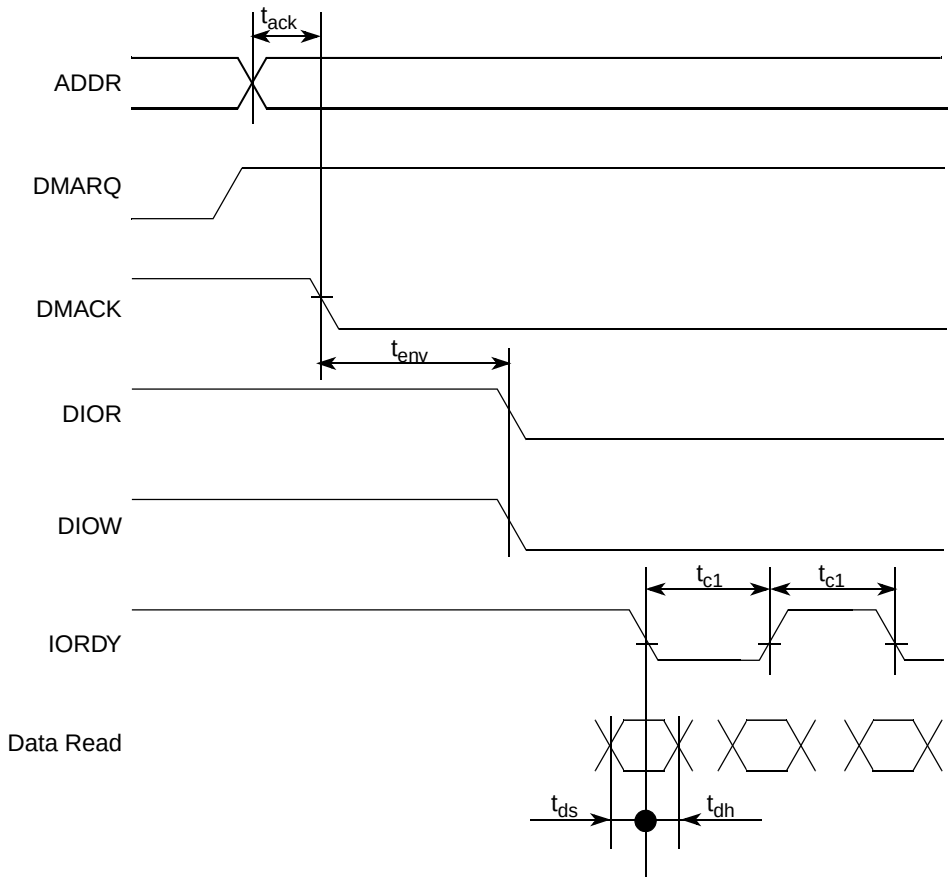

Figure 30. UDMA In Transfer Start Timing Diagram

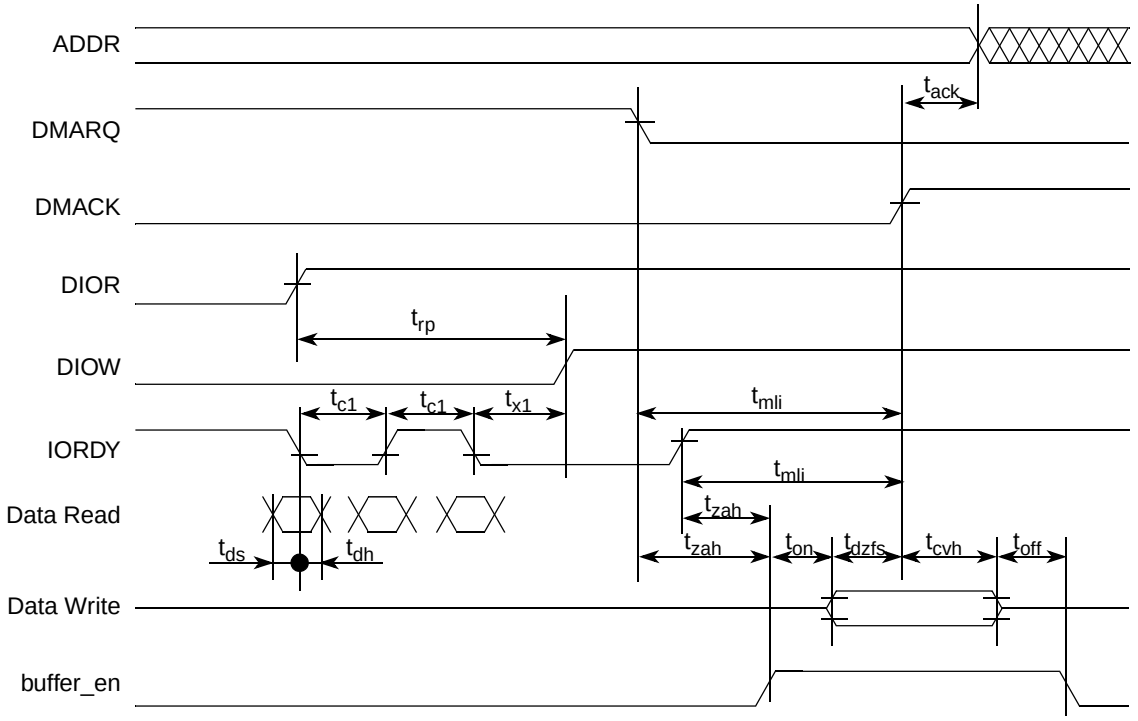

Figure 31. UDMA In Host Terminates Transfer

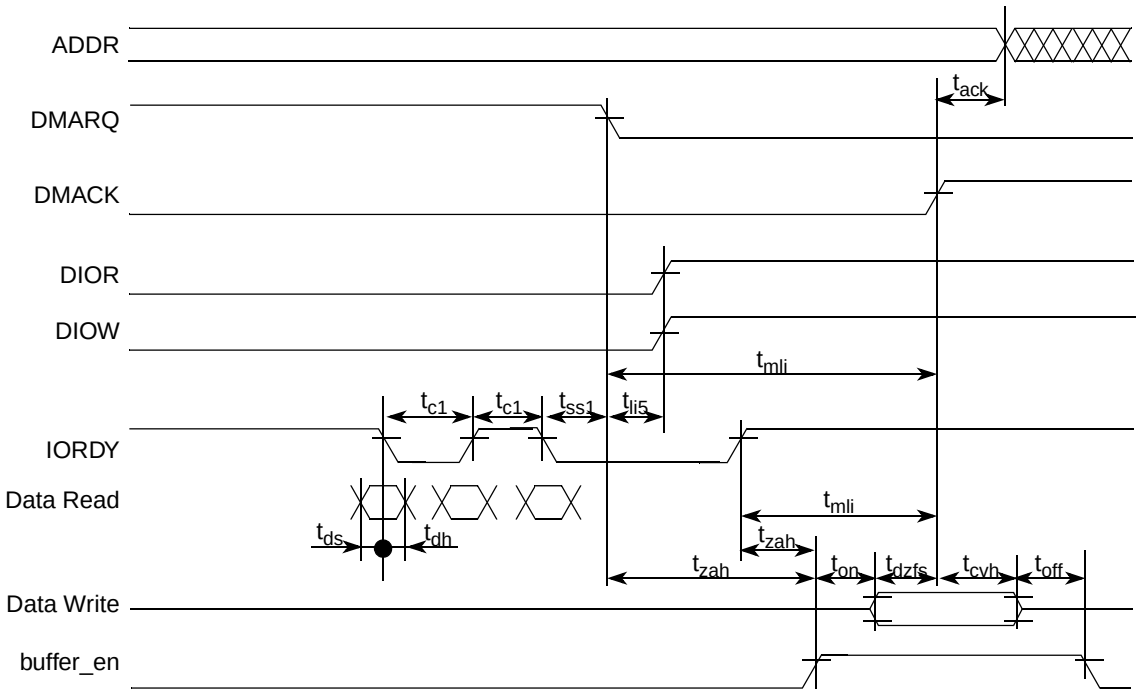

Figure 32. UDMA In Device Terminates Transfer

Timing parameters are explained in Table 30.

Table 30. Timing Parameters UDMA in Burst

ATA Parameter	UDMA In Timing Parameter	Value	How to Meet	SpecID
t_{ack}	t_{ack}	$t_{ack(min)} = (time\_ack \times T) - (t_{skew1} + t_{skew2})$	calculate and programming time_ack. [1]	A9.51
t_{env}	t_{env}	$t_{env(min)} = (time\_env \times T) - (t_{skew1} + t_{skew2})$ $t_{env(max)} = (time\_env \times T) + (t_{skew1} + t_{skew2})$	calculate and programming time_env. [1]	A9.52
t_{ds}	t_{ds1}	$t_{ds} - (t_{skew3}) - ti\_ds > 0$	t_{skew3}, ti_ds, ti_dh should be low enough	A9.53
t_{dh}	t_{dh1}	$t_{dh} - (t_{skew3}) - ti\_dh > 0$		A9.54
t_{cyc}	t_{c1}	$(t_{cyc} - t_{skew}) > T$	Bus clock period T big enough	A9.55
t_{rp}	t_{rp}	$t_{rp(min)} = time\_rp \times T - (t_{skew1} + t_{skew2} + t_{skew6})$	calculate and programming time_rp. [1]	A9.56
—	t_{x1} [2]	$(time\_rp \times T) - [tco + tsu + 3T + (2 \times t_{buf}) + (2 \times tcable2)] >$ trfs (drive)	calculate and programming time_rp. [1]	A9.57
t_{mli}	t_{mli1}	$t_{mli1(min)} = (time\_mlix + 0.4) \times T$	calculate and programming time_mlix. [1]	A9.58
t_{zah}	t_{zah}	$t_{zah(min)} = (time\_zah + 0.4) \times T$	calculate and programming time_zah. [1]	A9.59
t_{dzfs}	t_{dzfs}	$t_{dzfs} = (time\_dzfs \times T) - (t_{skew1} + t_{skew2})$	calculate and programming time_dzfs. [1]	A9.60
t_{cvh}	t_{cvh}	$t_{cvh} = (time\_cvh \times T) - (t_{skew1} + t_{skew2})$	calculate and programming time_cvh. [1]	A9.61
—	t_{on} t_{off} [3]	$t_{on} = (time\_on \times T) - t_{skew1}$ $t_{off} = (time\_off \times T) - t_{skew1}$	—	A9.62

1 See the *MPC5121e Microcontroller Reference Manual.*

2 A special timing requirement in the ATA host requires the internal DIOW to go only high three clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

3 Make t_{on} and t_{off} large enough to avoid bus contention.

3.3.9.5 UDMA Out Timing Diagrams

UDMA mode timing is more complicated than PIO mode or MDMA mode. In this section, timing diagrams for UDMA out are given:

- Figure 33 gives timing for UDMA out transfer start
- Figure 34 gives timing for host terminating UDMA out transfer
- Figure 35 gives timing for device terminating UDMA out transfer

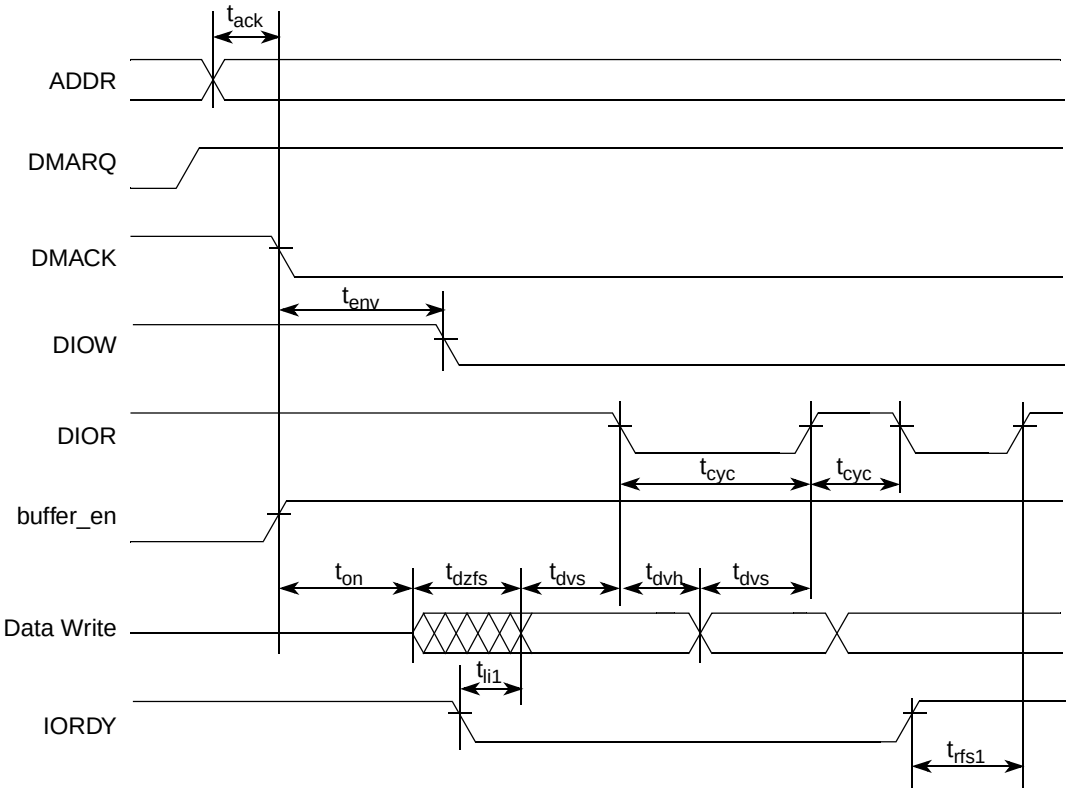

Figure 33. UDMA Out Transfer Start Timing Diagram

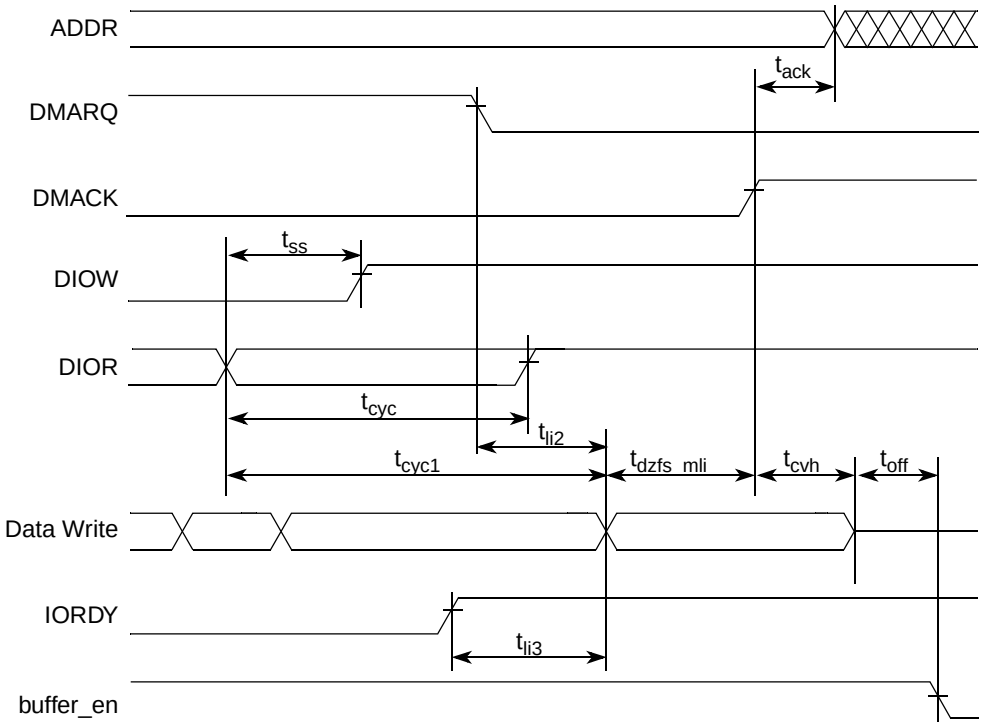

Figure 34. UDMA Out Host Terminates Transfer

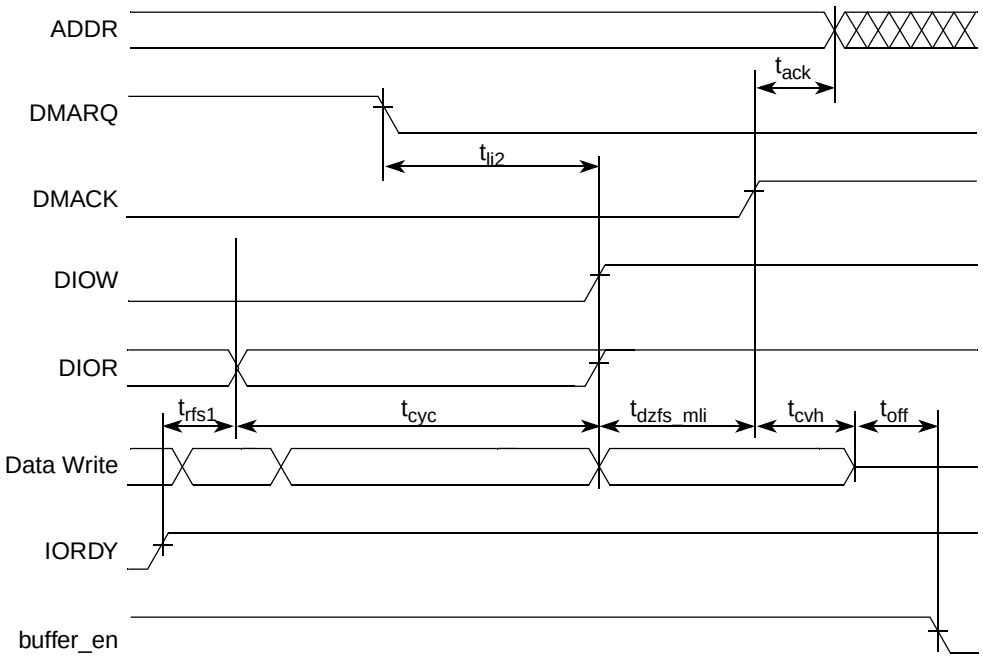

Figure 35. UDMA Out Device Terminates Transfer

Timing parameters are explained in Table 31.

Table 31. Timing Parameters UDMA Out Burst

ATA Parameter	UDMA Out Timing Parameter	Value	How to meet	SpecID
t_{ack}	t_{ack}	$t_{ack(min)} = (time\_ack \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_ack. [1]	A9.63
t_{env}	t_{env}	$t_{env(min)} = (time\_env \times T) - (t_{skew1} + t_{skew2})$ $t_{env(max)} = (time\_env \times T) + (t_{skew1} + t_{skew2})$	calculate and program time_env. [1]	A9.64
t_{dvs}	t_{dvs}	$t_{dvs} = (time\_dvs \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_dvs. [1]	A9.65
t_{dvh}	t_{dvh}	$t_{dvs} = (time\_dvh \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_dvh. [1]	A9.66
t_{cyc}	t_{cyc}	$t_{cyc} = time\_cyc \times T - (t_{skew1} + t_{skew2})$	calculate and program time_cyc. [1]	A9.67
t_{2cyc}	—	$t_{2cyc} = time\_cyc \times 2 \times T$	calculate and program time_cyc. [1]	A9.68
t_{rfs1}	t_{rfs1}	$t_{rfs1} = 1.6 \times T + t_{sui} + t_{co} + t_{buf} + t_{buf}$	—	A9.69
—	t_{dzfs}	$t_{dzfs} = time\_dzfs \times T - (t_{skew1})$	calculate and program time_dzfs. [1]	A9.70
t_{ss}	t_{ss}	$t_{ss} = time\_ss \times T - (t_{skew1} + t_{skew2})$	calculate and program time_ss. [1]	A9.71
t_{mli}	t_{dzfs_mli}	$t_{dzfs\_mli} = \max(time\_dzfs, time\_mli) \times T - (t_{skew1} + t_{skew2})$	—	A9.72
t_{li}	t_{li1}	$t_{li1} > 0$	—	A9.73

Table 31. Timing Parameters UDMA Out Burst (continued)

ATA Parameter	UDMA Out Timing Parameter	Value	How to meet	SpecID
t_{li}	t_{li2}	$t_{li2} > 0$	—	A9.74
t_{li}	t_{li3}	$t_{li3} > 0$	—	A9.75
t_{cvh}	t_{cvh}	$t_{cvh} = (time\_cvh \times T) - (t_{skew1} + t_{skew2})$	calculate and program time_cvh. [1]	A9.76
—	t_{on} t_{off}	$t_{on} = time\_on \times T - t_{skew1}$ $t_{off} = time\_off \times T - t_{skew1}$	—	A9.77

1 See the *MPC5121e Microcontroller Reference Manual.*

3.3.10 SATA PHY

1.5 Gbps SATA PHY Layer

See “Serial ATA: High Speed Serialized AT Attachment” Revision 1.0a, 7-January-2003.

3.3.11 FEC

AC Test Timing Conditions:

- Output Loading
  All Outputs: 25 pF

Table 32. MII Rx Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns	A11.1
2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns	A11.2
3	RX_CLK pulse width high	35%	65%	RX_CLK Period[1]	A11.3
4	RX_CLK pulse width low	35%	65%	RX_CLK Period[1]	A11.4

1 RX_CLK shall have a frequency of 25% of data rate of the received signal. See the IEEE 802.3 Specification.

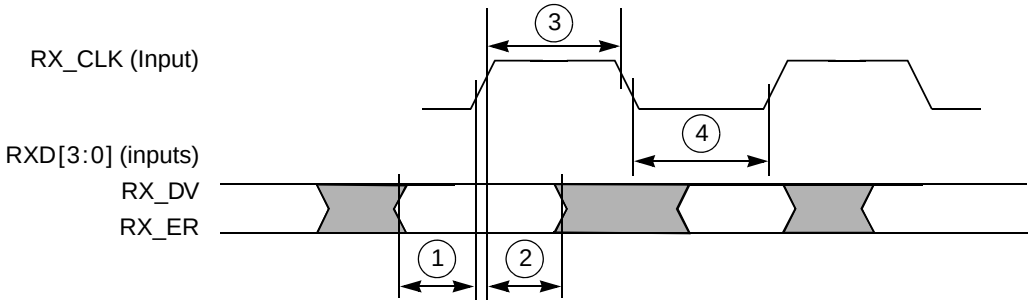

Figure 36. Ethernet Timing Diagram – MII Rx Signal

Table 33. MII Tx Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
5	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER invalid	3	—	ns	A11.5
6	TX_CLK rising edge to TXD[3:0], TX_EN, TX_ER valid	—	25	ns	A11.6
7	TX_CLK pulse width high	35%	65%	TX_CLK Period[1]	A11.7
8	TX_CLK pulse width low	35%	65%	TX_CLK Period[1]	A11.8

1 The TX_CLK frequency shall be 25% of the nominal transmit frequency, e.g., a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. See the IEEE 802.3 Specification.

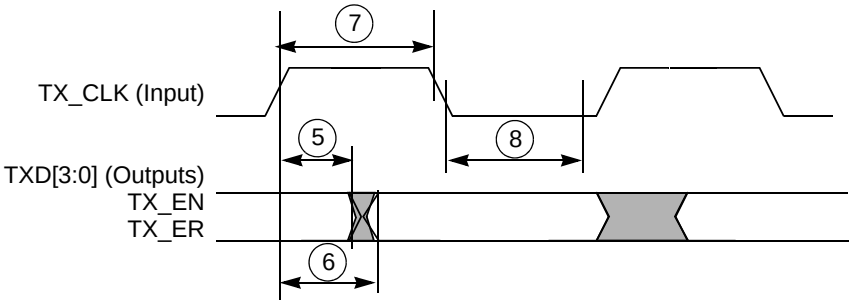

Figure 37. Ethernet Timing Diagram – MII Tx Signal

Table 34. MII Async Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
9	CRS, COL minimum pulse width	1.5	—	TX_CLK Period	A11.9

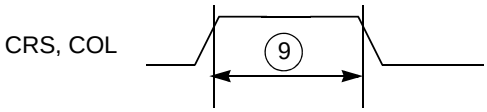

Figure 38. Ethernet Timing Diagram – MII Async

Table 35. MII Serial Management Channel Signal Timing

Symbol	Description	Min	Max	Unit	SpecID
10	MDC falling edge to MDIO output delay	0	25	ns	A11.10
11	MDIO (input) to MDC rising edge setup	10	—	ns	A11.11
12	MDIO (input) to MDC rising edge hold	0	—	ns	A11.12
13	MDC pulse width high[1]	160	—	ns	A11.13
14	MDC pulse width low[1]	160	—	ns	A11.14
15	MDC period[2]	400	—	ns	A11.15

1 MDC is generated by MPC5121e/MPC5123 with a duty cycle of 50% except when MII_SPEED in the FEC MII_SPEED control register is changed during operation. See the MPC5121e/MPC5123 Reference Manual.

2 The MDC period must be set to a value of less than or equal to 2.5 MHz (to be compliant with the IEEE MII characteristic) by programming the FEC MII_SPEED control register. See the MPC5121e/MPC5123 Reference Manual.

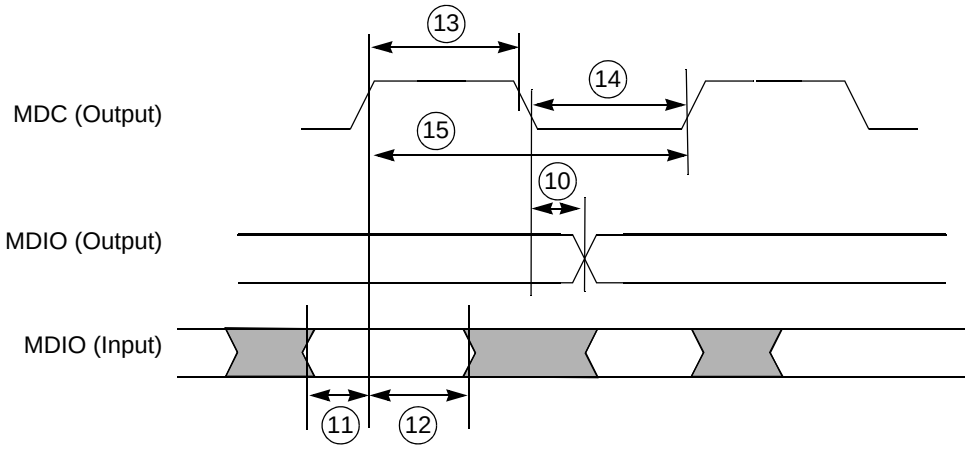

Figure 39. Ethernet Timing Diagram – MII Serial Management

3.3.12 USB ULPI

This section specifies the USB ULPI timing.

For more information refer to UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1, October 20, 2004.

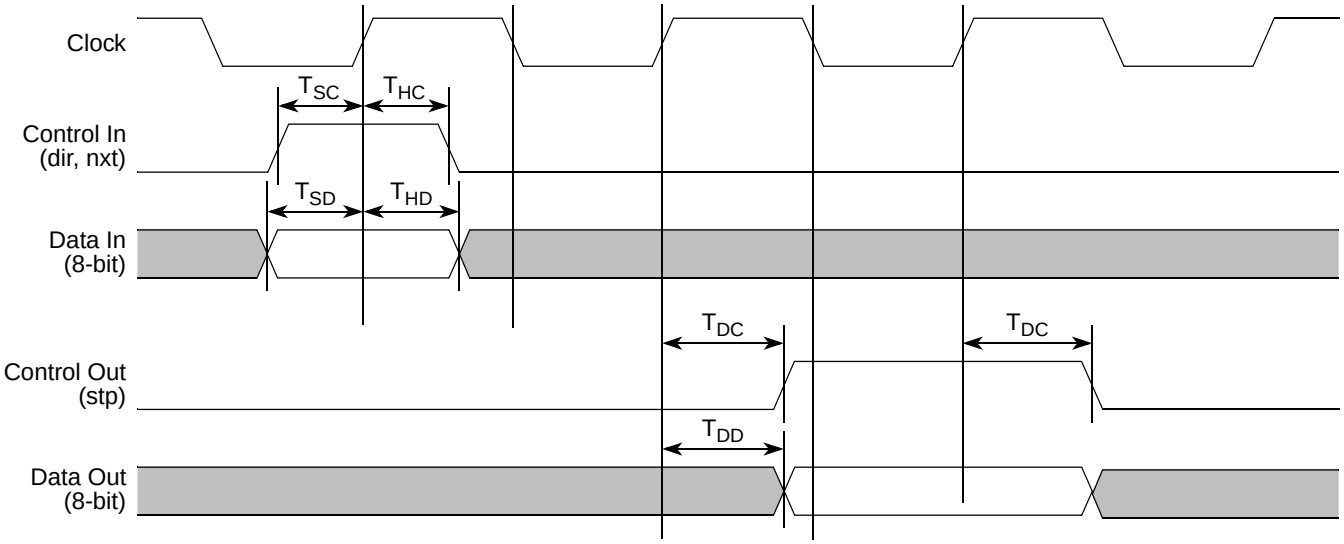

Figure 40. ULPI Timing Diagram

Table 36. Timing Specifications – ULPI

Symbol	Description	Min	Max	Units	SpecID
T_{CK}	Clock Period	15	—	ns	A12.1
T_{SC}, T_{SD}	Setup time (control in, 8-bit data in)	—	6.0	ns	A12.2
T_{HC}, T_{HD}	Hold time (control in, 8-bit data in)	0.0	—	ns	A12.3
T_{DC}, T_{DD}	Output delay (control out, 8-bit data out)	—	9.0	ns	A12.4

NOTE

Output timing is specified at a nominal 50 pF load.

3.3.13 On-Chip USB PHY

The USB PHY is an USB2.0 compatible PHY integrated on-chip. See Chapter 7 in the USB Specification Rev. 2.0 at www.usb.org.

3.3.14 SDHC

Figure 41 shows the timings of the SDHC.

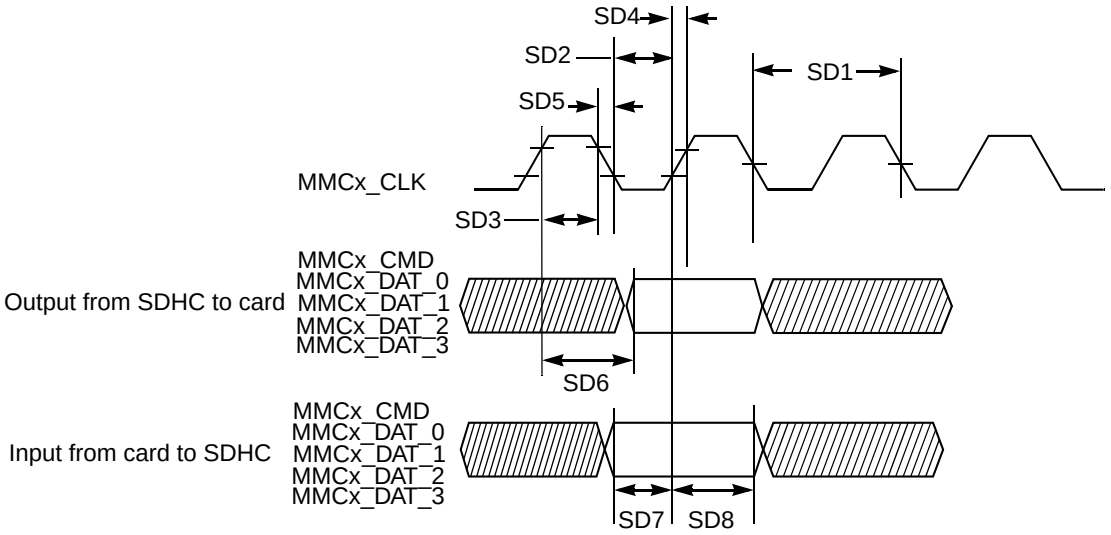

Figure 41. SDHC Timing Diagram

Table 37 lists the timing parameters.

Table 37. MMC/SD Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit	SpecID
Card Input Clock						
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz	A14.1
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz	A14.2
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz	A14.3
	Clock Frequency (Identification Mode)	f_{OD}[4]	100	400	kHz	A14.4
SD2	Clock Low Time (Full Speed/High Speed)	t_{WL}	10/7		ns	A14.5
SD3	Clock High Time (Full Speed/High Speed)	t_{WH}	10/7		ns	A14.6
SD4	Clock Rise Time (Full Speed/High Speed)	t_{TLH}		10/3	ns	A14.7
SD5	Clock Fall Time (Full Speed/High Speed)	t_{THL}		10/3	ns	A14.8
SDHC Output / Card Inputs CMD, DAT (Reference to CLK)						
SD6	SDHC Output Delay	t_{OD}	TH[5] – 3	TH+3	ns	A14.9
SDHC Input / Card Outputs CMD, DAT (Reference to CLK)						
SD7	SDHC Input Setup Time	t_{ISU}	2.5		ns	A14.10
SD8	SDHC Input Hold Time	t_{IH}	2.5		ns	A14.11

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal data transfer mode for SD/SDIO card, clock frequency can be any value between 0 ~ 25 MHz.

3 In normal data transfer mode for MMC card, clock frequency can be any value between 0 ~ 20 MHz.

4 In card identification mode, card clock must be 100 kHz ~ 400 kHz, voltage ranges from 2.7 to 3.6 V.

5 Suggested ClockPeriod = T, CLK_DIVIDER (in SDHC Clock Rate Register) = D, then TH = [(D + 1)/2]/(D + 1) × T where the value is rounded.

3.3.15 DIU

The DIU is a display controller designed to manage the TFT LCD display.

3.3.15.1 Interface to TFT LCD Panels, Functional Description

Figure 42 shows the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with positive polarity. The sequence of events for active matrix interface timing is:

- DIU_CLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, DIU_CLK runs continuously. This signal frequency could be from 5 to 100 MHz depending on the panel type.
- DIU_HSYNC causes the panel to start a new line. It always encompasses at least one DIU_CLK pulse.
- DIU_VSYNC causes the panel to start a new frame. It always encompasses at least one DIU_HSYNC pulse.
- DIU_DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

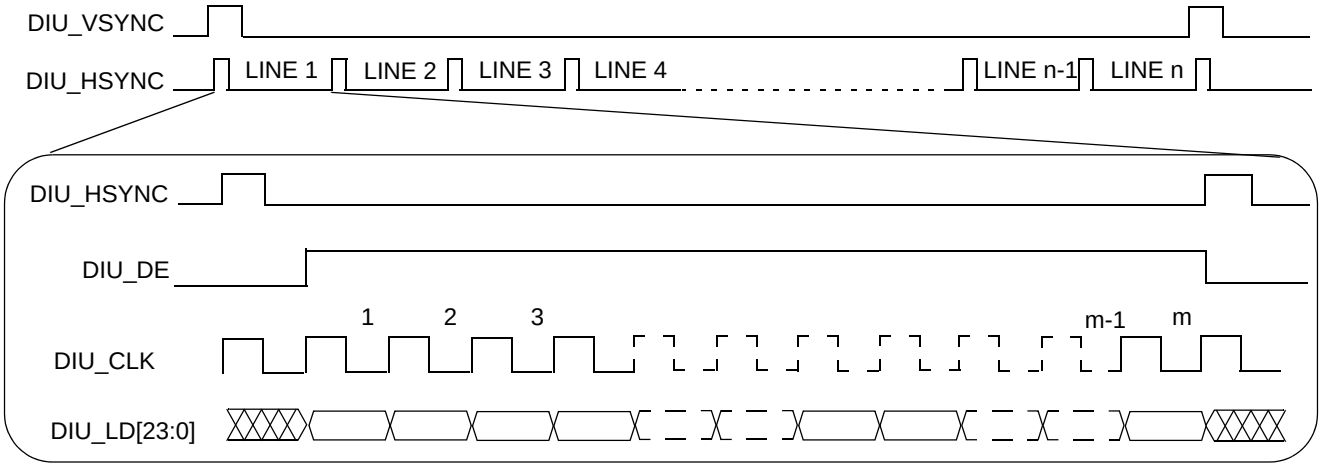

Figure 42. Interface Timing Diagram for TFT LCD Panels

3.3.15.2 Interface to TFT LCD Panels, Electrical Characteristics

Figure 43 shows the horizontal timing (timing of one line), including the horizontal sync pulse and the data. All parameters shown in the diagram are programmable. This timing diagram corresponds to positive polarity of the DIU_CLK signal (meaning the data and sync. signals change at the rising edge of it) and active-high polarity of the DIU_HSYNC, DIU_VSYNC and DIU_DE signal. You can select the polarity of the DIU_HSYNC and DIU_VSYNC signal via the SYN_POL register, whether active-high or active-low, the default is active-high. The DIU_DE signal is always active-high. And, pixel clock inversion and a flexible programmable pixel clock delay is also supported, programed via the DIU Clock Config Register (DCCR) in the system clock module.

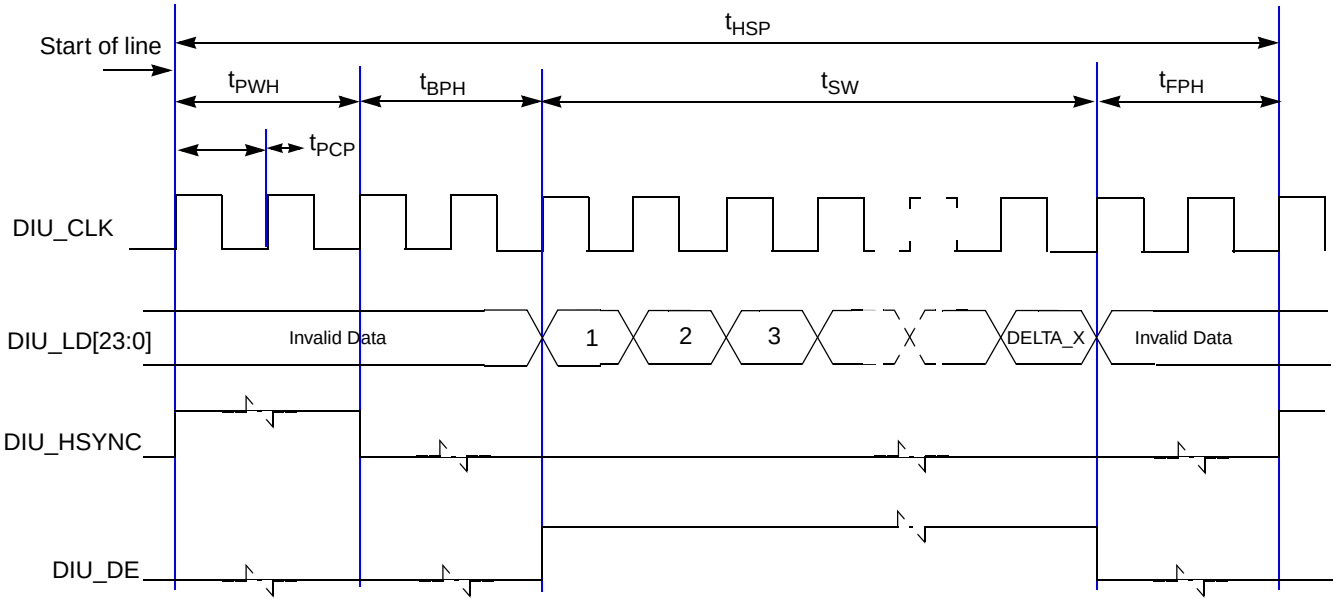

Figure 43. TFT LCD Interface Timing Diagram – Horizontal Sync Pulse

Figure 44 shows the vertical timing (timing of one frame), including the vertical sync pulse and the data. All parameters shown in the diagram are programmable.

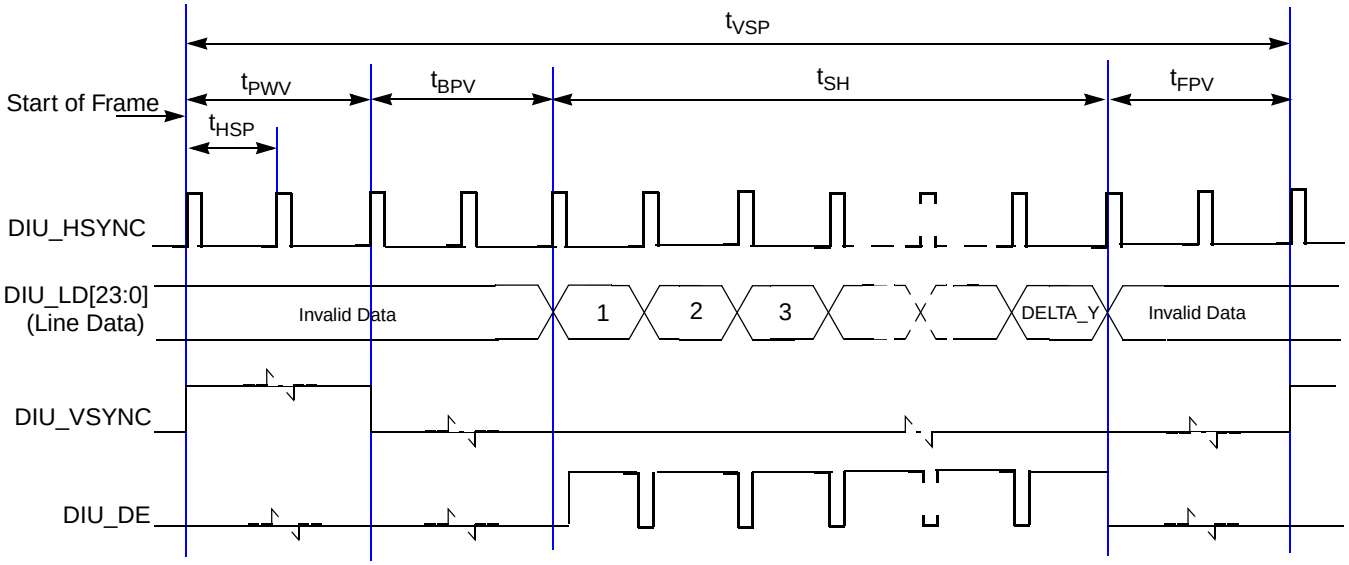

Figure 44. TFT LCD Interface Timing Diagram – Vertical Sync Pulse

Table 38 shows timing parameters of signals.

Table 38. LCD Interface Timing Parameters – Pixel Level

Name	Description	Value	Unit	SpecID
t_{PCP}	Display Pixel Clock Period	15[1]	ns	A15.1
t_{PWH}	HSYNC Pulse Width	PW_H × t_{PCP}	ns	A15.2
t_{BPH}	HSYNC Back Porch Width	BP_H × t_{PCP}	ns	A15.3

Table 38. LCD Interface Timing Parameters – Pixel Level (continued)

Name	Description	Value	Unit	SpecID
t_{FPH}	HSYNC Front Porch Width	FP_H × t_{PCP}	ns	A15.4
t_{SW}	Screen Width	DELTA_X × t_{PCP}	ns	A15.5
t_{HSP}	HSYNC (Line) Period	(PW_H + BP_H + DELTA_X + FP_H) × t_{PCP}	ns	A15.6
t_{PWV}	VSYNC Pulse Width	PW_V × t_{HSP}	ns	A15.7
t_{BPV}	VSYNC Back Porch Width	BP_V × t_{HSP}	ns	A15.8
t_{FPV}	VSYNC Front Porch Width	FP_V × t_{HSP}	ns	A15.9
t_{SH}	Screen Height	DELTA_Y × t_{HSP}	ns	A15.10
t_{VSP}	VSYNC (Frame) Period	(PW_V + BP_V + DELTA_Y + FP_H) × t_{HSP}	ns	A15.11

1 Display interface pixel clock period immediate value (in nanosecond).

The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register; The PW_H, BP_H, and FP_H parameters are programmed via the HSYN_PARA register; And the PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register. See appropriate section in the reference manual for detailed descriptions on these parameters.

Figure 45 shows the synchronous display interface timing for access level, and Table 39 lists the timing parameters.

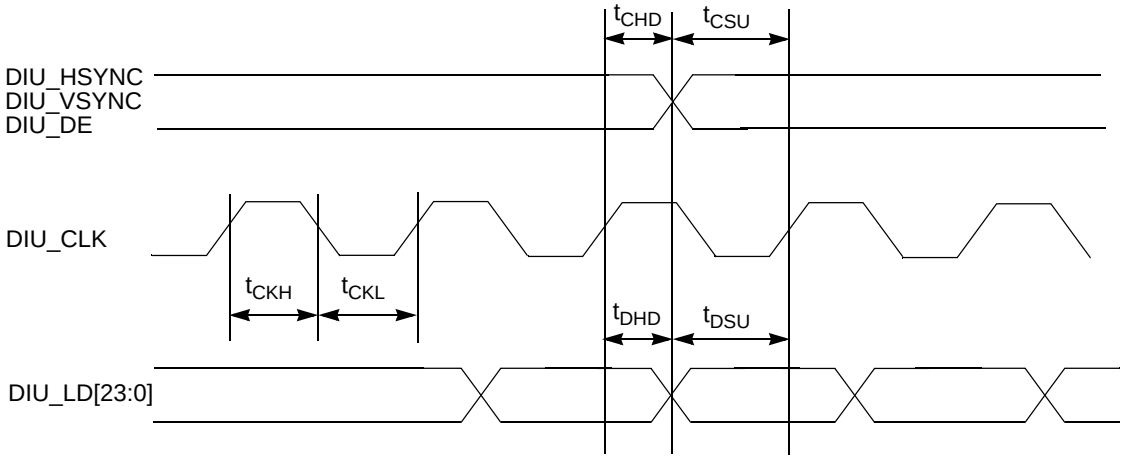

Figure 45. LCD Interface Timing Diagram – Access Level

Table 39. LCD Interface Timing Parameters – Access Level

Parameter	Description	Min	Typ	Max	Unit	SpecID
t_{CKH}	LCD Interface Pixel Clock High Time	t_{PCP} × 0.4	t_{PCP} × 0.5	t_{PCP} × 0.6	ns	A15.12
t_{CKL}	LCD Interface Pixel Clock Low Time	t_{PCP} × 0.4	t_{PCP} × 0.5	t_{PCP} × 0.6	ns	A15.13
t_{DSU}	LCD Interface Data Setup Time	5.0	—	—	ns	A15.14
t_{DHD}	LCD Interface Data Hold Time	6.0	—	—	ns	A15.15
t_{CSU}	LCD Interface Control Signal Setup Time	5.0	—	—	ns	A15.16
t_{CHD}	LCD Interface Control Signal Hold Time	6.0	—	—	ns	A15.17

3.3.16 SPDIF

The Sony/Philips Digital Interface (SPDIF) timing is totally asynchronous, therefore there is no need for relationship with the clock.

3.3.17 CAN

The CAN functions are available as TX and CAN3/4_RX pins at normal IO pads and as CAN1/2 RX pins at the VBAT_RTC domain. There is no filter for the WakeUp dominant pulse. Any High-to-Low edge can cause WakeUp, if configured.

3.3.18 I^2C

This section specifies the timing parameters of the Inter-Integrated Circuit (I^2C) interface. Refer to the I^2C Bus Specification.

Table 40. I^2C Input Timing Specifications – SCL and SDA

Symbol	Description	Min	Max	Units	SpecID
1	Start condition hold time	2	—	IP-Bus Cycle[1]	A18.1
2	Clock low time	8	—	IP-Bus Cycle[1]	A18.2
4	Data hold time	0.0	—	ns	A18.3
6	Clock high time	4	—	IP-Bus Cycle[1]	A18.4
7	Data setup time	0.0	—	ns	A18.5
8	Start condition setup time (for repeated start condition only)	2	—	IP-Bus Cycle[1]	A18.6
9	Stop condition setup time	2	—	IP-Bus Cycle[1]	A18.7

1 Inter Peripheral Clock is defined in the MPC5121e/MPC5123 *Reference Manual*.

Table 41. I^2C Output Timing Specifications – SCL and SDA

Symbol	Description	Min	Max	Units	SpecID
1[1]	Start condition hold time	6	—	IP-Bus Cycle[2]	A18.8
2[1]	Clock low time	10	—	IP-Bus Cycle[2]	A18.9
3[3]	SCL/SDA rise time	—	7.9	ns	A18.10
4[1]	Data hold time	7	—	IP-Bus Cycle[2]	A18.11
5[1]	SCL/SDA fall time	—	7.9	ns	A18.12
6[1]	Clock high time	10	—	IP-Bus Cycle[2]	A18.13
7[1]	Data setup time	2	—	IP-Bus Cycle[2]	A18.14
8[1]	Start condition setup time (for repeated start condition only)	20	—	IP-Bus Cycle[2]	A18.15
9[1]	Stop condition setup time	10	—	IP-Bus Cycle[2]	A18.16

1 Programming IFDR with the maximum frequency results in the minimum output timings listed. The I^2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

2 Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Inter Peripheral Clock is defined in the *MPC5121e/MPC5123 Reference Manual.*

NOTE

Output timing is specified at a nominal 50 pF load.

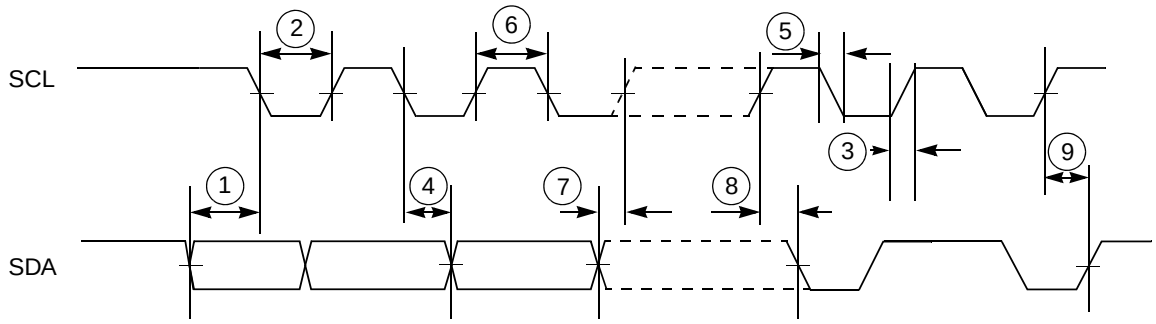

Figure 46. Timing Diagram – I²C Input/Output

3.3.19 J1850

See the MPC5121e/MPC5123 Reference Manual.

3.3.20 PSC

The Programmable Serial Controllers (PSC) support different modes of operation (UART, Codec, AC97, SPI). UART is an asynchronous interface, there is no AC characteristic.

3.3.20.1 Codec Mode (8,16,24 and 32-bit)/I²S Mode

Table 42. Timing Specifications – 8,16, 24, and 32-bit CODEC/I²S Master Mode

Symbol	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time, programmed in CCS register	40.0	—	—	ns	A20.1
2	Clock duty cycle	45	50	55	%[1]	A20.2
3	Bit Clock fall time	—	—	7.9	ns	A20.3
4	Bit Clock rise time	—	—	7.9	ns	A20.4
5	FrameSync valid after clock edge	—	—	8.4	ns	A20.5
6	FrameSync invalid after clock edge	—	—	8.4	ns	A20.6
7	Output Data valid after clock edge	—	—	9.3	ns	A20.7
8	Input Data setup time	6.0	—	—	ns	A20.8

1 Bit Clock cycle time

NOTE

Output timing is specified at a nominal 50 pF load.

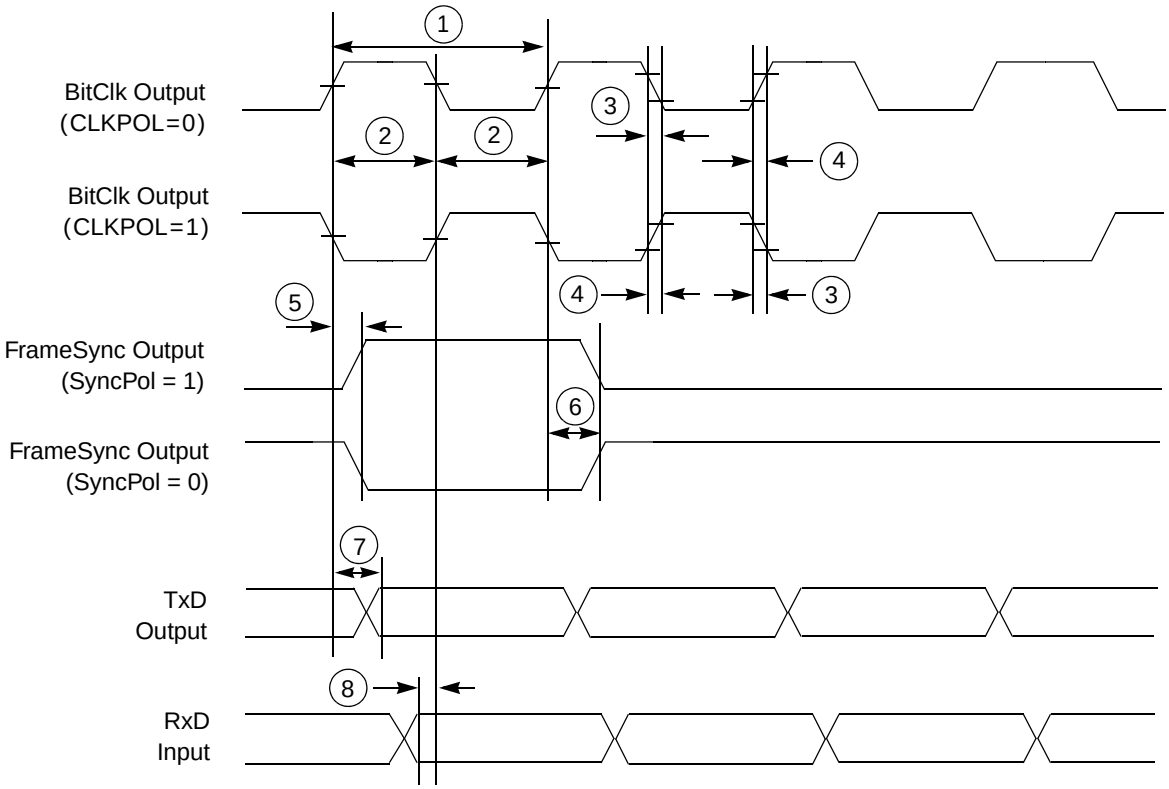

Figure 47. Timing Diagram – 8, 16, 24, and 32-bit CODEC/I^{2}S Master Mode

Table 43. Timing Specifications – 8, 16, 24, and 32-bit CODEC/I^{2}S Slave Mode

Symbol	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	40.0	—	—	ns	A20.9
2	Clock duty cycle	—	50	—	%[1]	A20.10
3	FrameSync setup time	1.0	—	—	ns	A20.11
4	Output Data valid after clock edge	—	—	14.0	ns	A20.12
5	Input Data setup time	1.0	—	—	ns	A20.13
6	Input Data hold time	1.0	—	—	ns	A20.14

1 Bit Clock cycle time

NOTE

Output timing is specified at a nominal 50 pF load.

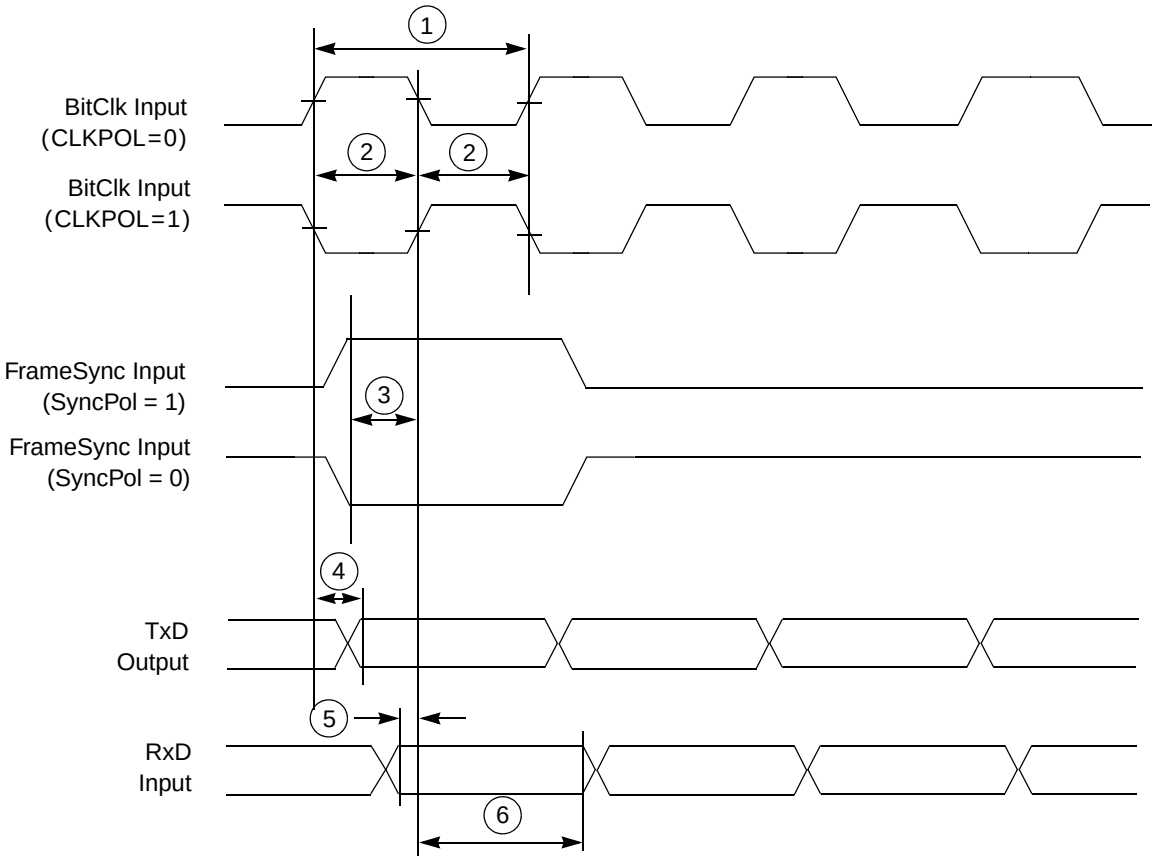

Figure 48. Timing Diagram – 8,16, 24, and 32-bit CODEC/I^{2}S Slave Mode

3.3.20.2 AC97 Mode

Table 44. Timing Specifications – AC97 Mode

Symbol	Description	Min	Typ	Max	Units	SpecID
1	Bit Clock cycle time	—	81.4	—	ns	A20.15
2	Clock pulse high time	—	40.7	—	ns	A20.16
3	Clock pulse low time	—	40.7	—	ns	A20.17
4	FrameSync valid after rising clock edge	—	—	13.0	ns	A20.18
5	Output Data valid after rising clock edge	—	—	14.0	ns	A20.19
6	Input Data setup time	1.0	—	—	ns	A20.20
7	Input Data hold time	1.0	—	—	ns	A20.21

NOTE

Output timing is specified at a nominal 50 pF load.

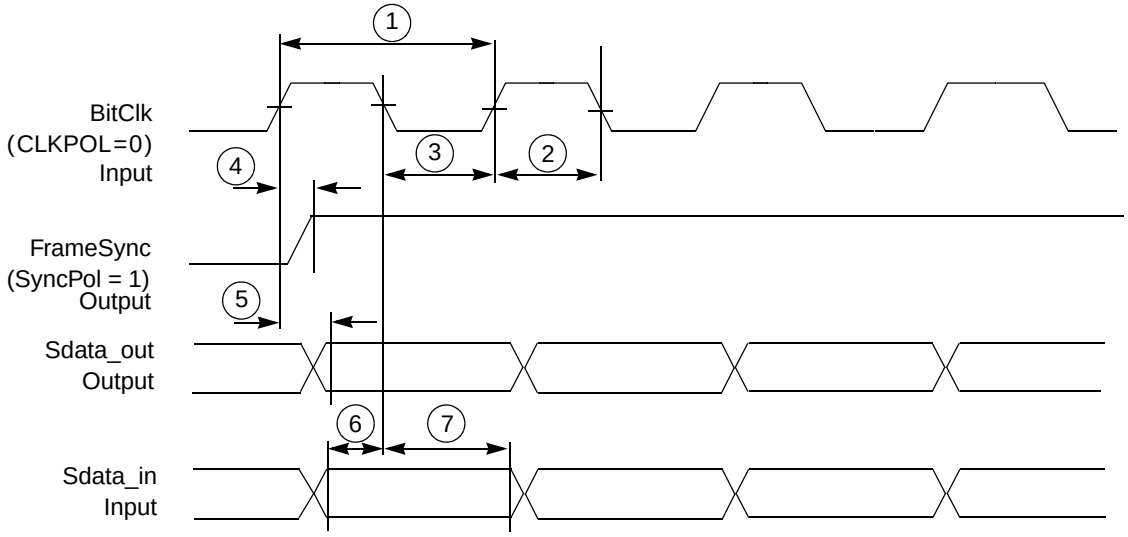

Figure 49. Timing Diagram – AC97 Mode

3.3.20.3 SPI Mode

Table 45. Timing Specifications – SPI Master Mode, Format 0 (CPHA = 0)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.26
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.27
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A20.28
4	Output Data valid after Slave Select ($\overline{SS}$)	—	8.9	ns	A20.29
5	Output Data valid after SCK	—	8.9	ns	A20.30
6	Input Data setup time	6.0	—	ns	A20.31
7	Input Data hold time	1.0	—	ns	A20.32
8	Slave disable lag time	—	TSCK	ns	A20.33
9	Sequential Transfer delay, programmable in the PSC CTUR / CTLR register	15.0	—	ns	A20.34
10	Clock falling time	—	7.9	ns	A20.35
11	Clock rising time	—	7.9	ns	A20.36

NOTE

Output timing is specified at a nominal 50 pF load.

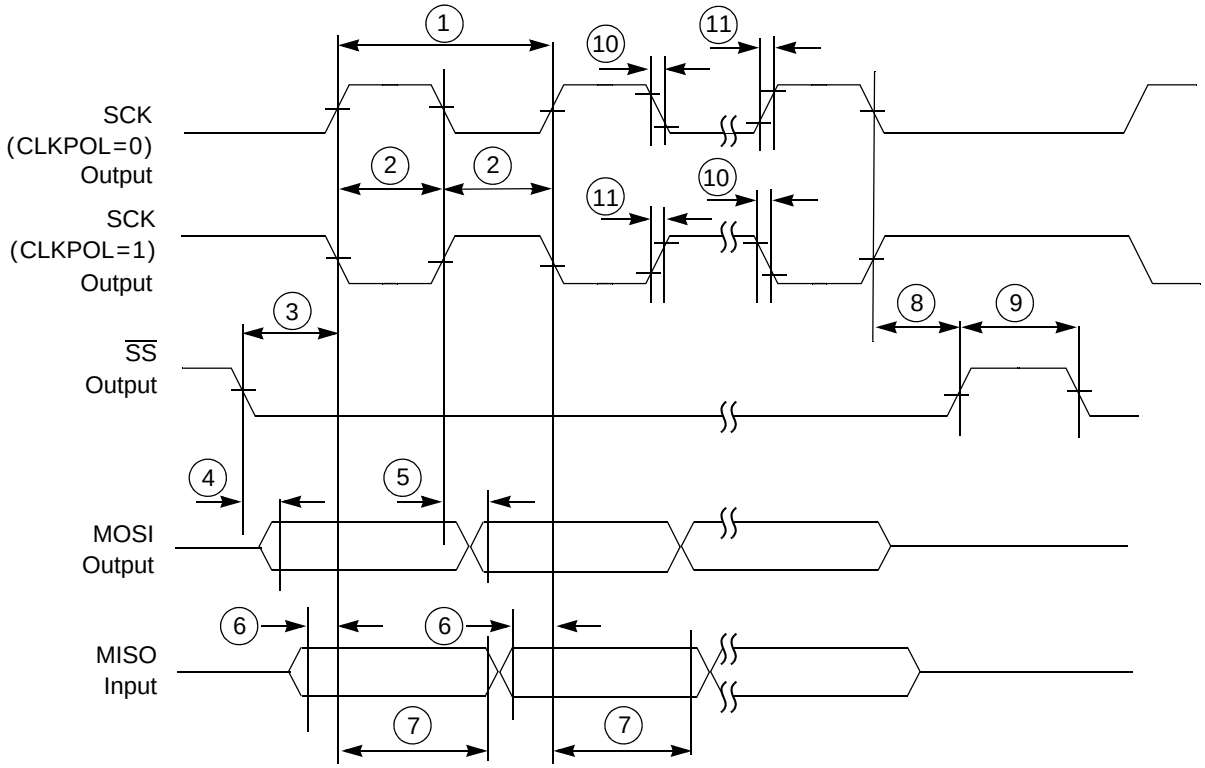

Figure 50. Timing Diagram – SPI Master Mode, Format 0 (CPHA = 0)

Table 46. Timing Specifications – SPI Slave Mode, Format 0 (CPHA = 0)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.37
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.38
3	Slave select clock delay	1.0	—	ns	A20.39
4	Input Data setup time	1.0	—	ns	A20.40
5	Input Data hold time	1.0	—	ns	A20.41
6	Output data valid after $\overline{SS}$	—	14.0	ns	A20.42
7	Output data valid after SCK	—	14.0	ns	A20.43
8	Slave disable lag time	0.0	—	ns	A20.44
9	Minimum Sequential Transfer delay = 2 × IP Bus clock cycle time	30.0	—	—	A20.45

NOTE

Output timing is specified at a nominal 50 pF load.

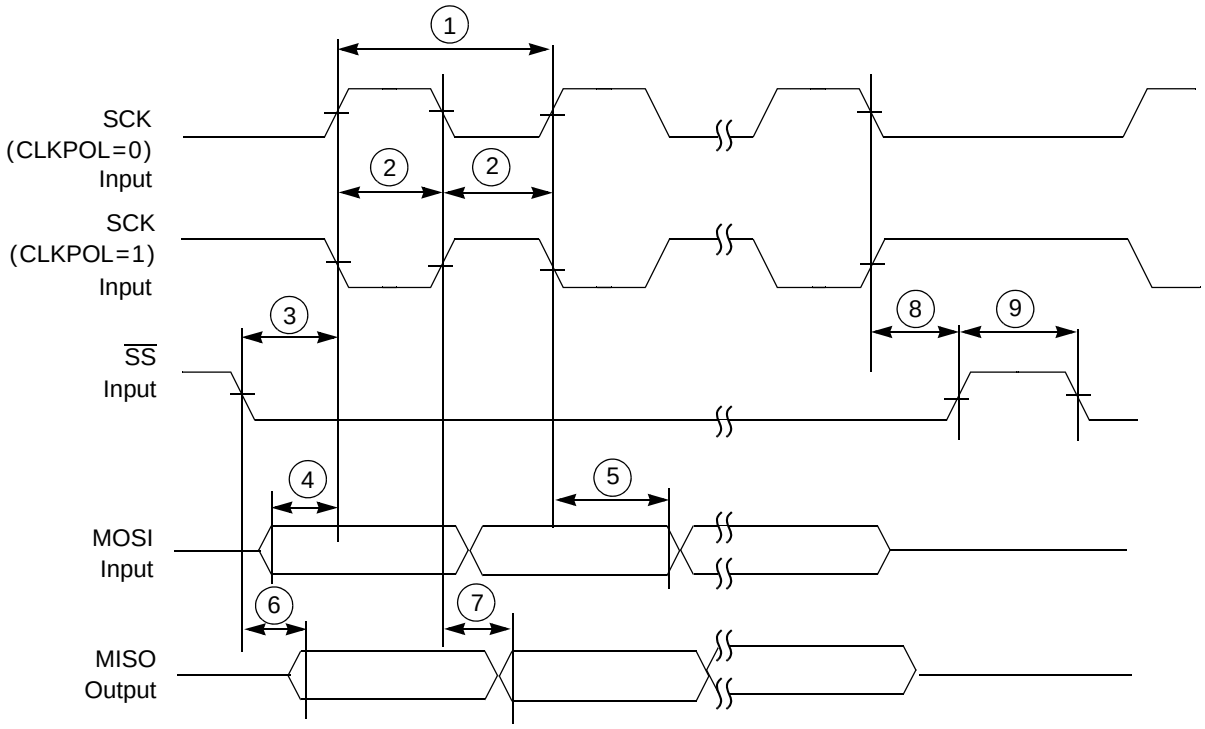

Figure 51. Timing Diagram – SPI Slave Mode, Format 0 (CPHA = 0)

Table 47. Timing Specifications – SPI Master Mode, Format 1 (CPHA = 1)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.46
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.47
3	Slave select clock delay, programable in the PSC CCS register	30.0	—	ns	A20.48
4	Output data valid	—	8.9	ns	A20.49
5	Input Data setup time	6.0	—	ns	A20.50
6	Input Data hold time	1.0	—	ns	A20.51
7	Slave disable lag time	—	TSCK	ns	A20.52
8	Sequential Transfer delay, programable in the PSC CTUR / CTLR register	15.0	—	ns	A20.53
9	Clock falling time	—	7.9	ns	A20.54
10	Clock rising time	—	7.9	ns	A20.55

NOTE

Output timing is specified at a nominal 50 pF load.

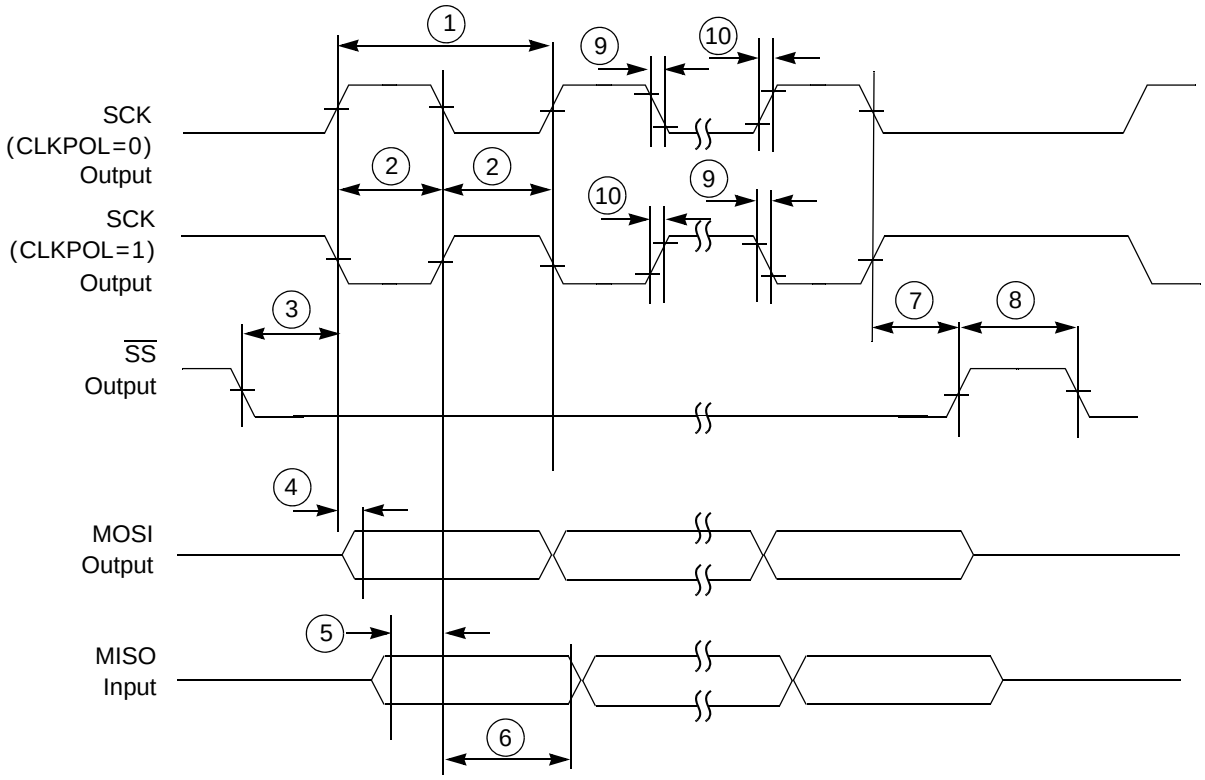

Figure 52. Timing Diagram – SPI Master Mode, Format 1 (CPHA = 1)

Table 48. Timing Specifications – SPI Slave Mode, Format 1 (CPHA = 1)

Symbol	Description	Min	Max	Units	SpecID
1	SCK cycle time, programable in the PSC CCS register	30.0	—	ns	A20.56
2	SCK pulse width, 50% SCK duty cycle	15.0	—	ns	A20.57
3	Slave select clock delay	0.0	—	ns	A20.58
4	Output data valid	—	14.0	ns	A20.59
5	Input Data setup time	2.0	—	ns	A20.60
6	Input Data hold time	1.0	—	ns	A20.61
7	Slave disable lag time	0.0	—	ns	A20.62
8	Minimum Sequential Transfer delay = 2 × IP-Bus clock cycle time	30.0	—	ns	A20.63

NOTE

Output timing is specified at a nominal 50 pF load.

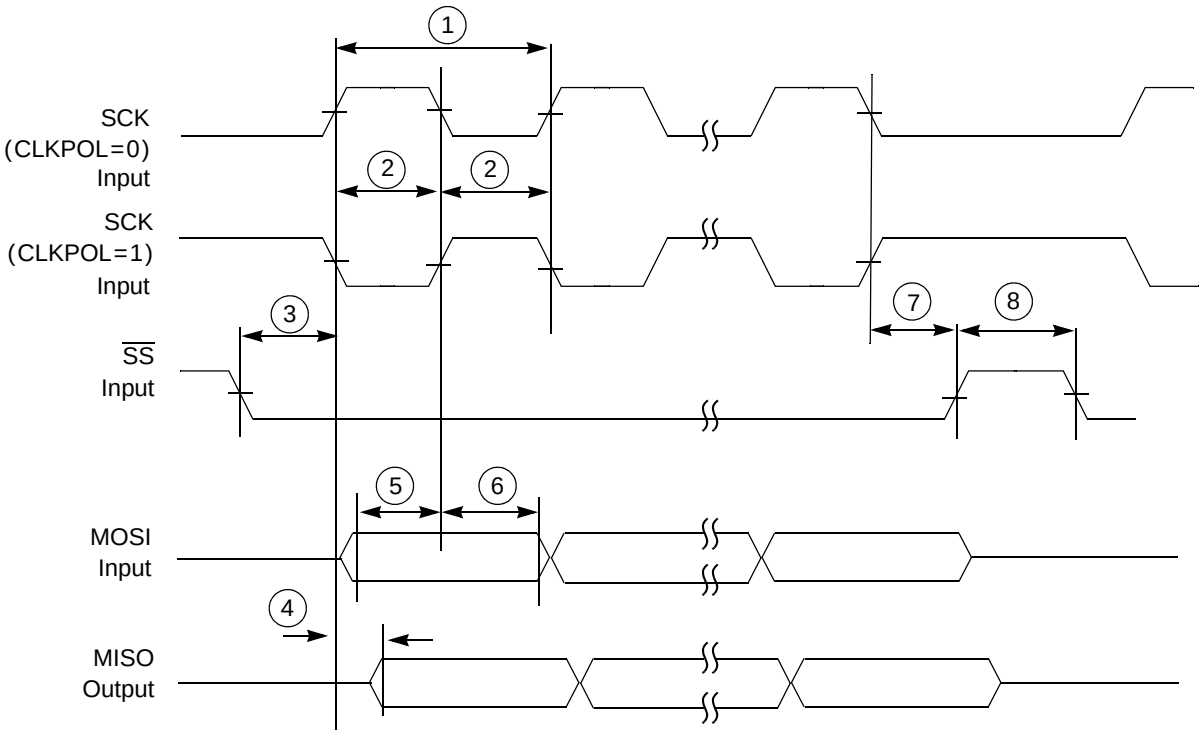

Figure 53. Timing Diagram – SPI Slave Mode, Format 1 (CPHA = 1)

3.3.21 GPIOs and Timers

The MPC5121e/MPC5123 contains several sets of I/Os that do not require special setup, hold, or valid requirements. The external events (GPIO or timer inputs) are asynchronous to the system clock. The inputs must be valid for at least tIOWID to ensure proper capture by the internal IP clock.

Table 49. GPIO/Timers Input AC Timing Specifications

Symbol	Description	Min	Unit	SpecID
t_{IOWID}	GPIO/Timers inputs—minimum pulse width	2T[1]	ns	A21.1

1 T is the IP bus clock cycle. T= 12 ns is the minimum value (for the maximum IP bus frequency of 83 MHz).

3.3.22 Fusebox

Table 50 gives the Fusebox specification.

Table 50. Fusebox Characteristics

Symbol	Description	Min	Max	Units	SpecID
t_{FUSEWR}	Program time[1] for Fuse	125	—	us	A22.1
I_{FUSEWR}	Program current to program one fuse bit	—	10	mA	A22.2

1 The program length is defined by the value defined in the EPM_PGM_LENGTH bits of the IIM module.

3.3.23 IEEE 1149.1 (JTAG)

Table 51. JTAG Timing Specification

Symbol	Characteristic	Min	Max	Unit	SpecID
—	TCK frequency of operation	0	25	MHz	A23.1
1	TCK cycle time	40	—	ns	A23.2
2	TCK clock pulse width measured at 1.5V	1.08	—	ns	A23.3
3	TCK rise and fall times	0	3	ns	A23.4
4	$\overline{\text{TRST}}$ setup time to tck falling edge[1]	10	—	ns	A23.5
5	$\overline{\text{TRST}}$ assert time	5	—	ns	A23.6
6	Input data setup time[2]	5	—	ns	A23.7
7	Input data hold time[2]	15	—	ns	A23.8
8	TCK to output data valid[3]	0	30	ns	A23.9
9	TCK to output high impedance[3]	0	30	ns	A23.10
10	TMS, TDI data setup time.	5	—	ns	A23.11
11	TMS, TDI data hold time.	1	—	ns	A23.12
12	TCK to TDO data valid.	0	15	ns	A23.13
13	TCK to TDO high impedance.	0	15	ns	A23.14

1 $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.

2 Non-test, other than TDI and TMS, signal input timing with respect to TCK.

3 Non-test, other than TDO, signal output timing with respect to TCK.

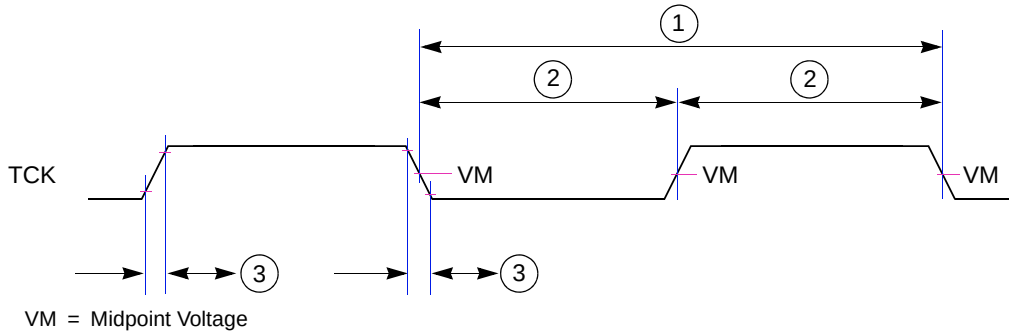

Figure 54. Timing Diagram – JTAG Clock Input

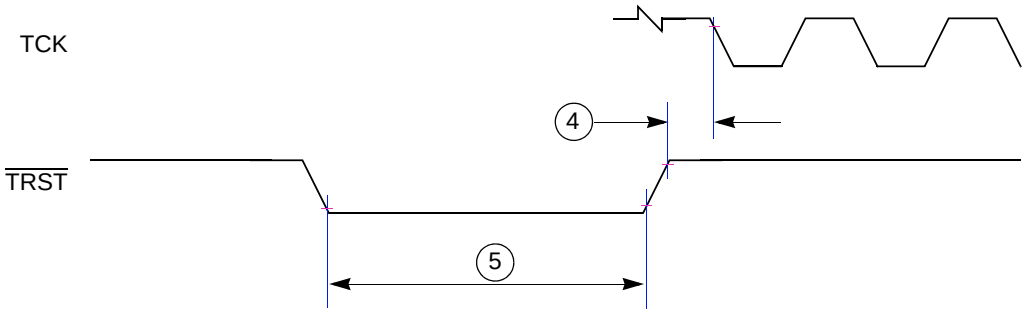

Figure 55. Timing Diagram – JTAG TRST

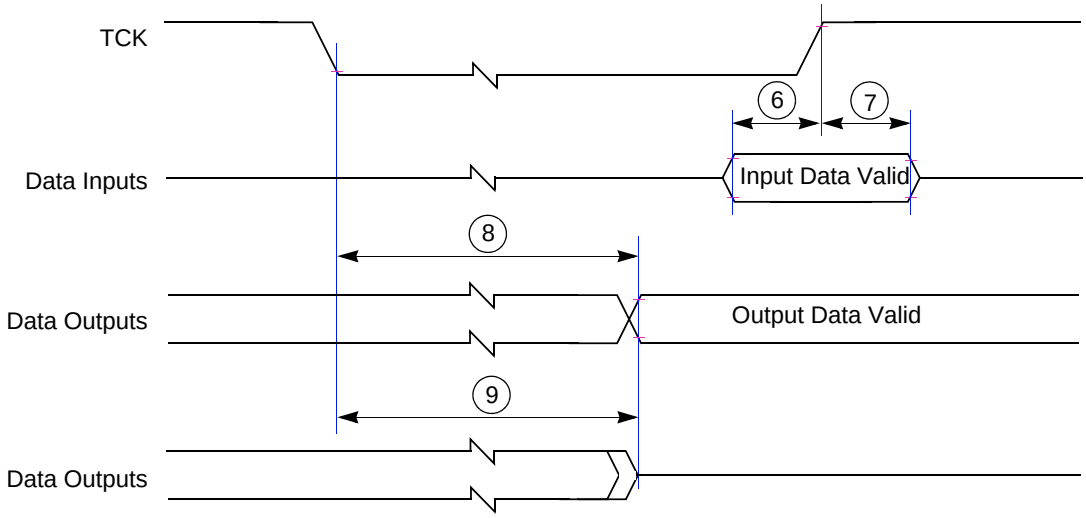

Figure 56. Timing Diagram – JTAG Boundary Scan

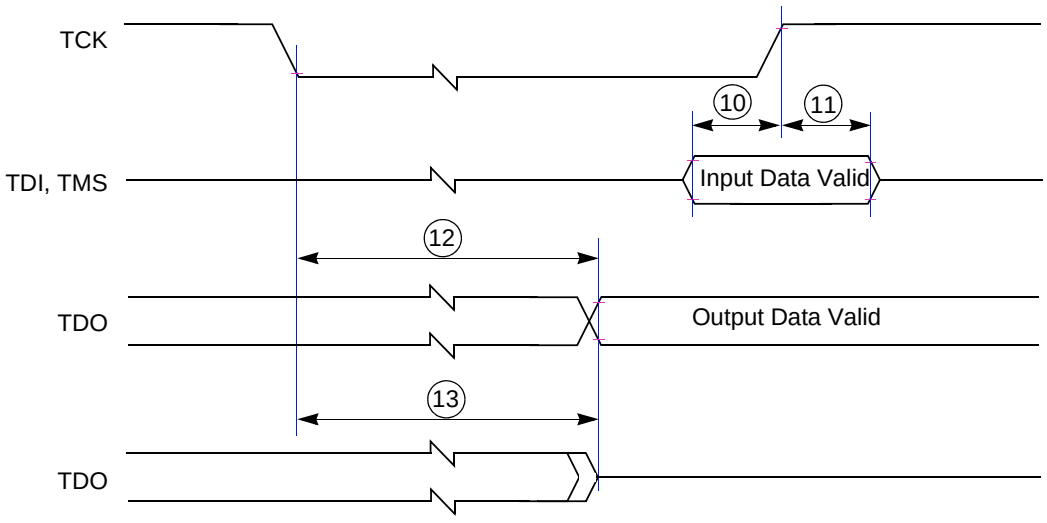

Figure 57. Timing Diagram – Test Access Port

3.3.24 VIU

The Video Input Unit (VIU) is an interface which accepts the ITU656 format compatible video stream.

Figure 58 shows the VIU interface timing and Table 52 lists the timing parameters.

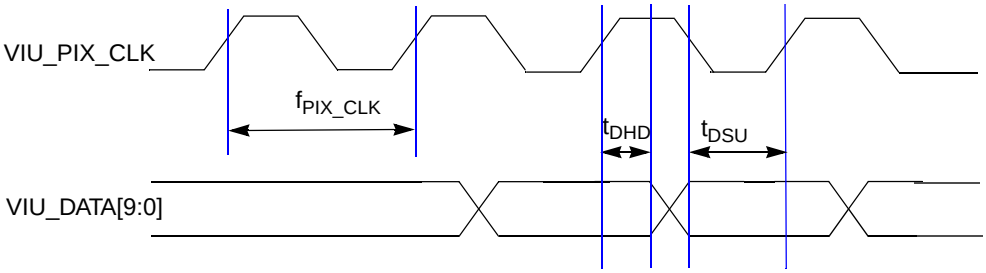

Figure 58. VIU Interface Timing Diagram

Table 52. VIU Interface Timing Parameters

Parameter	Description	Min	Typ	Max	Unit	SpecID
f_{PIX_CK}	VIU Pixel Clock Frequency	—	—	83	MHz	A24.1
t_{DSU}	VIU Data Setup Time	2.5	—	—	ns	A24.2
t_{DHD}	VIU Data Hold Time	2.5	—	—	ns	A24.3

4 System Design Information

4.1 Power Up/Down Sequencing

Power sequencing between the 1.4 V power supply V_{DD_CORE} and the remaining supplies is required to prevent excessive current during power up phase.

The required power sequence is as follows:

- Use 12 V/millisecond or slower time for all supplies.
- Power up V_{DD_IO}, PLL_AV_{DD}, V_{BAT_RTC} (if not applied permanently), $V_{DD\_MEM\_IO}$, USB PHY, and SATA PHY supplies first in any order and then power up V_{DD_CORE}. If required, AV_{DD_FUSEWR} should be powered up afterwards.
- All the supplies must reach the specified operating conditions before the $\overline{\text{PORESET}}$ can be released.
- For power down, drop AV_{DD_FUSEWR} to 0 V first, drop V_{DD_CORE} to 0 V, and then drop all other supplies.
- V_{DD_CORE} should not exceed V_{DD_IO}, $V_{DD\_MEM\_IO}$, V_{BAT_RTC}, or PLL_AV_{DD}s by more than 0.4 V at any time, including power-up.

4.2 System and CPU Core AVDD Power Supply Filtering

Each of the independent PLL power supplies require filtering external to the device. The following drawing Figure 59 is a recommendation for the required filter circuit.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits.

All traces should be as low impedance as possible, especially ground pins to the ground plane.

The filter for System/Core $PLLV_{DD}$ to V_{SS} should be connected to the power and ground planes, respectively, not fingers of the planes.

In addition to keeping the filter components for System/Core $PLLV_{DD}$ as close as practical to the body of the MPC5121e as previously mentioned, special care should be taken to avoid coupling switching power supply noise or digital switching noise onto the portion of that supply between the filter and the MPC5121e.

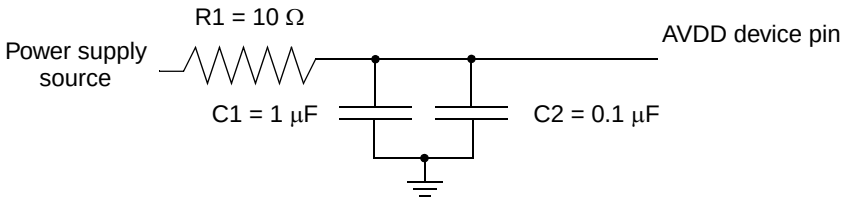

Figure 59. Power Supply Filtering

The capacitors for C2 in Figure 59 should be rated X5R or better due to temperature performance. It is recommended to add a bypass capacitance of at least 1 µF for the V_{BAT_RTC} pin.

4.3 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to V_{DD_IO}. Unused active high inputs should be connected to V_{SS}. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} and V_{SS} pins of the MPC5121e/MPC5123.

The unused AV_{DD_FUSEWR} power should be connected to V_{SS} directly or via a resistor.

For DDR or LPDDR modes the unused pins MVTT[3:0] for DDR2 Termination voltage can be unconnected.

The SATA PHY needs to be powered even if it is not used in an application. In this case, you should not enable the SATA oscillator and the SATA PHY by software.

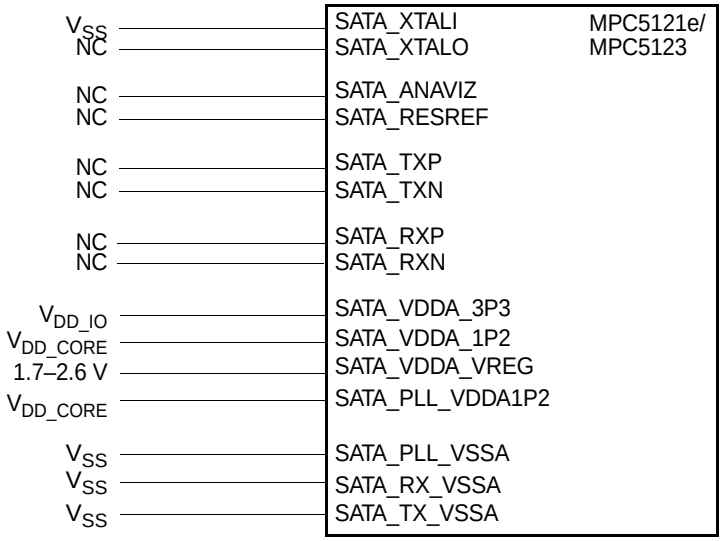

Figure 60. Recommended Connection for Pins of Unused SATA PHY

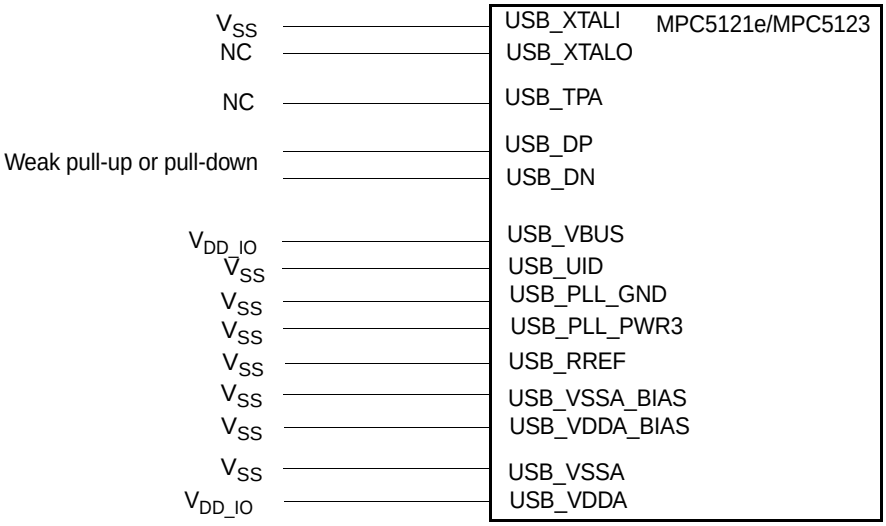

Figure 61. Recommended connection for pins of unused USB PHY

4.4 Pull-Up/Pull-Down Resistor Requirements

The MPC5121e/MPC5123 requires external pull-up or pull-down resistors on certain pins.

4.4.1 Pull-Down Resistor Requirements for TEST pin

The MPC5121e/MPC5123 requires a pull-down resistor on the test pin TEST.

4.4.2 Pull-Up Requirements for the PCI Control Lines

PCI control signals always require pull-up resistors on the motherboard (not the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes PCI_FRAME, PCI_TRDY, PCI_IRDY, PCI_DEVSEL, PCI_STOP, PCI_SERR, PCI_PERR, and PCI_REQ.

Refer to the PCI Local Bus specification.

4.5 JTAG

The MPC5121e/MPC5123 provides you with an IEEE 1149.1 JTAG interface to facilitate board/system testing. It also provides a Common On-Chip Processor (COP) Interface, which shares the IEEE 1149.1 JTAG port.

The COP Interface provides access to the MPC5121e/MPC5123's embedded e300 processor and to other on-chip resources. This interface provides a means for executing test routines and for performing software development and debug functions.

4.5.1 TRST

Boundary scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification but is provided on all processors that implement the Power Architecture. To obtain a reliable power-on reset performance, the TRST signal must be asserted during power-on reset.

4.5.1.1 TRST and PORESET

The JTAG interface can control the direction of the MPC5121e/MPC5123 I/O pads via the boundary scan chain. The JTAG module must be reset before the MPC5121e/MPC5123 comes out of power-on reset; do this by asserting TRST before PORESET is released.

For more details refer to the Reset and JTAG Timing Specification.

Figure 62. PORESET vs. TRST

4.5.2 e300 COP/BDM Interface

There are two possibilities to connect the JTAG interface: using it with a COP connector and without a COP connector.

4.5.2.1 Boards Interfacing the JTAG Port via a COP Connector

The MPC5121e/MPC5123 functional pin interface and internal logic provides access to the embedded e300 processor core through the Freescale standard COP/BDM interface. Table 53 gives the COP/BDM interface signals. The pin order shown reflects only the COP/BDM connector order.

Table 53. COP/BDM Interface Signals

BDM Pin #	MPC5121e/MPC5123 I/O Pin	BDM Connector	Internal Pull Up/Down	External Pull Up/Down	I/O[1]
16	—	GND	—	—	—
15	$\overline{\text{CKSTP\_OUT}}$	ckstp_out	—	10 kΩ Pull-up	I
14	—	KEY	—	—	—
13	$\overline{\text{HRESET}}$	hreset	Pull-up	10 kΩ Pull-up	O
12	—	GND	—	—	—
11	$\overline{\text{SRESET}}$	sreset	Pull-up	10 kΩ Pull-up	O
10	—	N/C	—	—	—
9	TMS	tms	Pull-up	10 kΩ Pull-up	O
8	$\overline{\text{CKSTP\_IN}}$	ckstp_in	—	10 kΩ Pull-up	O
7	TCK	tck	Pull-up	10 kΩ Pull-up	O
6	—	VDD[2]	—	—	—
5	See Note[3]	halted[3]	—	—	I
4	$\overline{\text{TRST}}$	trst	Pull-up	10 kΩ Pull-up	O
3	TDI	tdi	Pull-up	10 kΩ Pull-up	O
2	See Note[4]	qack[4]	—	—	O
1	TDO	tdo	—	—	I

1 With respect to the emulator tool's perspective:
Input is really an output from the embedded e300 core.
Output is really an input to the core.

2 From the board under test, power sense for chip power.

3 HALTED is not available from e300 core.

4 Input to the e300 core to enable/disable soft-stop condition during breakpoints. MPC5121e/MPC5123 internally ties CORE_QACK to GND in its normal/functional mode (always asserted).

For a board with a COP (common on-chip processor) connector that accesses the JTAG interface and needs to reset the JTAG module, only wiring $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ is not recommended.

To reset the MPC5121e/MPC5123 via the COP connector, the $\overline{\text{HRESET}}$ pin of the COP should be connected to the $\overline{\text{HRESET}}$ pin of the MPC5121e/MPC5123. The circuitry shown in Figure 63 allows the COP to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ separately, while any other board sources can drive $\overline{\text{PORESET}}$.

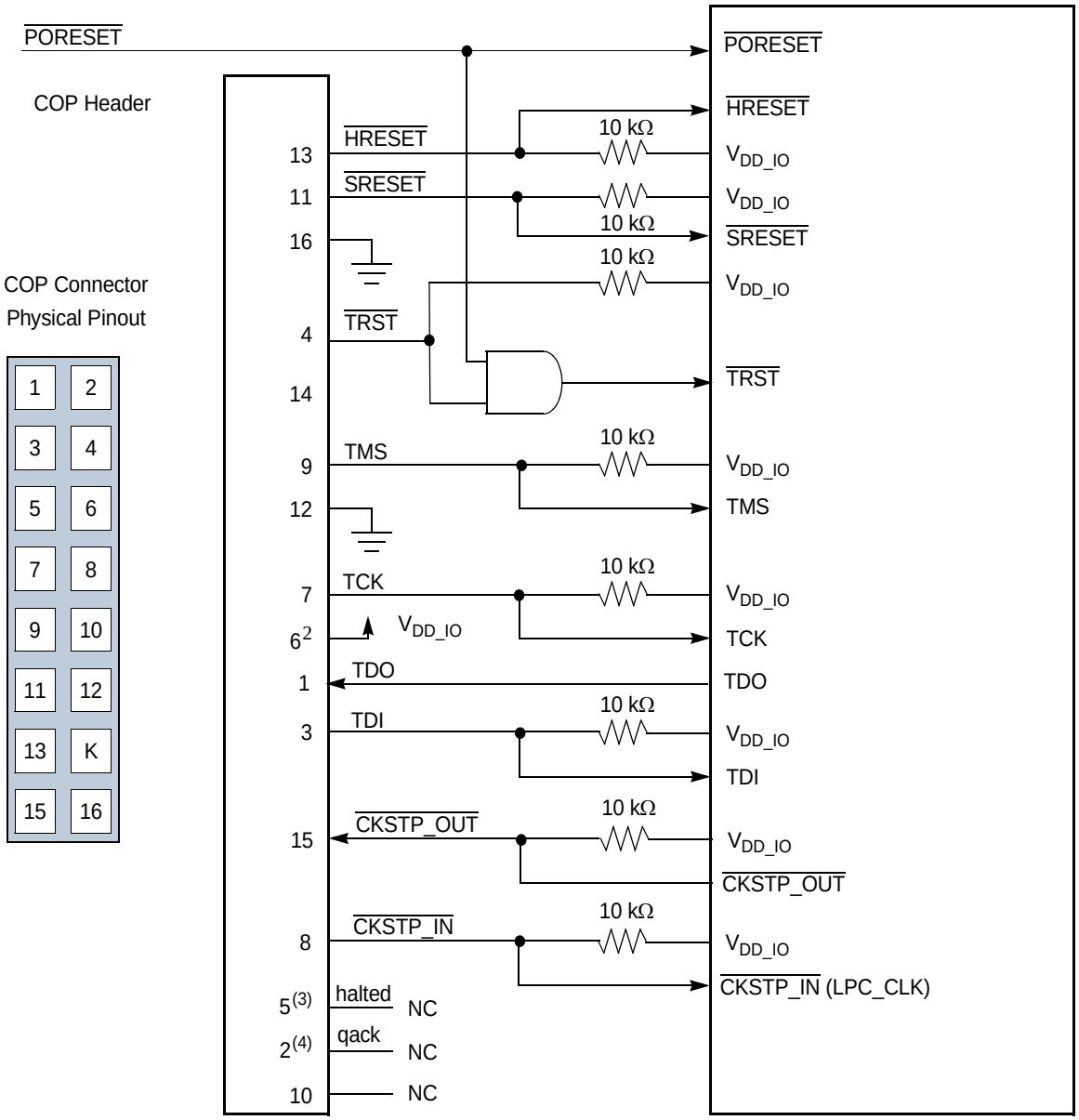

Figure 63. COP Connector Diagram

4.5.2.2 Boards Without COP Connector

If the JTAG interface is not used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$, so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted. This ensures that the JTAG scan chain is initialized during power on. Figure 64 shows the connection of the JTAG interface without COP connector.

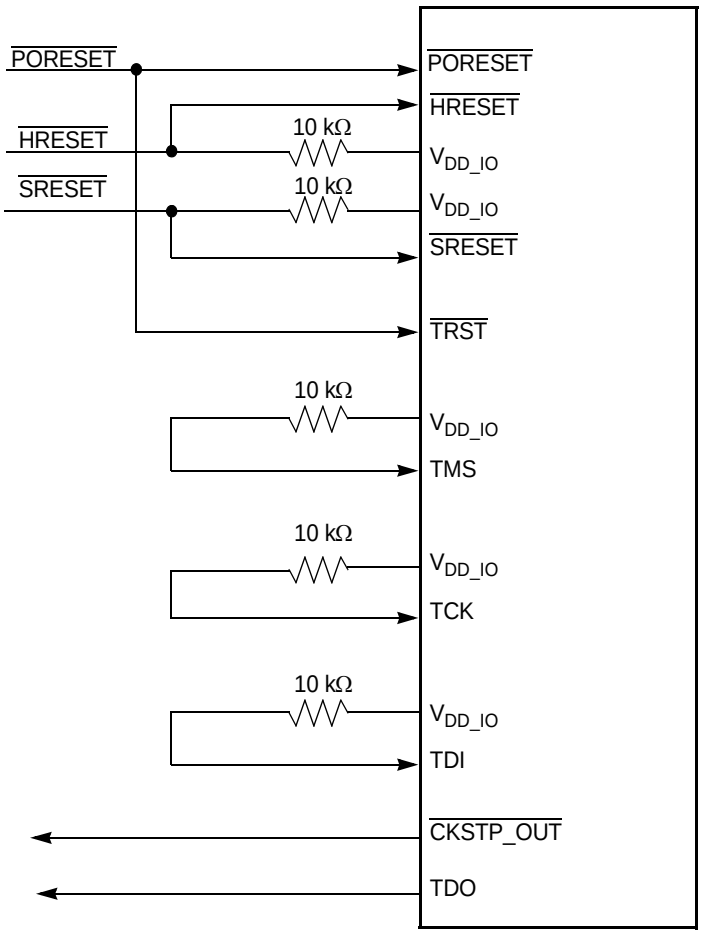

Figure 64. $\overline{\text{TRST}}$ Wiring for Boards without COP Connector

5 Package Information

This section details package parameters and dimensions. The MPC5121e/MPC5123 is available in a Thermally Enhanced Plastic Ball Grid Array (TEPBGA), see Section 5.1, “Package Parameters,” and Section 5.2, “Mechanical Dimensions,” for information on the TEPBGA.

5.1 Package Parameters

Table 54. TEPBGA Parameters

Package outline	27 mm × 27 mm
Interconnects	516
Pitch	1.00 mm
Module height (typical)	2.25 mm
Solder Balls	96.5 Sn/3.5Ag (VY *package)*
Ball diameter (typical)	0.6 mm

5.2 Mechanical Dimensions

Figure 65 shows the mechanical dimensions and bottom surface nomenclature of the MPC5121e/MPC5123 516 PBGA package.

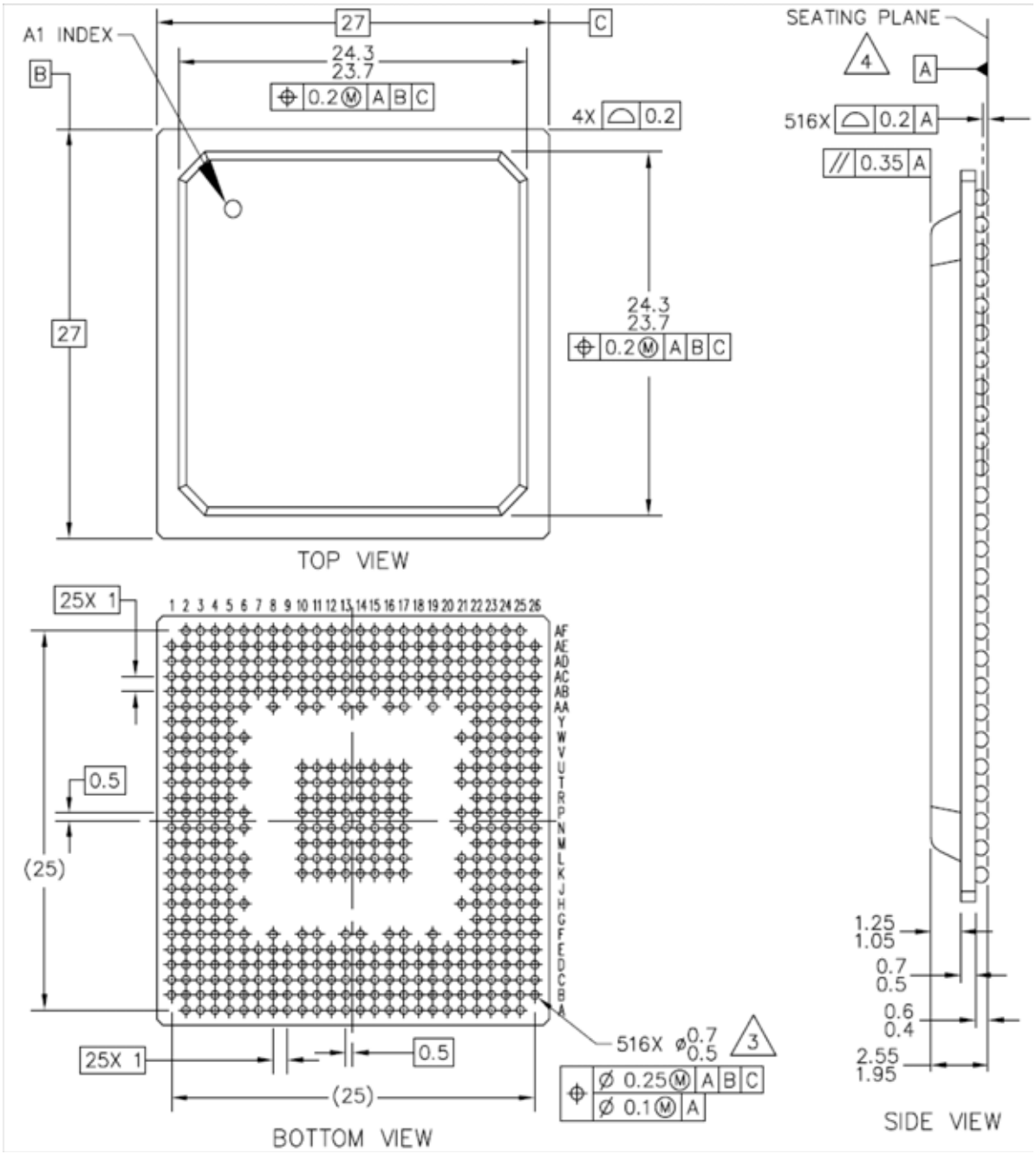

Figure 65. Mechanical Dimension and Bottom Surface Nomenclature of the MPC5121e/MPC5123 TEPBGA

1 All dimensions are in millimeters.
2 Dimensions and tolerances per ASME Y14.5M-1994.
3 Maximum solder ball diameter measured parallel to datum A.
4 Datum A, the seating plane, is determined by the spherical crowns of the solder balls.

6 Product Documentation

This Data Sheet is labeled as a particular type: Product Preview, Advance Information, or Technical Data. Definitions of these types are available at: http://www.freescale.com.

Table 55 provides a revision history for this document.

Table 55. Document Revision History

Revision	Substantive Change(s)
Rev. 0, DraftA	First Draft (5/2008)
Rev. 0, DraftB	Second Draft (5/2008)
Rev. 0, DraftC	Third Draft (7/2008)
Rev. 1	Advance Information (10/2008)
Rev. 2	Technical Data (2/2009)
Rev. 3	Technical Data (2/2009). Corrected Table 5, Footnote 3.
Rev. 3.1	Technical Data (12/2009). Interim release for removing AVDD_FUSERD throughout document, changing pin D9 to VDD_IO, and adding D9 to list of pins for VDD_IO.
Rev. 4	Technical Data (1/2010). Minor editorial and graphical updates. No technical updates.
Rev 5	— Updated table “DDR and DDR2 SDRAM Timing Specification”, removed the row of ‘MCK AC differential crosspoint voltage' . — Updated table “Thermal Resistance Data”. — Added table “NFC Timing Characteristics in Symmetric Mode ”and added figure “Read data latch timing in Symmetric Mode”. —Published as Rev. 5

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