

# 74VHC574FT

## 1. Functional Description

- Octal D-Type Flip Flop with 3-State Outputs

## 2. General

The 74VHC574FT is an advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ).

When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up.

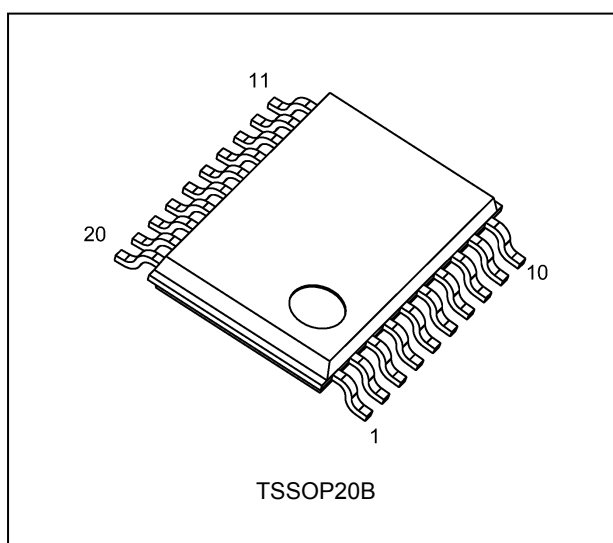
This circuit prevents device destruction due to mismatched supply and input voltages.

## 3. Features

- (1) AEC-Q100 (Rev. H) (Note 1)
- (2) Wide operating temperature range:  $T_{opr} = -40$  to  $125$  °C
- (3) High speed:  $f_{MAX} = 180$  MHz (typ.) at  $V_{CC} = 5.0$  V
- (4) Low power dissipation:  $I_{CC} = 4.0$   $\mu$ A (max) at  $T_a = 25$ °C
- (5) High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- (6) Power-down protection is provided on all inputs.
- (7) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (8) Wide operating voltage range:  $V_{CC(opr)} = 2.0$  V to  $5.5$  V
- (9) Low noise:  $V_{OLP} = 1.0$  V (max)
- (10) Pin and function compatible with the 74 series  
(74AC/HC/AHC/LV etc.) 574 type.

Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

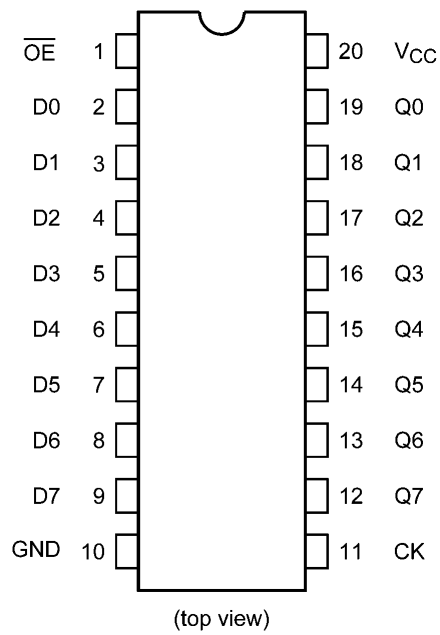
## 4. Packaging



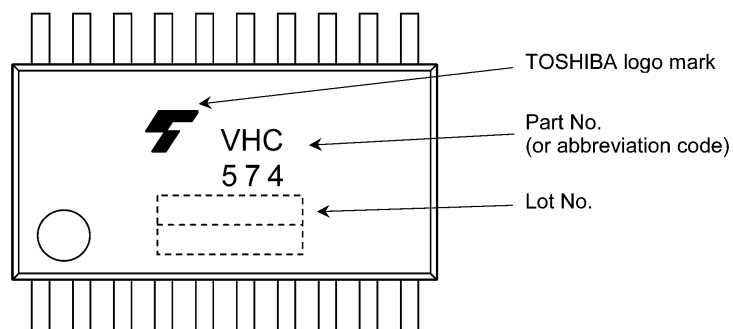
Start of commercial production

2013-03

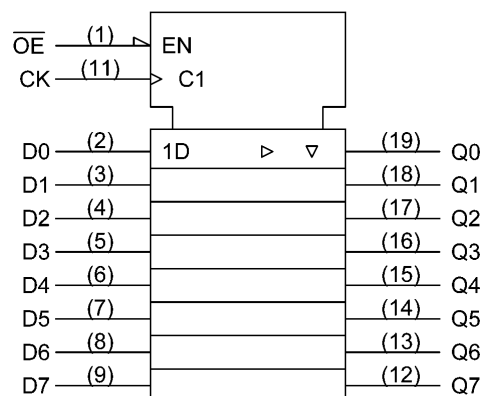
**5. Pin Assignment**






**6. Marking**



**7. IEC Logic Symbol**

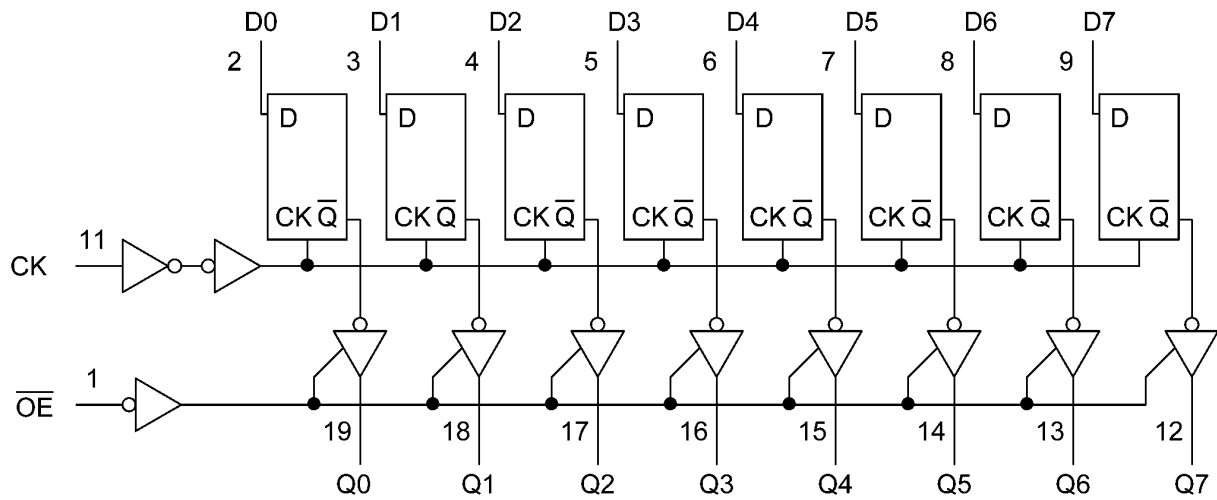


**8. Truth Table**

Inputs			Output
$\overline{OE}$	CK	D	
H	X	X	Z
L		X	$Q_n$
L		L	L
L		H	H

X: Don't care  
 Z: High impedance  
 $Q_n$ : No change

**9. System Diagram**



**10. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	$V_{CC}$		-0.5 to 7.0	V
Input voltage	$V_{IN}$		-0.5 to 7.0	V
Output voltage	$V_{OUT}$		-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$		-20	mA
Output diode current	$I_{OK}$		$\pm 20$	mA
Output current	$I_{OUT}$		$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$		$\pm 75$	mA
Power dissipation	$P_D$	(Note 1)	180	mW
Storage temperature	$T_{stg}$		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of  $T_a = -40$  to 85 °C. From  $T_a = 85$  to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

**11. Operating Ranges (Note)**

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$		2.0 to 5.5	V
Input voltage	$V_{IN}$		0 to 5.5	V
Output voltage	$V_{OUT}$		0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		-40 to 125	°C
Input rise and fall times	$dt/dv$	$V_{CC} = 3.3 \pm 0.3$ V	0 to 100	ns/V
		$V_{CC} = 5 \pm 0.5$ V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

**12. Electrical Characteristics**

**12.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Typ.	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	$V_{CC} \times 0.3$	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
			4.5	4.4	4.5	—		
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.94	—	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
			$I_{OL} = 8\text{ mA}$	4.5	—	—	0.36	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		5.5	—	—	$\pm 0.25$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	—	$\pm 0.1$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	—	4.0	$\mu\text{A}$

**12.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				3.0 to 5.5	—	$V_{CC} \times 0.3$	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
			$I_{OH} = -8\text{ mA}$	4.5	3.80	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
			$I_{OL} = 8\text{ mA}$	4.5	—	0.44	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND		5.5	—	$\pm 2.50$	$\mu\text{A}$
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND		0 to 5.5	—	$\pm 1.0$	$\mu\text{A}$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND		5.5	—	40.0	$\mu\text{A}$

**12.3. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $125$  °C)**

Characteristics	Symbol	Test Condition		$V_{CC}$ (V)	Min	Max	Unit
High-level input voltage	$V_{IH}$	—		2.0	1.50	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	
Low-level input voltage	$V_{IL}$	—		2.0	—	0.50	V
				3.0 to 5.5	—	$V_{CC} \times 0.3$	
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
				$I_{OH} = -4$ mA	3.0	2.40	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
				$I_{OL} = 4$ mA	3.0	—	
3-state output OFF-state leakage current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	—	5.5	—	$\pm 10.0$	$\mu A$
				—	—	—	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5$ V or GND	—	0 to 5.5	—	$\pm 2.0$	$\mu A$
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	—	5.5	—	80.0	$\mu A$

**12.4. Timing Requirements (Unless otherwise specified,  $T_a = 25$ °C, Input:  $t_r = t_f = 3$  ns)**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	ns
Minimum setup time	$t_s$	—	$3.3 \pm 0.3$	3.5	ns
			$5.0 \pm 0.5$	3.5	ns
Minimum hold time	$t_h$	—	$3.3 \pm 0.3$	1.5	ns
			$5.0 \pm 0.5$	1.5	ns

**12.5. Timing Requirements (Unless otherwise specified,  $T_a = -40$  to  $85$ °C, Input:  $t_r = t_f = 3$  ns)**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum setup time	$t_s$	—	$3.3 \pm 0.3$	3.5	ns
			$5.0 \pm 0.5$	3.5	
Minimum hold time	$t_h$	—	$3.3 \pm 0.3$	1.5	ns
			$5.0 \pm 0.5$	1.5	

**12.6. Timing Requirements (Unless otherwise specified,  $T_a = -40$  to  $125$  °C, Input:  $t_r = t_f = 3$  ns)**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum setup time	$t_s$	—	$3.3 \pm 0.3$	4.5	ns
			$5.0 \pm 0.5$	4.0	
Minimum hold time	$t_h$	—	$3.3 \pm 0.3$	1.5	ns
			$5.0 \pm 0.5$	1.5	

**12.7. AC Characteristics (Unless otherwise specified, T<sub>a</sub> = 25 °C, Input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)**

Characteristics	Symbol	Note	Test Condition	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max	Unit
Propagation delay time (CK-Q)	t <sub>PLH</sub> , t <sub>PHL</sub>		—	3.3 ± 0.3	15	—	8.5	13.2	ns
					50	—	11.0	16.7	
				5.0 ± 0.5	15	—	5.6	8.6	
					50	—	7.1	10.6	
3-state output enable time	t <sub>PZL</sub> , t <sub>PZH</sub>		R <sub>L</sub> = 1 kΩ	3.3 ± 0.3	15	—	8.2	12.8	ns
					50	—	10.7	16.3	
				5.0 ± 0.5	15	—	5.9	9.0	
					50	—	7.4	11.0	
3-state output disable time	t <sub>PLZ</sub> , t <sub>PHZ</sub>		R <sub>L</sub> = 1 kΩ	3.3 ± 0.3	50	—	11.0	15.0	ns
				5.0 ± 0.5	50	—	7.1	10.1	
Maximum clock frequency	f <sub>MAX</sub>		—	3.3 ± 0.3	15	80	125	—	MHz
					50	50	75	—	
				5.0 ± 0.5	15	130	180	—	
					50	85	115	—	
Output skew	t <sub>osLH</sub> , t <sub>osHL</sub>	(Note 1)	—	3.3 ± 0.3	50	—	—	1.5	ns
				5.0 ± 0.5	50	—	—	1.0	
Input capacitance	C <sub>IN</sub>		—			—	4	10	pF
Output capacitance	C <sub>OUT</sub>		—			—	6	—	pF
Power dissipation capacitance	C <sub>PD</sub>	(Note 2)	—			—	28	—	pF

Note 1: Parameter guaranteed by design. (t<sub>osLH</sub> = |t<sub>PLHM</sub> - t<sub>PLHN</sub>|, t<sub>osHL</sub> = |t<sub>PMLM</sub> - t<sub>PMLN</sub>|)

Note 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8 \text{ (per F/F)}$$

And the total C<sub>PD</sub> when n pcs of F/F operate can be gained by the following equation.

$$C_{PD} \text{ (total)} = 20 + 8 \times n$$

**12.8. AC Characteristics (Unless otherwise specified, T<sub>a</sub> = -40 to 85 °C, Input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)**

Characteristics	Symbol	Note	Test Condition	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Max	Unit
Propagation delay time (CK-Q)	t <sub>PLH</sub> , t <sub>PHL</sub>		—	3.3 ± 0.3	15	1.0	15.5	ns
					50	1.0	19.0	
				5.0 ± 0.5	15	1.0	10.0	
					50	1.0	12.0	
3-state output enable time	t <sub>PZL</sub> , t <sub>PZH</sub>		R <sub>L</sub> = 1 kΩ	3.3 ± 0.3	15	1.0	15.0	ns
					50	1.0	18.5	
				5.0 ± 0.5	15	1.0	10.5	
					50	1.0	12.5	
3-state output disable time	t <sub>PLZ</sub> , t <sub>PHZ</sub>		R <sub>L</sub> = 1 kΩ	3.3 ± 0.3	50	1.0	17.0	ns
				5.0 ± 0.5	50	1.0	11.5	
Maximum clock frequency	f <sub>MAX</sub>		—	3.3 ± 0.3	15	65	—	MHz
					50	45	—	
				5.0 ± 0.5	15	110	—	
					50	75	—	
Output skew	t <sub>osLH</sub> , t <sub>osHL</sub>	(Note 1)	—	3.3 ± 0.3	50	—	1.5	ns
				5.0 ± 0.5	50	—	1.0	
Input capacitance	C <sub>IN</sub>		—			—	10	pF

Note 1: Parameter guaranteed by design. (t<sub>osLH</sub> = |t<sub>PLHM</sub> - t<sub>PLHN</sub>|, t<sub>osHL</sub> = |t<sub>PMLM</sub> - t<sub>PMLN</sub>|)

**12.9. AC Characteristics**  
 (Unless otherwise specified,  $T_a = -40$  to  $125$  °C, Input:  $t_r = t_f = 3$  ns)

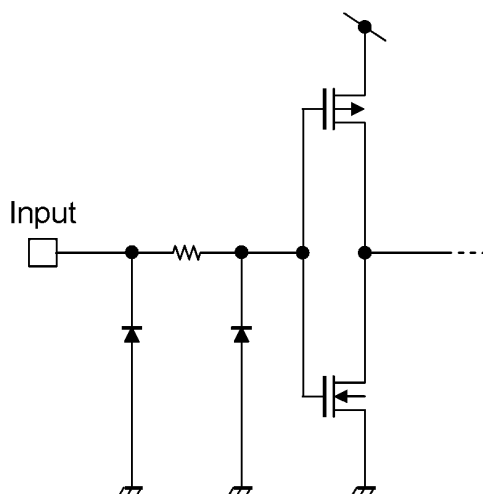
Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit
Propagation delay time	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	1.0	17.5	ns
					50	1.0	21.0	
				$5.0 \pm 0.5$	15	1.0	11.5	
					50	1.0	13.5	
3-state output enable time	$t_{PZL}, t_{PZH}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	15	1.0	17.0	ns
					50	1.0	20.5	
				$5.0 \pm 0.5$	15	1.0	12.0	
					50	1.0	14.0	
3-state output disable time	$t_{PLZ}, t_{PHZ}$		$R_L = 1$ k $\Omega$	$3.3 \pm 0.3$	50	1.0	19.0	ns
				$5.0 \pm 0.5$	50	1.0	13.0	
Maximum clock frequency	$f_{MAX}$		—	$3.3 \pm 0.3$	15	60	—	MHz
					50	40	—	
				$5.0 \pm 0.5$	15	100	—	
					50	65	—	
Output skew	$t_{osLH}, t_{osHL}$	(Note 1)	—	$3.3 \pm 0.3$	50	—	1.5	ns
				$5.0 \pm 0.5$	50	—	1.0	
Input capacitance	$C_{IN}$		—			—	10	pF

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLHM} - t_{PLHN}|$ ,  $t_{osHL} = |t_{PHLM} - t_{PHLN}|$ )

**12.10. Noise Characteristics** (Unless otherwise specified,  $T_a = 25$ °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Quiet output maximum dynamic $V_{OL}$	$V_{OLP}$	$C_L = 50$ pF	5.0	0.8	1.0	V
Quiet output minimum dynamic $V_{OL}$	$V_{OLV}$	$C_L = 50$ pF	5.0	-0.8	-1.0	
Minimum high-level dynamic input voltage	$V_{IHD}$	$C_L = 50$ pF	5.0	—	3.5	
Maximum low-level dynamic input voltage	$V_{ILD}$	$C_L = 50$ pF	5.0	—	1.5	

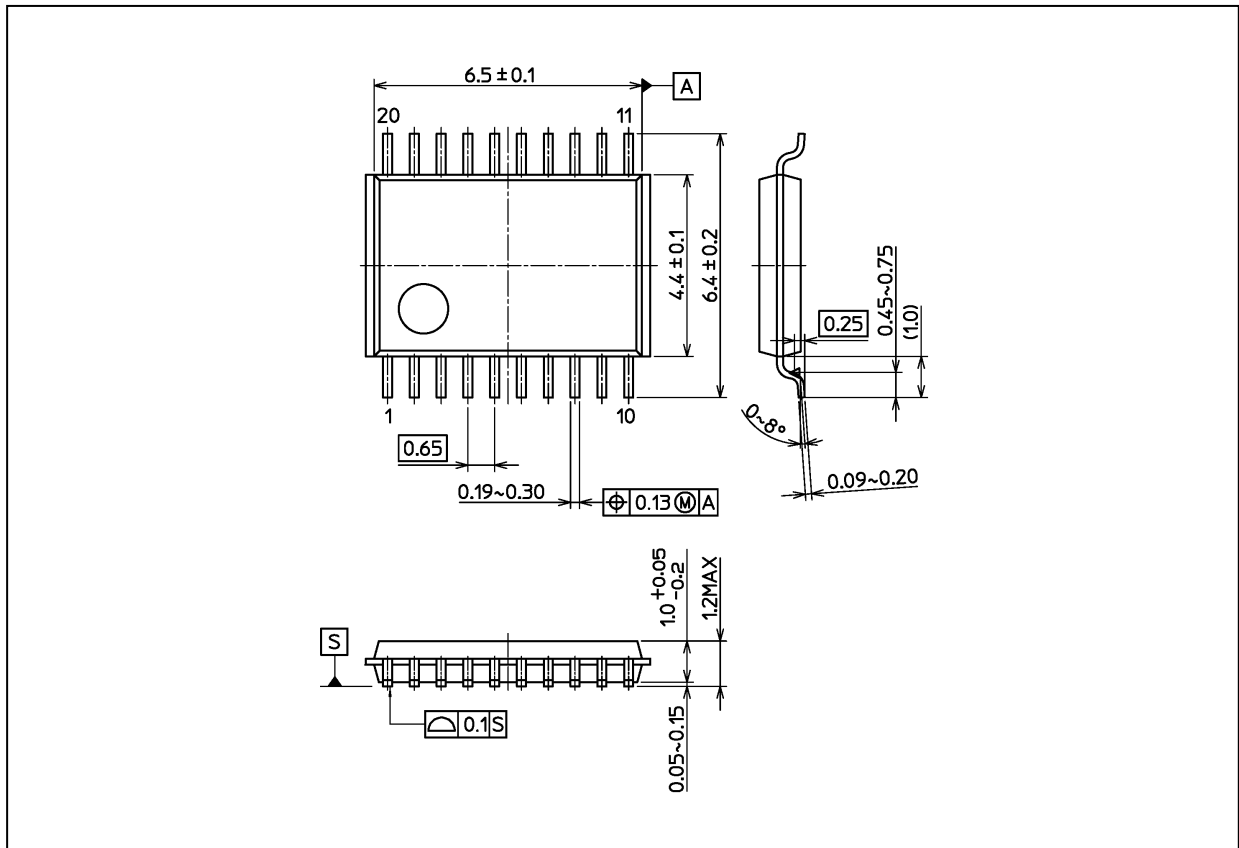
**13. Input Equivalent Circuit**





Package Dimensions

Unit: mm



Weight: 0.071 g (typ.)

Package Name(s)
Nickname: TSSOP20B

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