STB80N4F6AG

Automotive-grade N-Channel 40 V, 5.5 mΩ typ.,80 A STripFET™ F6 Power MOSFET in a D²PAK package

Datasheet - production data

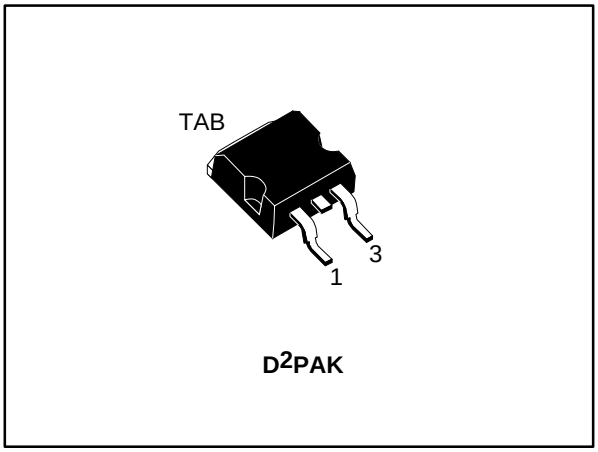
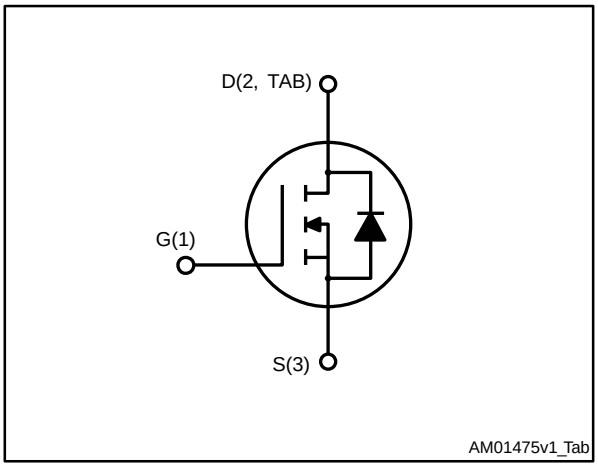


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB80N4F6AG	40 V	6 mΩ	80 A

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STB80N4F6AG	80N4F6	D²PAK	Tape and Reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	80	A
I_D	Drain current (continuous) at T_C= 100 °C	56	A
I_{DM}(1)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	W
I_{AV}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	40	A
E_{AS}	Single pulse avalanche energy(Starting T_J= 25 °C, = I_D =I_{AV}, V_{DD}= 25 V)	149	mJ
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Max. operating junction temperature	175	°C

Notes:

(1) Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	2.14	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-ambient max.	35	°C/W

Notes:

(1)When mounted on FR-4 board of inch2, 2 oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4: On/Off States

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS}= 0V)	V_{DS} = 40 V			1	µA
		V_{DS} = 40 V Tj = 125 °C			100	µA
I_{GSS}	Gate-body leakage current (V_{DS}= 0 V)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 40 A		5.5	6	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2150	-	pF
C_{oss}	Output capacitance		-	335	-	pF
C_{rss}	Reverse transfer capacitance		-	160	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 80 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	36	-	nC
Q_{gs}	Gate-source charge		-	11	-	nC
Q_{gd}	Gate-drain charge		-	9	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 40 A R_G = 4.7 Ω, V_{GS} = 10 V(see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	10.5	-	ns
t_r	Rise time		-	7.6	-	ns
$t_{d(off)}$	Turn-off-delay time		-	46.1	-	ns
t_f	Fall time		-	11.9	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source drain current				80	A
I_{SDM}(1)	Source-drain current (pulsed)				320	A
V_{SD}(2)	Forward on voltage	I_{SD}= 40 A, V_{GS}= 0 V			1.3	V
t_{rr}	Reverse recovery time	I_{SD}= 80 A, di/dt = 100 A/µs, V_{DD}= 32 V (See *Figure 17: "Unclamped inductive waveform"*)		41.1		ns
Q_{RR}	Reverse recovery charge			43.6		nC
I_{RRM}	Reverse recovery current			2.1		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

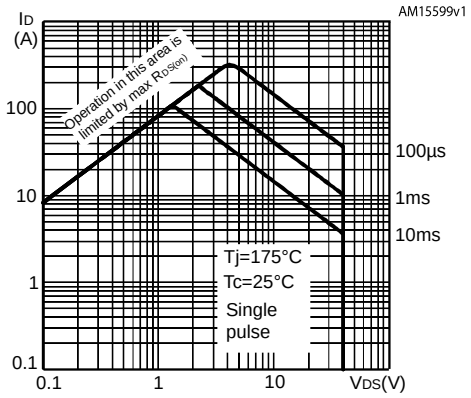


Figure 3: Thermal impedance

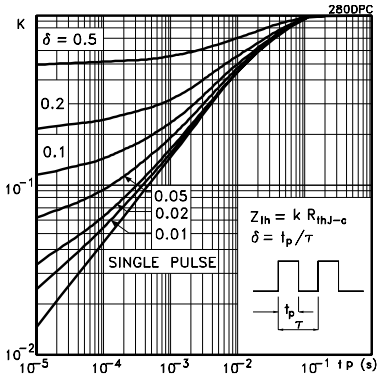


Figure 4: Output characteristics

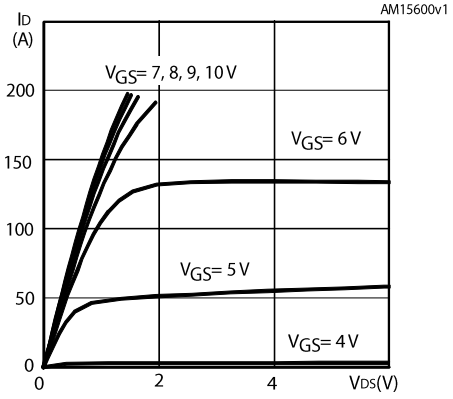


Figure 5: Transfer characteristics

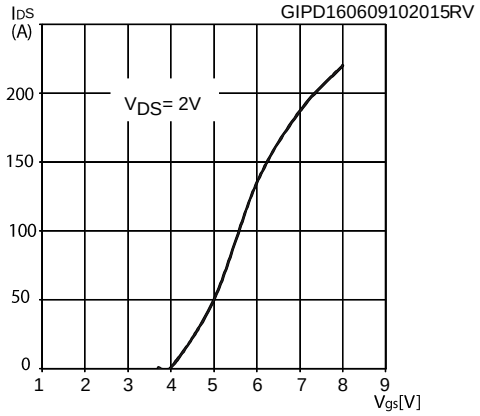


Figure 6: Normalized gate threshold voltage vs. temperature

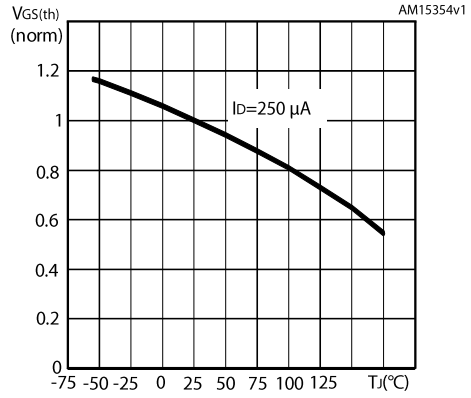


Figure 7: Normalized V(BR)DSS vs. temperature

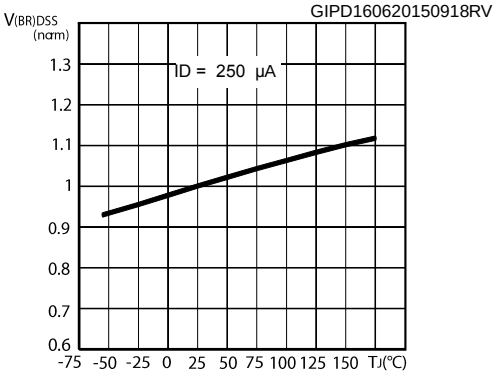


Figure 8: Static drain-source on-resistance

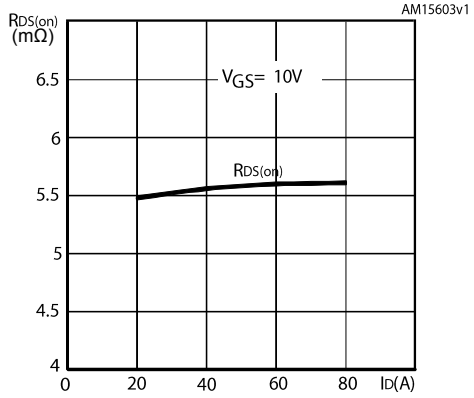


Figure 9: Normalized on-resistance vs. temperature

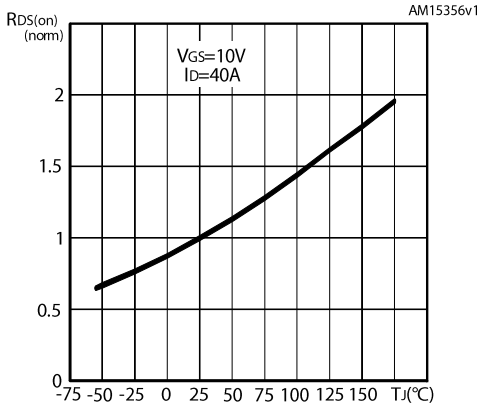


Figure 10: Gate charge vs. gate-source voltage

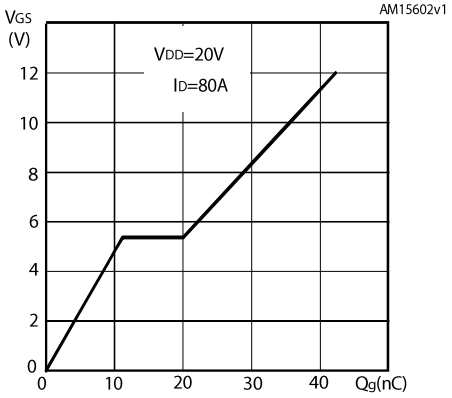


Figure 11: Capacitance variations

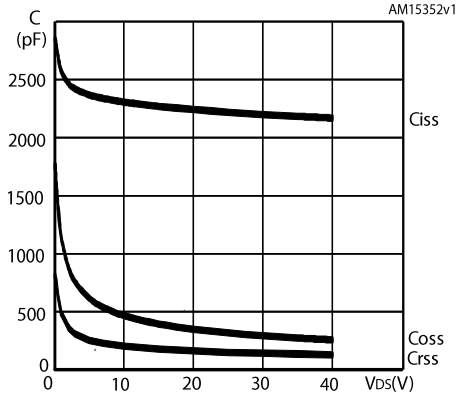
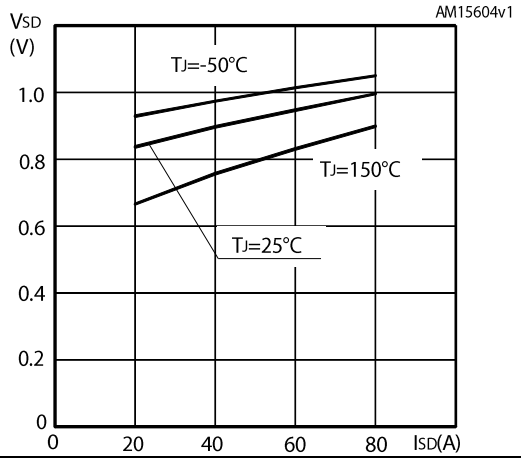


Figure 12: Source- drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

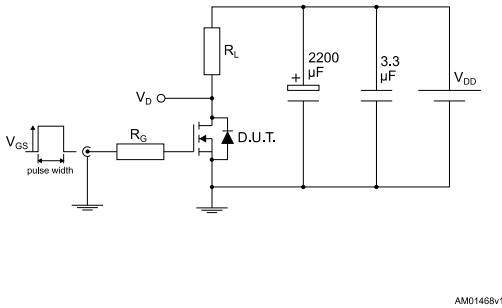


Figure 14: Test circuit for gate charge behavior

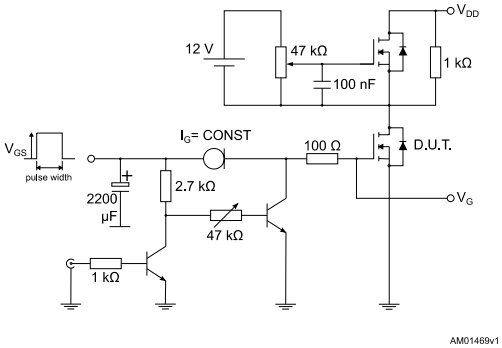


Figure 15: Test circuit for inductive load switching and diode recovery times

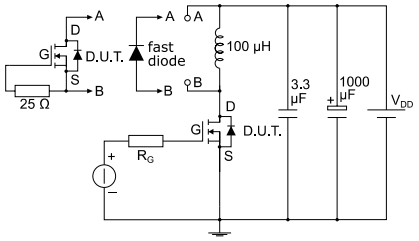


Figure 16: Unclamped inductive load test circuit

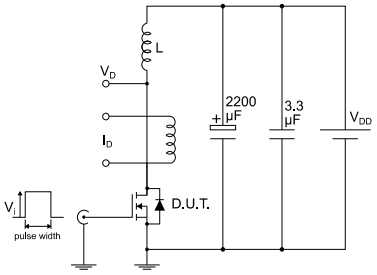


Figure 17: Unclamped inductive waveform

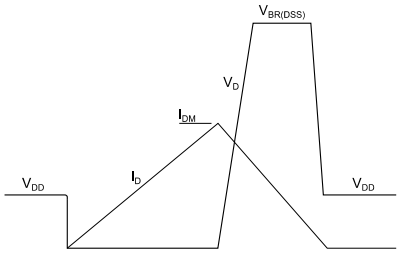
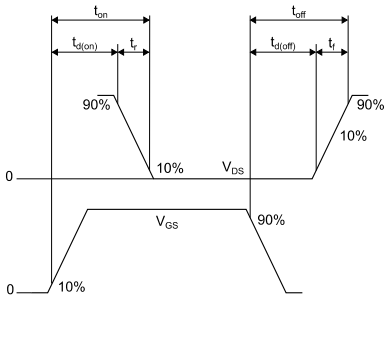


Figure 18: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 D²PAK package information

Figure 19: D²PAK (TO-263) type A package outline

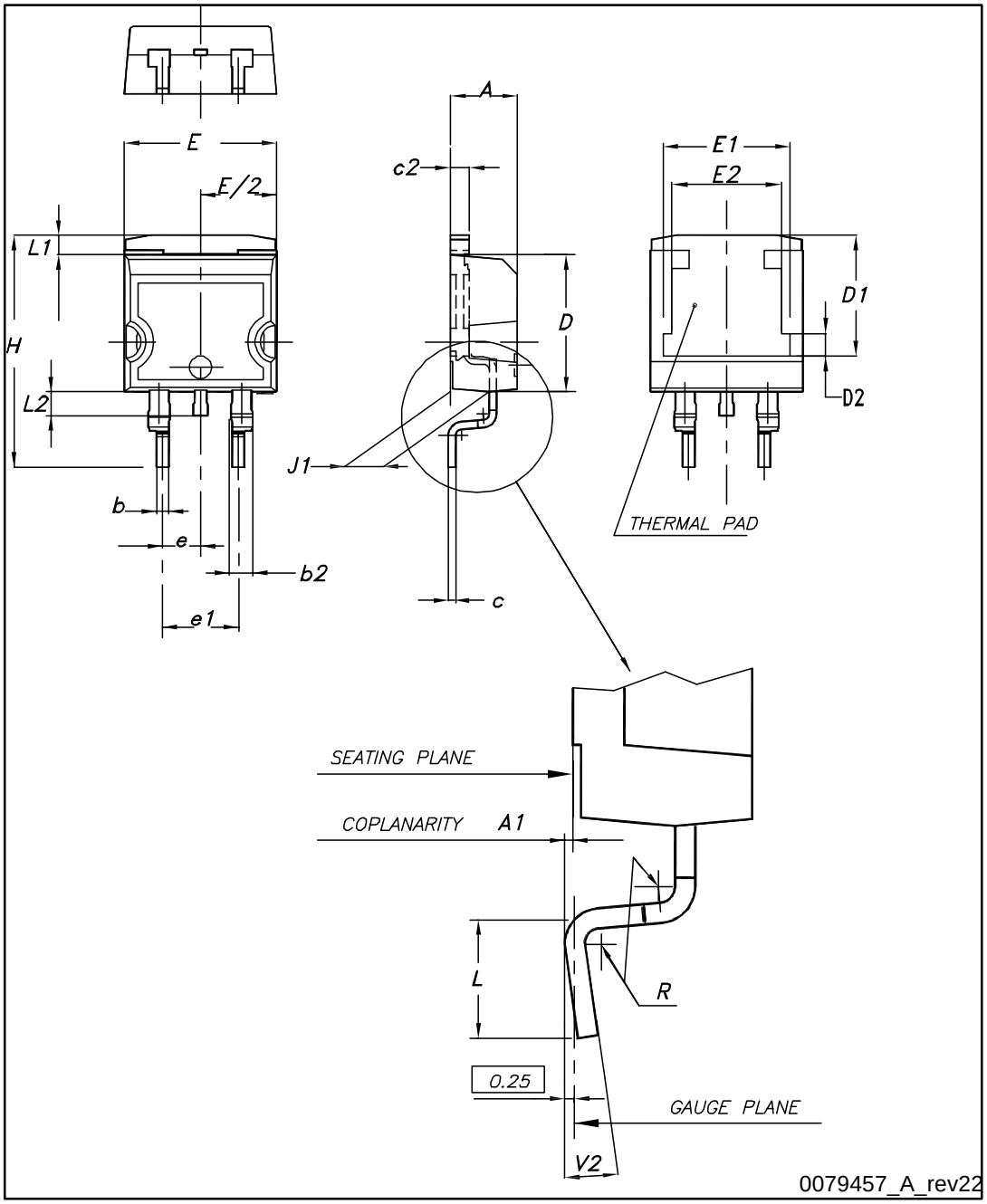
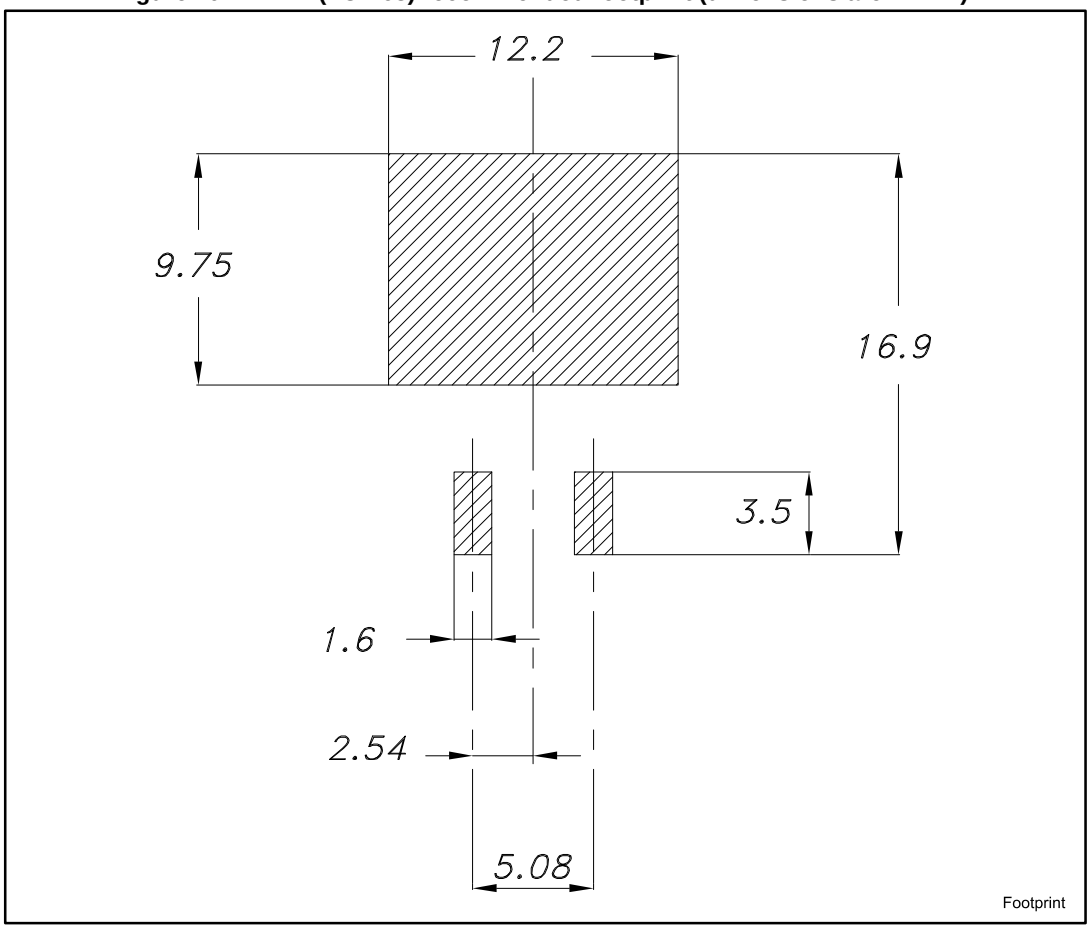


Table 8: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20: D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 D²PAK packing information

Figure 21: Tape outline

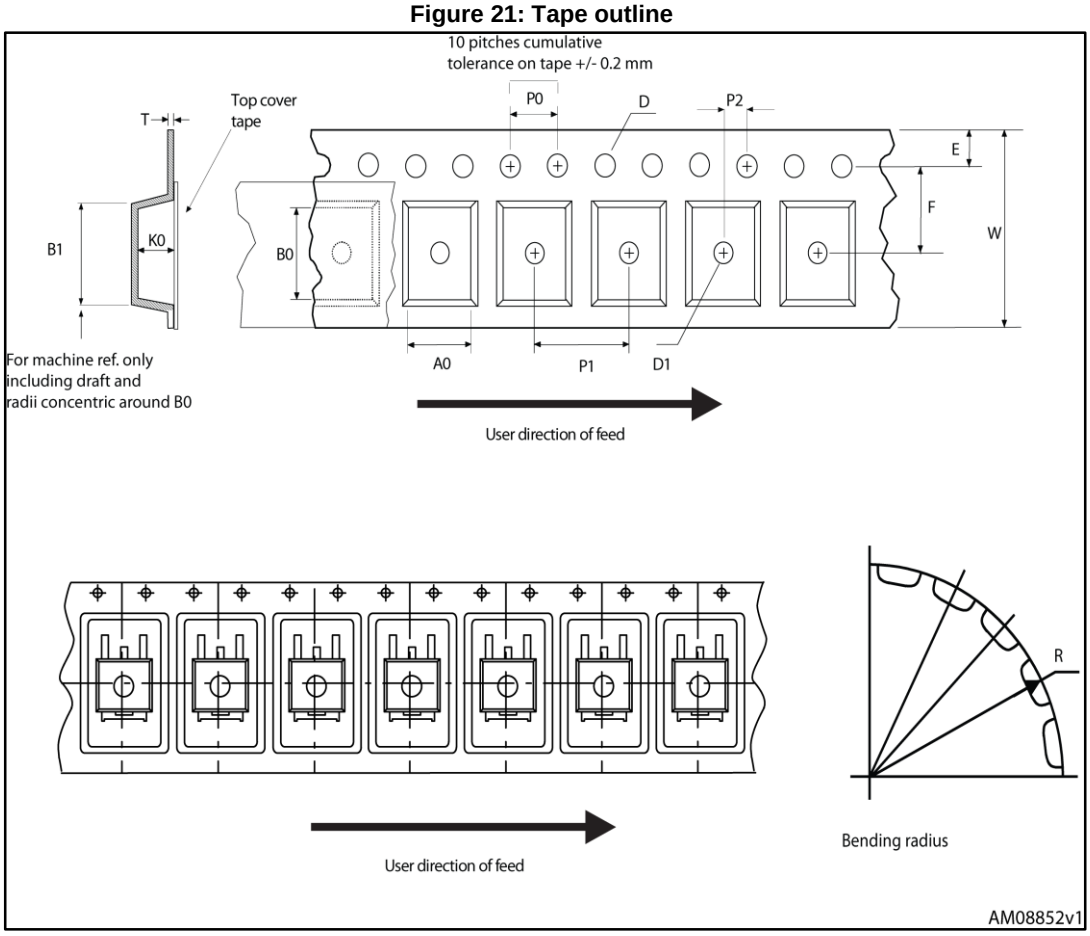


Figure 22: Reel outline

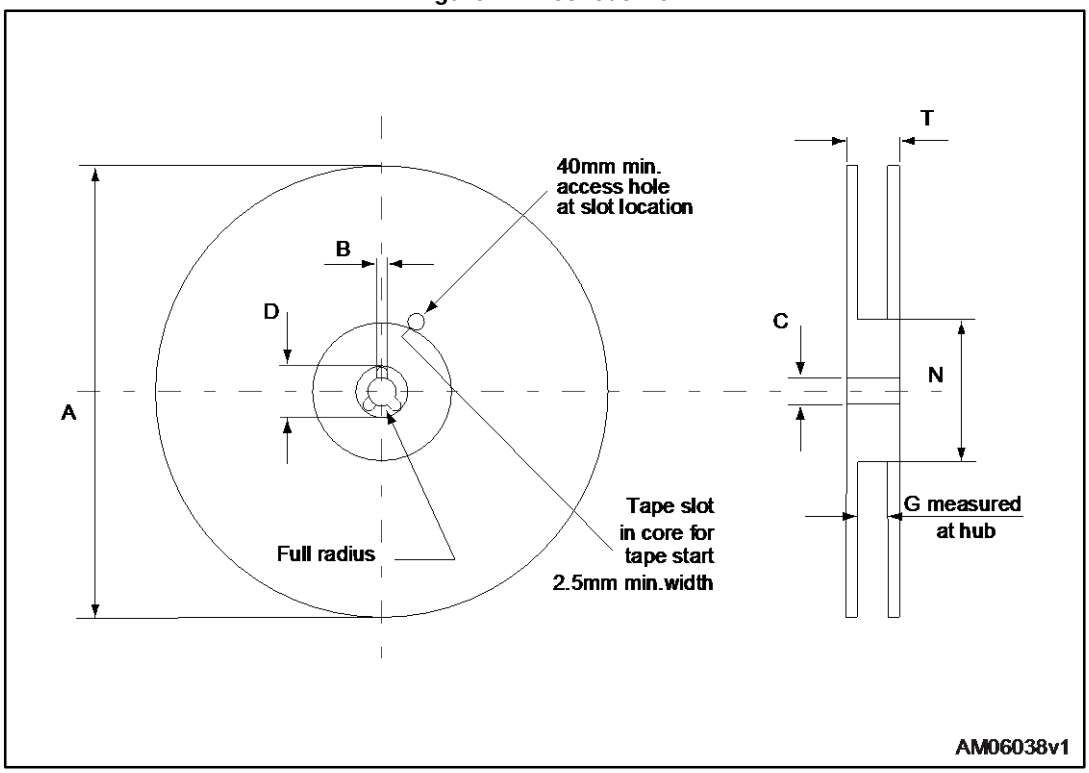


Table 9: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
16-Jun-2015	1	Initial release
18-Nov-2015	2	Document status promoted from preliminary to production data. Updated title and features in cover page.

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