RAA730502
Monolithic Programmable Analog IC

R02DS0010EJ0120
Rev.1.20
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Overview

The RAA730502 is a monolithic programmable analog IC with a range of on-chip circuits such as high-speed instrumentation amplifiers with comparators, D/A converters, and a temperature sensor, allowing the RAA730502 to be used as an analog front-end device for sensing current in motor control applications. The RAA730502 uses a Serial Peripheral Interface (SPI) to allow external devices to control each on-chip circuit, enabling a more compact package and a reduction in the number of control pins. The compact package used by the RAA730502—a 48-pin LQFP—in turns enables a more compact set design.

Features

- On-chip high-speed instrumentation amplifier with comparator × 4 ch
- On-chip D/A converter × 5 ch
- On-chip temperature sensor × 1 ch
- On-chip SPI × 1 ch
- Includes a low-current mode.
- Operating voltage range: 3.0 V ≤ V_{DD} ≤ 5.5 V
- Operating temperature range: -40ºC ≤ T_A ≤ 105ºC
- Package: 48-pin plastic LQFP (fine pitch) (7 × 7)

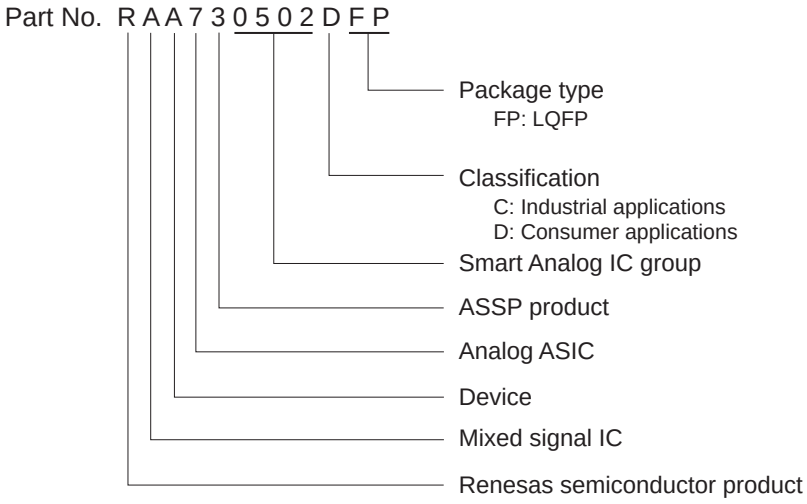
Applications

Home appliances

- Air purifiers
- Air conditioners
- Refrigerators
- Dishwashers
- Electric bicycles

Ordering Information

Pin count	Package	Part Number
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	RAA730502CFP, RAA730502DFP



How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, electronic circuits.

- To gain a general understanding of functions:
  →Read this manual in the order of the CONTENTS.
- To check the revised points :
  →The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what: " field.

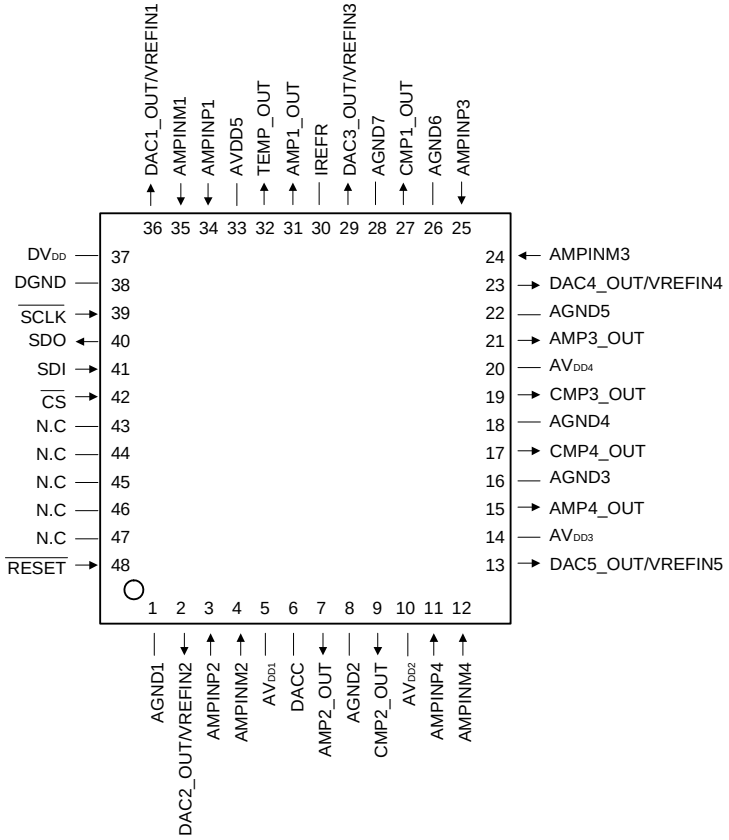
Conventions

Data significance	: Higher digits on the left and lower digits on the right
Active low representations	: $\overline{xxx}$ (overscore over pin and signal name)
Note	: Footnote for item marked with Note in the text
Caution	: Information requiring particular attention
Remark	: Supplementary information
Numerical representations	: Binary ...xxxx or xxxxB Decimal ...xxxx Hexadecimal ...xxxxH

Contents

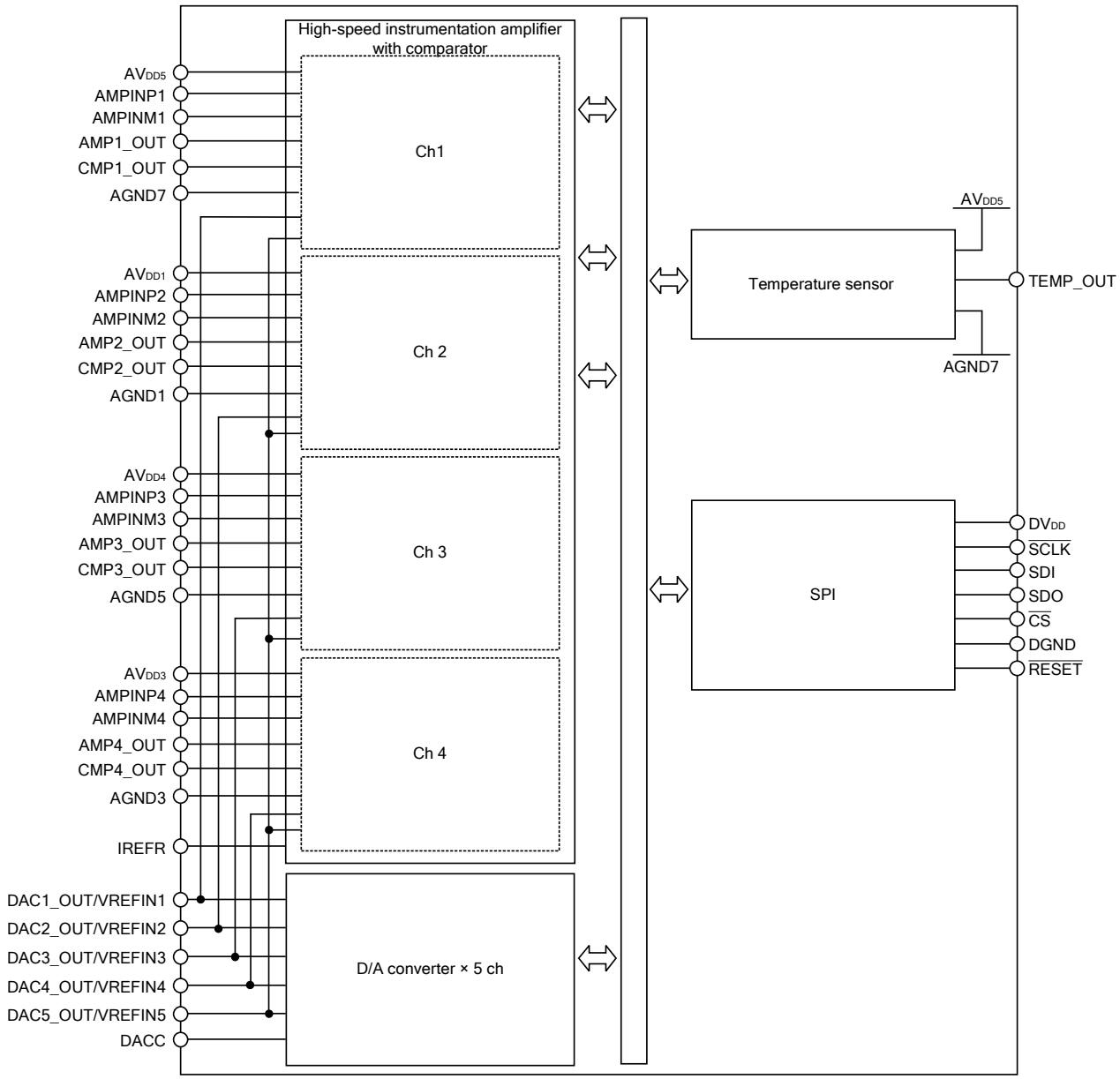
1. Pin Configuration

1.1 Pin Layout



Cautions
1. Make the potential of AGND1, AGND2, AGND3, AGND4, AGND5, AGND6, AGND7, and DGND the same.
2. Make the potential of AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, AV_{DD5}, and DV_{DD} the same.
3. Connect the DACC pin to AGND2 via a capacitor (100 nF: recommended).
4. Connect the IREFR pin to AGND7 via a resistor (56 kΩ: recommended).
5. Connect N.C to AGND1.

1.2 Block Diagram



1.3 Pin Functions

Table 1-1. Pin Functions (1/2)

Pin No.	Pin Name	I/O	Pin Functions
1	AGND1	–	GND pin for Ch2 high-speed instrumentation amplifier with comparator
2	DAC2_OUT/ VREFIN2	Input/ output	D/A converter Ch2 output pin/ Ch2 high-speed instrumentation amplifier reference voltage input pin
3	AMPINP2	Input	Ch2 high-speed instrumentation amplifier with comparator input pin (+)
4	AMPINM2	Input	Ch2 high-speed instrumentation amplifier with comparator input pin (-)
5	AV_{DD1}	–	Power supply pin for Ch2 high-speed instrumentation amplifier with comparator
6	DACC	Output	Pin for connecting stabilizing capacitor to D/A converter resistor arrays
7	AMP2_OUT	Output	High-speed instrumentation amplifier Ch2 output pin
8	AGND2	–	GND pin for D/A converter
9	CMP2_OUT	Output	Comparator Ch2 output pin
10	AV_{DD2}	–	Power supply pin for D/A converter
11	AMPINP4	Input	Ch4 high-speed instrumentation amplifier with comparator input pin (+)
12	AMPINM4	Input	Ch4 high-speed instrumentation amplifier with comparator input pin (-)
13	DAC5_OUT/ VREFIN5	Input/ output	D/A converter Ch5 output pin/comparator reference voltage input pin
14	AV_{DD3}	–	Power supply pin for Ch4 high-speed instrumentation amplifier with comparator
15	AMP4_OUT	Output	High-speed instrumentation amplifier Ch4 output pin
16	AGND3	–	GND pin for Ch4 high-speed instrumentation amplifier with comparator
17	CMP4_OUT	Output	Comparator Ch4 output pin
18	AGND4	–	GND pin for Ch2 high-speed instrumentation amplifier with comparator
19	CMP3_OUT	Output	Comparator Ch3 output pin
20	AV_{DD4}	–	Power supply pin for Ch3 high-speed instrumentation amplifier with comparator
21	AMP3_OUT	Output	High-speed instrumentation amplifier Ch3 output pin
22	AGND5	–	GND pin for Ch3 high-speed instrumentation amplifier with comparator
23	DAC4_OUT/ VREFIN4	Input/ output	D/A converter Ch4 output pin/ Ch4 high-speed instrumentation amplifier reference voltage input pin
24	AMPINM3	Input	Ch3 high-speed instrumentation amplifier with comparator input pin (-)
25	AMPINP3	Input	Ch3 high-speed instrumentation amplifier with comparator input pin (+)
26	AGND6	–	GND pin for temperature sensor
27	CMP1_OUT	Output	Comparator Ch1 output pin
28	AGND7	–	GND pin for temperature sensor
29	DAC3_OUT/ VREFIN3	Input/ output	D/A converter Ch3 output pin/ Ch3 high-speed instrumentation amplifier reference voltage input pin
30	IREFR	Output	Pin for connecting a resistor to stabilize the internal reference current
31	AMP1_OUT	Output	High-speed instrumentation amplifier Ch1 output pin
32	TEMP_OUT	Output	Temperature sensor output pin
33	AV_{DD5}	–	Power supply pin for Ch1 high-speed instrumentation amplifier with comparator
34	AMPINP1	Input	Ch1 high-speed instrumentation amplifier with comparator input pin (+)
35	AMPINM1	Input	Ch1 high-speed instrumentation amplifier with comparator input pin (-)

Table 1-1. Pin Functions (2/2)

Pin No.	Pin Name	I/O	Pin Functions
36	DAC1_OUT/ VREFIN1	Input/ output	D/A converter Ch1 output pin/ Ch1 high-speed instrumentation amplifier reference voltage input pin
37	DV_{DD}	–	Power supply pin for SPI
38	DGND	–	GND pin for SPI
39	$\overline{SCLK}$	Input	Serial clock input pin for SPI
40	SDO	Output	Serial data output pin for SPI
41	SDI	Input	Serial data input pin for SPI
42	$\overline{CS}$	Input	Chip select input pin for SPI
43	N.C[Note]	–	Non-connection
44	N.C[Note]	–	
45	N.C[Note]	–	
46	N.C[Note]	–	
47	N.C[Note]	–	
48	$\overline{RESET}$	Input	External reset input pin

Note Connect to AGND1.

1.4 Connection of Unused Pins

Table 1-2. Connection of Unused Pins

Pin Name	I/O	Recommended Connection of Unused Pins
DAC2_OUT/ VREFIN2	Input/ output	Leave open.
AMPINP2	Input	Directly connect to AGND1.
AMPINM2	Input	
AMP2_OUT	Output	Leave open.
CMP2_OUT	Output	
AMPINP4	Input	Directly connect to AGND3.
AMPINM4	Input	
DAC5_OUT/ VREFIN5	Input/ output	Leave open.
AMP4_OUT	Output	
CMP4_OUT	Output	
CMP3_OUT	Output	
AMP3_OUT	Output	
DAC4_OUT/ VREFIN4	Input/ output	
AMPINM3	Input	Directly connect to AGND5.
AMPINP3	Input	
CMP1_OUT	Output	Leave open.
DAC3_OUT/ VREFIN3	Output	
AMP1_OUT	Output	
TEMP_OUT	Output	
AMPINP1	Input	Directly connect to AGND7.
AMPINM1	Input	
DAC1_OUT/ VREFIN1	Input/ output	Leave open.
$\overline{SCLK}$	Input	
SDO	Output	
SDI	Input	
$\overline{CS}$	Input	
N.C	–	Directly connect to AGND1.
$\overline{RESET}$	Input	Connect to DV_{DD} directly or via a resistor.

1.5 Pin I/O Circuits

Figure 1-1. Pin I/O Circuit Type (1/5)

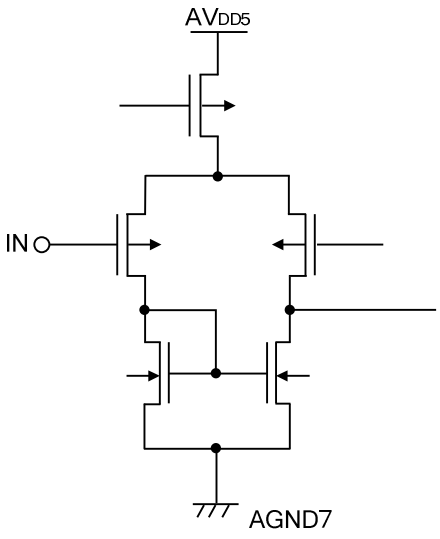
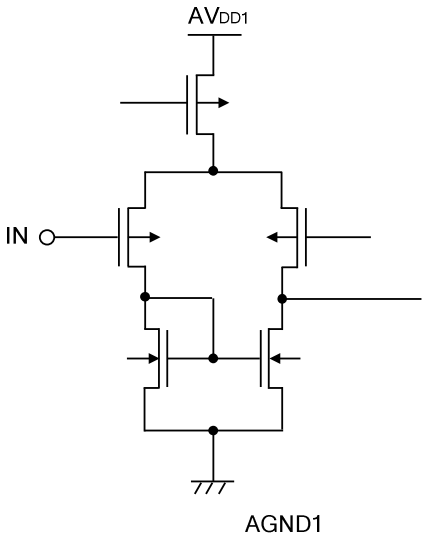
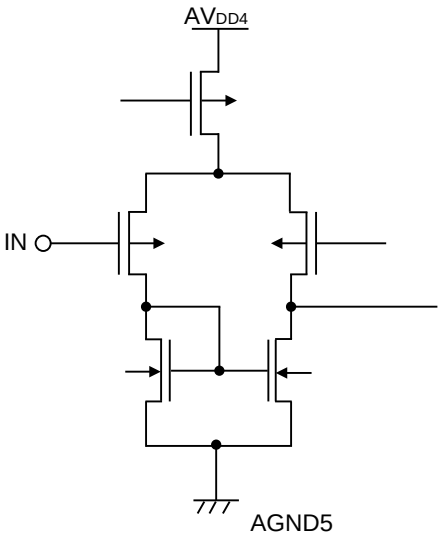
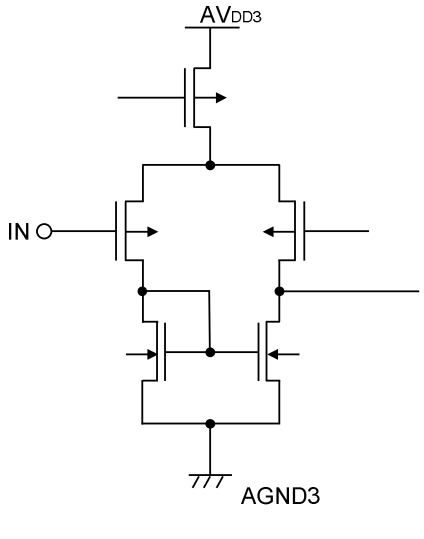
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
AMPINM1 AMPINP1		AMPINM2 AMPINP2	
AMPINM3 AMPINP3		AMPINM4 AMPINP4	

Figure 1-1. Pin I/O Circuit Type (2/5)

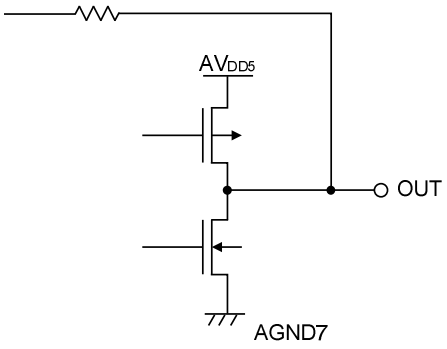
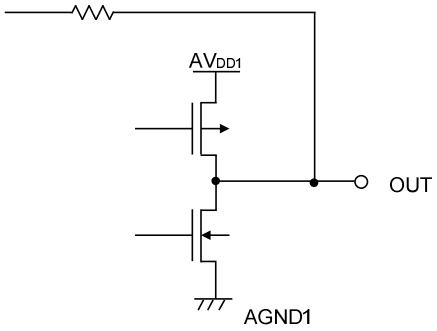
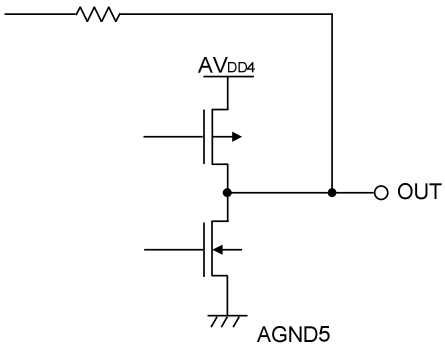
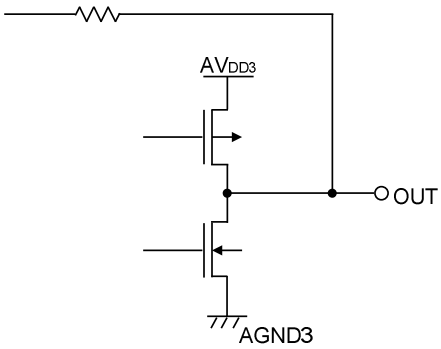
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
AMP1_OUT		AMP2_OUT	
AMP3_OUT		AMP4_OUT	

Figure 1-1. Pin I/O Circuit Type (3/5)

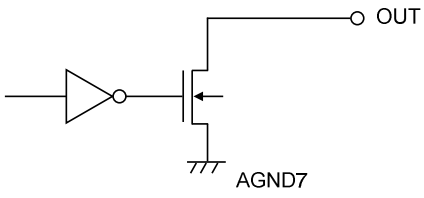
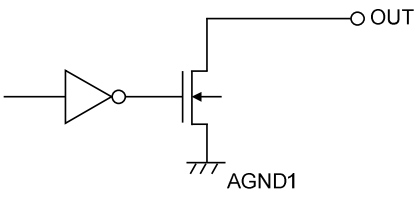
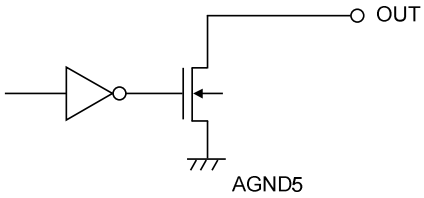
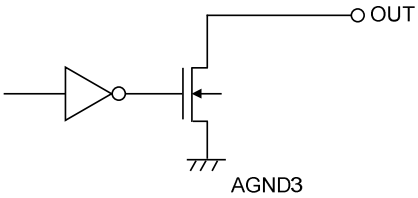
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
CMP1_OUT		CMP2_OUT	
CMP3_OUT		CMP4_OUT	

Figure 1-1. Pin I/O Circuit Type (4/5)

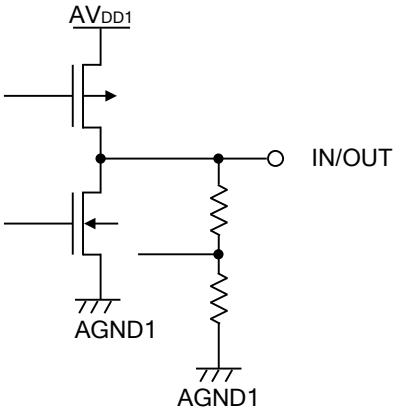
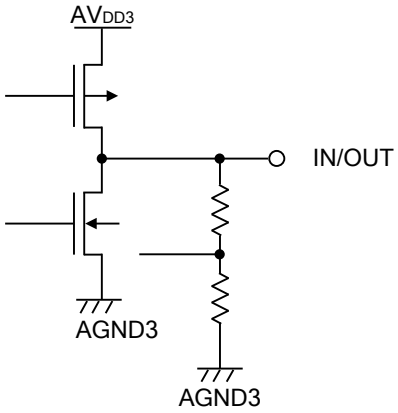
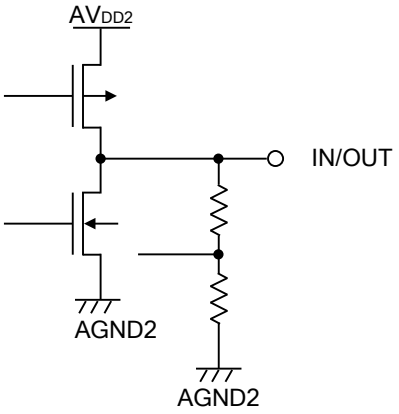
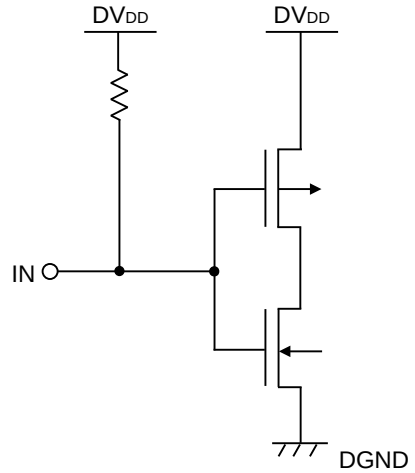
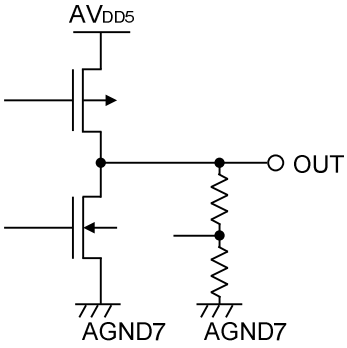
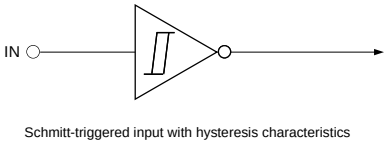
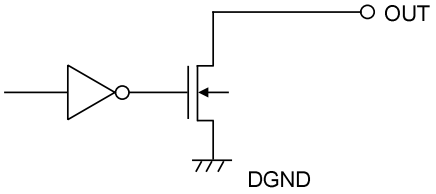
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
DAC1_OUT/ VREFIN1 DAC2_OUT/ VREFIN2		DAC3_OUT/ VREFIN3 DAC4_OUT/ VREFIN4	
DAC5_OUT/ VREFIN5		$\overline{SCLK}$ SDI $\overline{CS}$	

Figure 1-1. Pin I/O Circuit Type (5/5)

Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
TEMP_OUT		$\overline{\text{RESET}}$	 Schmitt-triggered input with hysteresis characteristics
SDO			

2. High-Speed Instrumentation Amplifiers with Comparators

The RAA730502 has four channels used as high-speed instrumentation amplifiers with comparators.

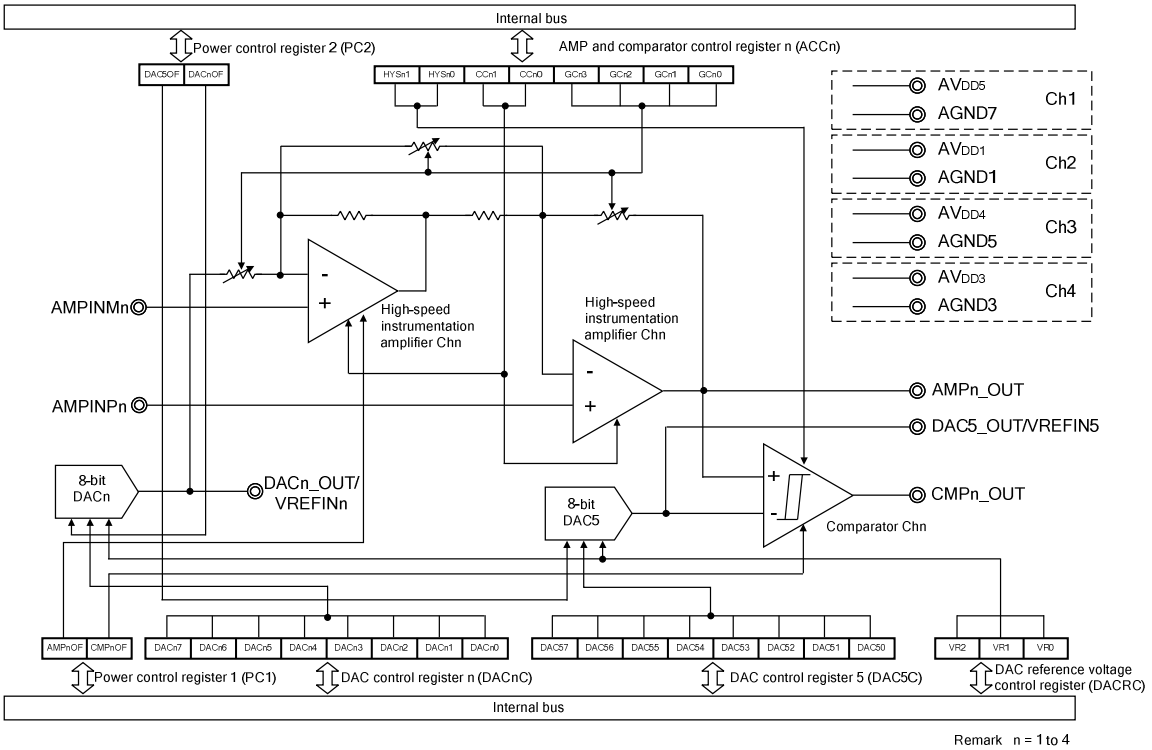
<R> 2.1 Overview of High-Speed Instrumentation Amplifiers with Comparators

Each high-speed instrumentation amplifier with comparator includes a high-speed instrumentation amplifier block and a comparator block.

- High-speed instrumentation amplifier block
  - The gain can be specified between 10 dB and 34 dB in 13 steps.
  - Four operating modes are available.
  - The reference voltage can be adjusted by using D/A converter Ch1 to Ch4.
  - Includes a power-off function.
- Comparator block
  - The signal output from a high-speed instrumentation amplifier with comparator can be input to the positive (+) pin of the comparator, compared with the D/A converter output, and then output.
  - The reference voltage can be adjusted by using D/A converter Ch5.
  - Includes a power-off function.

And also, the DACn_OUT (n = 1 to 5) output signal can be used as the reference voltage for high-speed instrumentation amplifier with comparator. If D/A converters are powered off, the external reference voltage is to be input to DACn_OUT/VREFINn (n = 1 to 5) pin. For details about use of D/A converter, see **3. D/A Converter**.

2.2 Block Diagram



Caution When using the comparators, connect the CMPn_OUT pin to a pull-up resistor (2.2 kΩ recommended).

Remark n = 1 to 4

2.3 Registers Controlling the High-Speed Instrumentation Amplifiers with Comparators

The high-speed instrumentation amplifiers with comparators are controlled by the following 2 registers:

- AMP and comparator control registers 1, 2, 3, 4 (ACC1, ACC2, ACC3, ACC4)
- Power control register 1 (PC1)

(1) AMP and comparator control registers 1, 2, 3, 4 (ACC1, ACC2, ACC3, ACC4)

This register is used to specify the operating mode and gain of the high-speed instrumentation amplifiers with comparators, and the hysteresis width of the comparators.
Reset signal input clears this register to 00H.

Address: 00H (n = 1), 01H (n = 2), 02H (n = 3), 03H (n = 4) After reset: 00H R/W

	7	6	5	4	3	2	1	0
ACCn	HYSn1	HYSn0	CCn1	CCn0	GCn3	GCn2	GCn1	GCn0

HYSn1	HYSn0	Hysteresis width (Typ.)
0	0	200 mV
0	1	100 mV
1	0	50 mV
1	1	No hysteresis

CCn1	CCn0	Operating mode of high-speed instrumentation amplifiers with comparators
0	0	High-speed mode
0	1	Mid-speed mode 2
1	0	Mid-speed mode 1
1	1	Low-speed mode

GCn3	GCn2	GCn1	GCn0	Gain of high-speed instrumentation amplifiers with comparators (Typ.)
0	0	0	0	10 dB
0	0	0	1	12 dB
0	0	1	0	14 dB
0	0	1	1	16 dB
0	1	0	0	18 dB
0	1	0	1	20 dB
0	1	1	0	22 dB
0	1	1	1	24 dB
1	0	0	0	26 dB
1	0	0	1	28 dB
1	0	1	0	30 dB
1	0	1	1	32 dB
1	1	0	0	34 dB
Other than above				Setting prohibited

Remark n = 1 to 4

(2) Power control register 1 (PC1)

This register is used to enable or disable operation of the high-speed instrumentation amplifiers with comparators.
Use this register to stop unused functions to reduce power consumption and noise.
When using one of Ch1 to Ch4 high-speed instrumentation amplifiers with comparators, be sure to set the control bit that corresponds to the comparators Ch1 to Ch4 and high-speed instrumentation amplifiers Ch1 to Ch4 to 1.
Reset signal input clears this register to 00H.

Address: 0AH After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	CMP4OF	CMP3OF	CMP2OF	CMP1OF	AMP4OF	AMP3OF	AMP2OF	AMP1OF

CMP4OF	Operation of comparator Ch4
0	Stop operation of comparator Ch4.
1	Enable operation of comparator Ch4.

CMP3OF	Operation of comparator Ch3
0	Stop operation of comparator Ch3.
1	Enable operation of comparator Ch3.

CMP2OF	Operation of comparator Ch2
0	Stop operation of comparator Ch2.
1	Enable operation of comparator Ch2.

CMP1OF	Operation of comparator Ch1
0	Stop operation of comparator Ch1.
1	Enable operation of comparator Ch1.

AMP4OF	Operation of high-speed instrumentation amplifier Ch4
0	Stop operation of high-speed instrumentation amplifier Ch4.
1	Enable operation of high-speed instrumentation amplifier Ch4.

AMP3OF	Operation of high-speed instrumentation amplifier Ch3
0	Stop operation of high-speed instrumentation amplifier Ch3.
1	Enable operation of high-speed instrumentation amplifier Ch3.

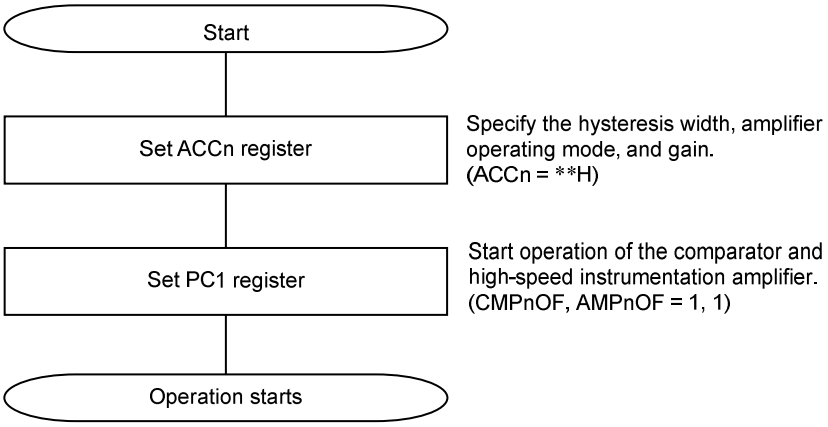
AMP2OF	Operation of high-speed instrumentation amplifier Ch2
0	Stop operation of high-speed instrumentation amplifier Ch2.
1	Enable operation of high-speed instrumentation amplifier Ch2.

AMP1OF	Operation of high-speed instrumentation amplifier Ch1
0	Stop operation of high-speed instrumentation amplifier Ch1.
1	Enable operation of high-speed instrumentation amplifier Ch1.

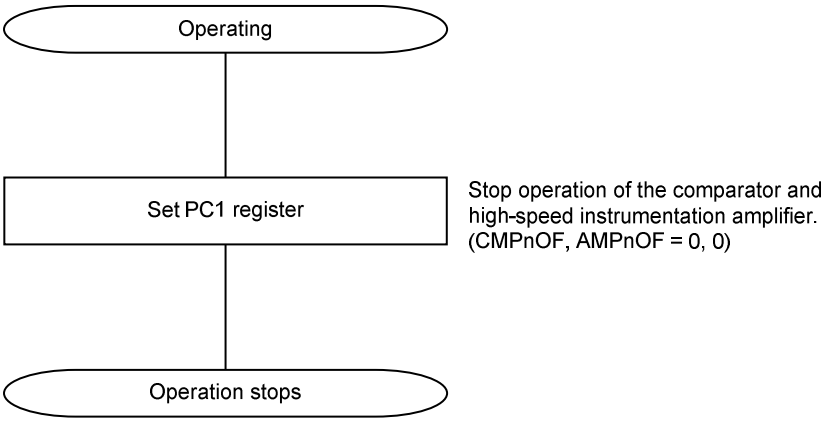
2.4 Procedure for Operating the High-Speed Instrumentation Amplifiers with Comparators

Follow the procedures below to start and stop the high-speed instrumentation amplifiers with comparators.

Example of procedure for starting the high-speed instrumentation amplifiers with comparators



Example of procedure for stopping the high-speed instrumentation amplifiers with comparators



Remark *: don´t care
n = 1 to 4

3. D/A Converters

The RAA730502 has five on-chip D/A converter channels.

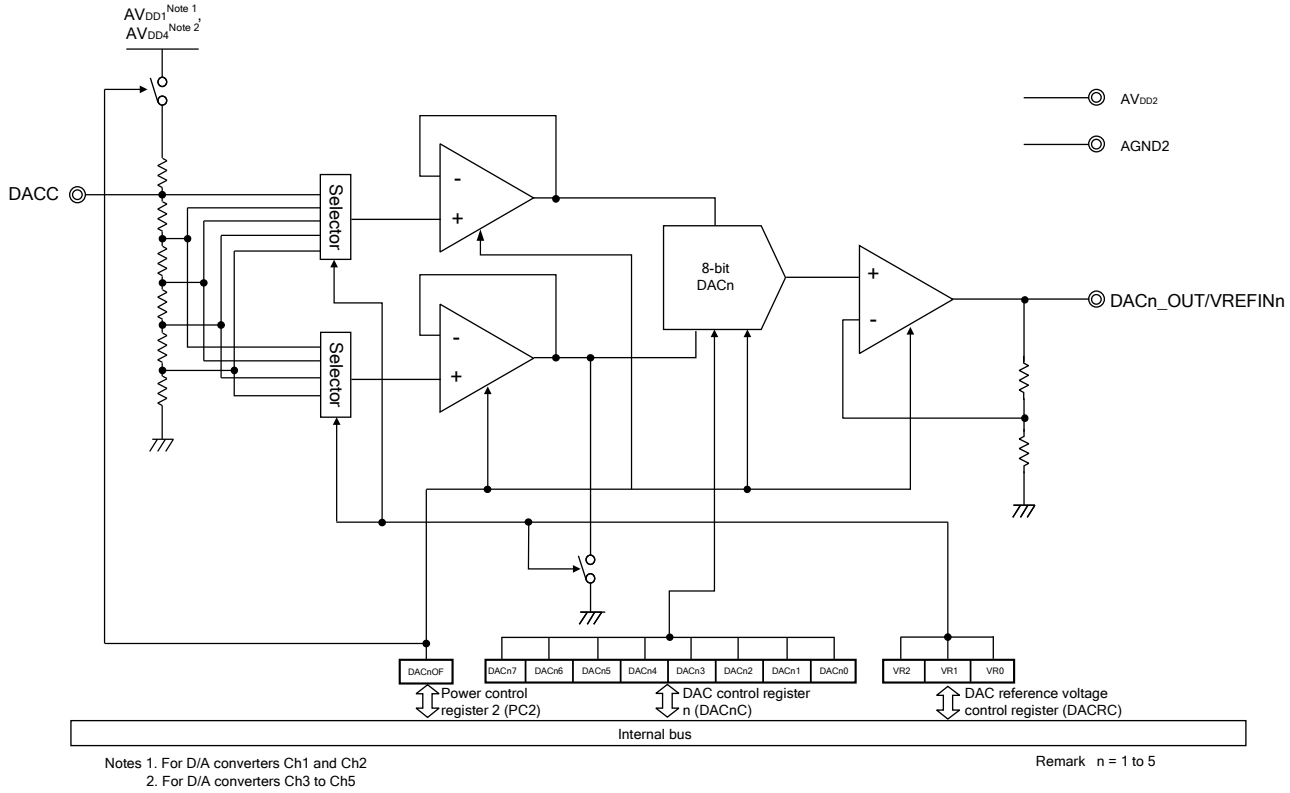
<R> 3.1 Overview of D/A Converter Features

The D/A converters are 8-bit resolution converters that convert digital input signals into analog signals.
The D/A converters have the following features:

- 8-bit resolution (× 5 ch: Ch1 to Ch5)
- R-2R ladder method
- Analog output voltage: Output voltage can be calculated with the equation shown below.
  Output voltage = {(Reference voltage upper limit – Reference voltage lower limit) × m/256}
  + Reference voltage lower limit (m = 0 to 255: Value set to DACnC register)
- Controls the reference voltage for the high-speed instrumentation amplifiers with comparators
- Includes a power-off function.

Remark n = 1 to 5

3.2 Block Diagram



3.3 Registers Controlling the D/A Converters

The D/A converters are controlled by the following 3 kinds of registers:

- DAC control registers 1, 2, 3, 4, 5 (DAC1C, DAC2C, DAC3C, DAC4C, DAC5C)
- DAC reference voltage control register (DACRC)
- Power control register 2 (PC2)

(1) DAC control registers 1, 2, 3, 4, 5 (DAC1C, DAC2C, DAC3C, DAC4C, DAC5C)

This register is used to specify the analog voltage to be output to the DACn_OUT pin.
The DACn_OUT output signal can be used as the reference voltage for the high-speed instrumentation amplifiers with comparators.
Reset signal input sets this register to 80H.

Address: 04H (n = 1), 05H (n = 2), 06H (n = 3), 07H (n = 4), 08H (n = 5) After reset: 80H R/W

	7	6	5	4	3	2	1	0
DACnC	DACn7	DACn6	DACn5	DACn4	DACn3	DACn2	DACn1	DACn0

Remark 1. n = 1 to 5

2. To calculate the output voltage, see **3. 1 Overview of D/A converter features**.

<R> **(2) DAC reference voltage control register (DACRC)**

This register is used to specify the upper (VRT) and lower (VRB) limits of the reference voltage for D/A converters Ch1 to Ch5.
Reset signal input clears this register to 00H.

Address: 09H After reset: 00H R/W

	7	6	5	4	3	2	1	0
DACRC	0	0	0	0	0	VR2	VR1	VR0

VR2	VR1	VR0	Reference voltage upper limit (Typ.)		Reference voltage lower limit (Typ.)	
			D/A converters Ch1, Ch2	D/A converters Ch3 to Ch5	D/A converters Ch1, Ch2	D/A converters Ch3 to Ch5
0	0	0	AV_{DD1}	AV_{DD4}	AGND1	AGND5
0	0	1	$AV_{DD1} \times 1/5$	$AV_{DD4} \times 1/5$	AGND1	AGND5
0	1	0	$AV_{DD1} \times 2/5$	$AV_{DD4} \times 2/5$	$AV_{DD1} \times 1/5$	$AV_{DD4} \times 1/5$
0	1	1	$AV_{DD1} \times 3/5$	$AV_{DD4} \times 3/5$	$AV_{DD1} \times 2/5$	$AV_{DD4} \times 2/5$
1	0	0	$AV_{DD1} \times 4/5$	$AV_{DD4} \times 4/5$	$AV_{DD1} \times 3/5$	$AV_{DD4} \times 3/5$
1	0	1	AV_{DD1}	AV_{DD4}	$AV_{DD1} \times 4/5$	$AV_{DD4} \times 4/5$
1	1	0	$AV_{DD1} \times 4/5$	$AV_{DD4} \times 4/5$	$AV_{DD1} \times 1/5$	$AV_{DD4} \times 1/5$
1	1	1	Setting prohibited			

Remark Bits 7 to 3 are fixed to 0. (Prohibited to be set to 1.)

(3) Power control register 2 (PC2)

This register is used to enable or disable operation of the D/A converters and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using one of D/A converter channels Ch1 to Ch5, be sure to set the control bit that corresponds to the channel (bits 4 to 0) to 1.
Reset signal input clears this register to 00H.

Address: 0BH After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	TEMPOF	DAC5OF	DAC4OF	DAC3OF	DAC2OF	DAC1OF

DAC5OF	Operation of D/A converter Ch5
0	Stop operation of D/A converter Ch5.
1	Enable operation of D/A converter Ch5.

DAC4OF	Operation of D/A converter Ch4
0	Stop operation of D/A converter Ch4.
1	Enable operation of D/A converter Ch4.

DAC3OF	Operation of D/A converter Ch3
0	Stop operation of D/A converter Ch3.
1	Enable operation of D/A converter Ch3.

DAC2OF	Operation of D/A converter Ch2
0	Stop operation of D/A converter Ch2.
1	Enable operation of D/A converter Ch2.

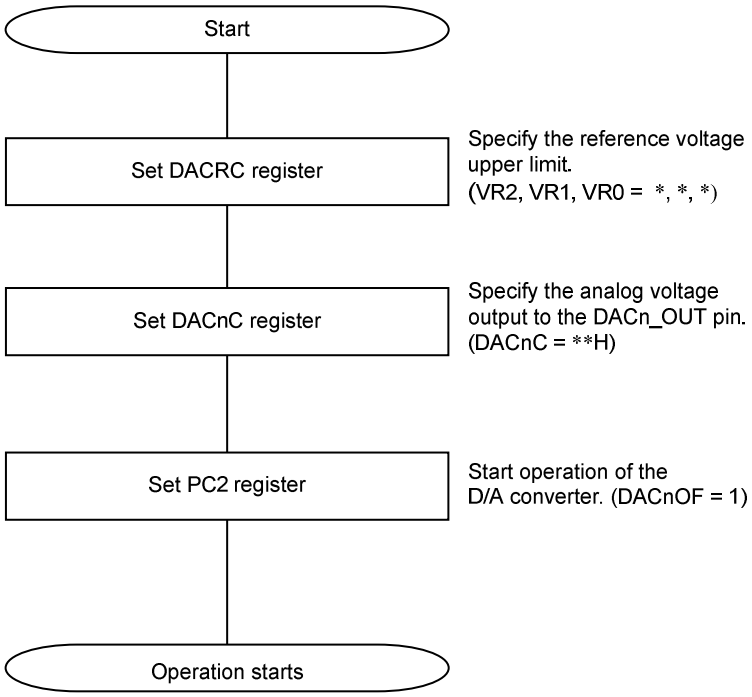
DAC1OF	Operation of D/A converter Ch1
0	Stop operation of D/A converter Ch1.
1	Enable operation of D/A converter Ch1.

Remark Bits 7 and 6 are fixed to 0. (Prohibited to be set to 1.)

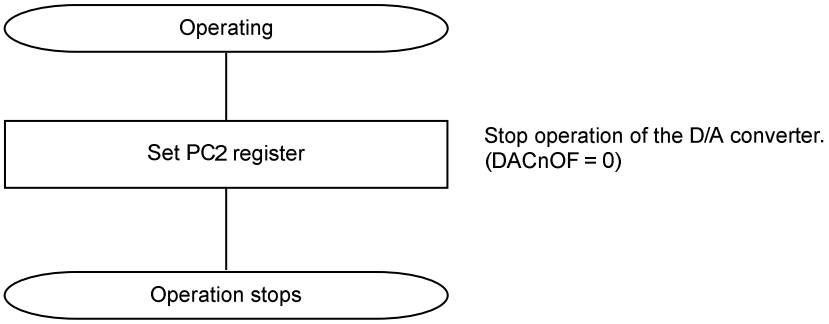
3.4 Procedure for Operating the D/A Converters

Follow the procedures below to start and stop the D/A converters.

Example of procedure for starting the D/A converters



Example of procedure for stopping the D/A converters



Remark *: don´t care
n = 1 to 5

3.5 Notes on Using the D/A Converters

Observe the following points when using the D/A converters:

(1) Only a very small current can flow from the DACn_OUT pin because the output impedance of the D/A converters is high. If the load input impedance is low, insert a follower amplifier between the load and the DACn_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible (because of the high output impedance). If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.

(2) If inputting an external reference power supply to the VREFINn pin, be sure to set the DACnOF bit to 0.

Remark n = 1 to 5

4. Temperature Sensor

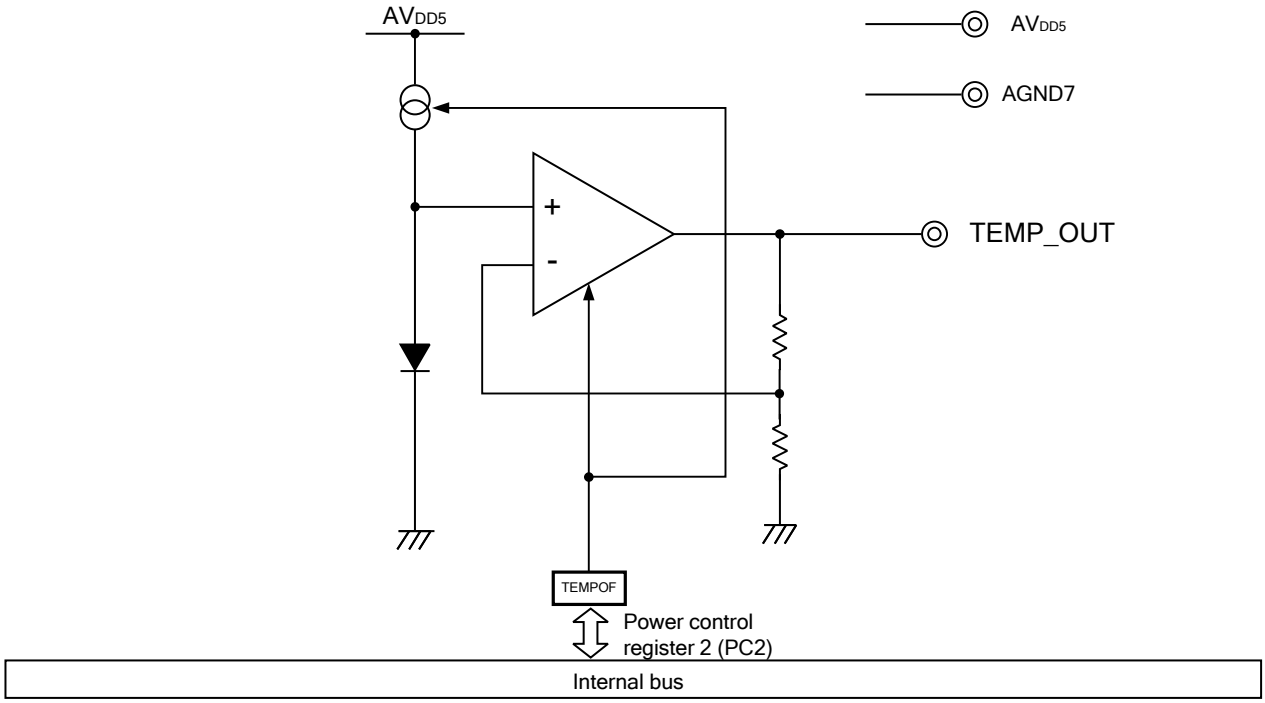
The RAA730502 has one on-chip temperature sensor channel.

4.1 Overview of Temperature Sensor Features

The temperature sensor have the following features:

- Output voltage temperature coefficient: -5mV/°C (Typ.)
- Includes a power-off function.

4.2 Block Diagram



4.3 Registers Controlling the Temperature Sensor

The temperature sensor is controlled by the following register:

- Power control register 2 (PC2)

(1) Power control register 2 (PC2)

This register is used to enable or disable operation of the temperature sensor and D/A converter. Use this register to stop unused functions to reduce power consumption and noise.
When selecting the signal to be input to the temperature sensor, be sure to set bit 5 to 1.
Reset signal input clears this register to 00H.

Address: 0BH After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	TEMPOF	DAC5OF	DAC4OF	DAC3OF	DAC2OF	DAC1OF

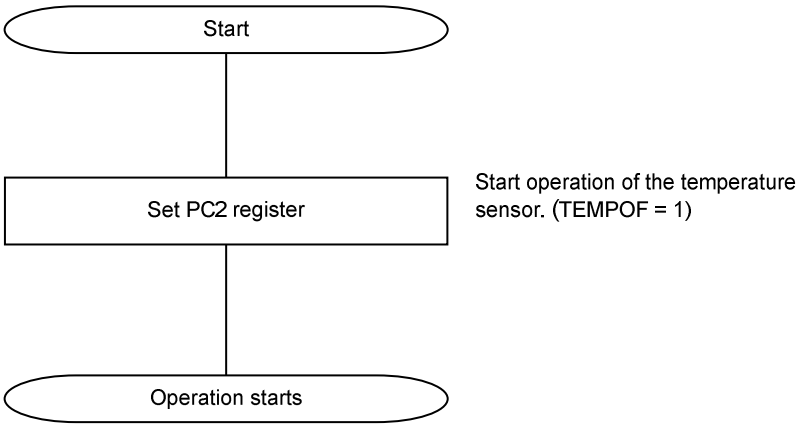
TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Remark Bits 7 and 6 are fixed to 0. (Prohibited to be set to 1.)

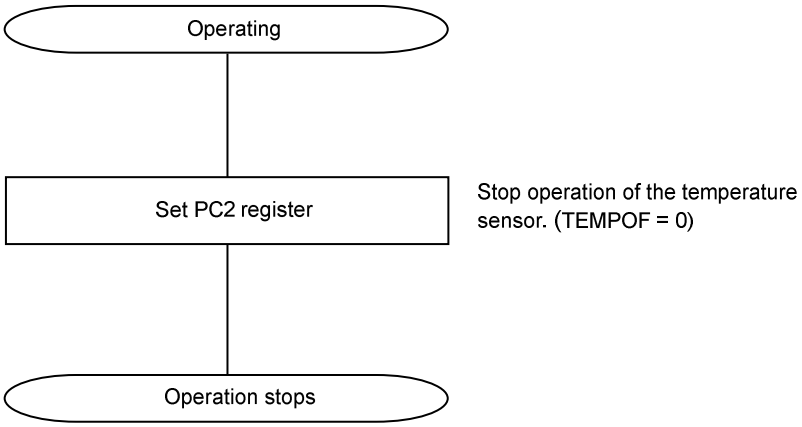
4.4 Procedure for Operating the Temperature Sensor

Follow the procedures below to start and stop the temperature sensor.

Example of procedure for starting the temperature sensor



Example of procedure for stopping the temperature sensor



5. SPI

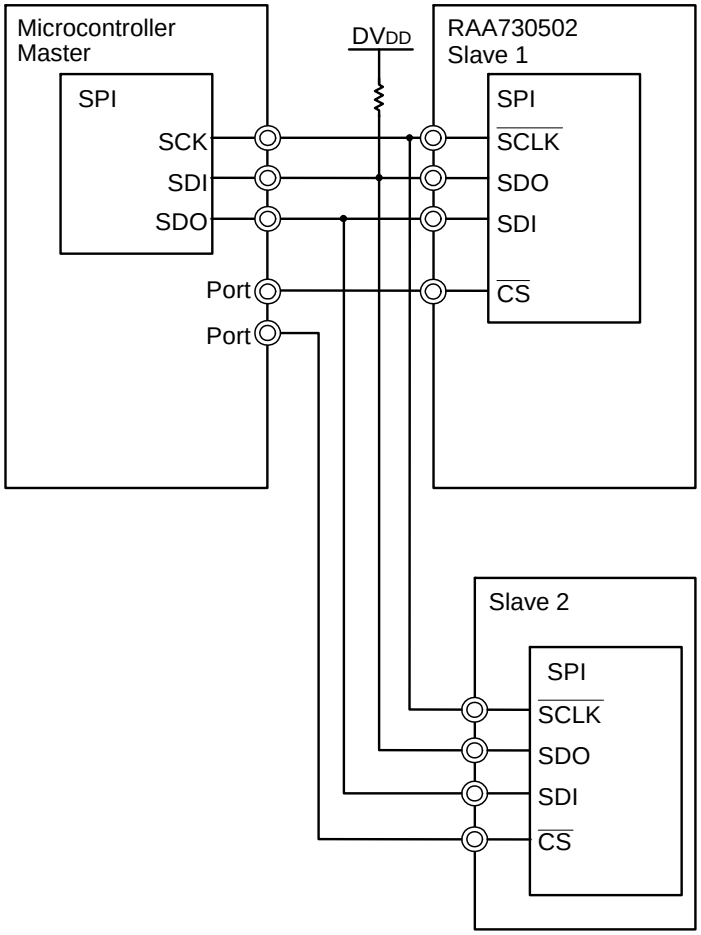
5.1 SPI Features

The SPI is used to allow control from external devices by using clocked communication via four lines: a serial clock line ($\overline{SCLK}$), two serial data lines (SDI and SDO), and a chip select input line ($\overline{CS}$).

Data transmission/reception:

- 16-bit data unit
- MSB first

Figure 5-1. SPI Configuration Example



<R> **Caution After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{RESET}$ pin before starting SPI communication. For details, see 6 Reset.**

5.2 SPI Communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when $\overline{CS}$ is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting after the 16th rising edge of $\overline{SCLK}$ has been detected following the fall of $\overline{CS}$. The operation specified by the data is then executed. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting in synchronization with the 9th and later falling edges of $\overline{SCLK}$ following the fall of $\overline{CS}$.

Figure 5-2. SPI Communication Timing

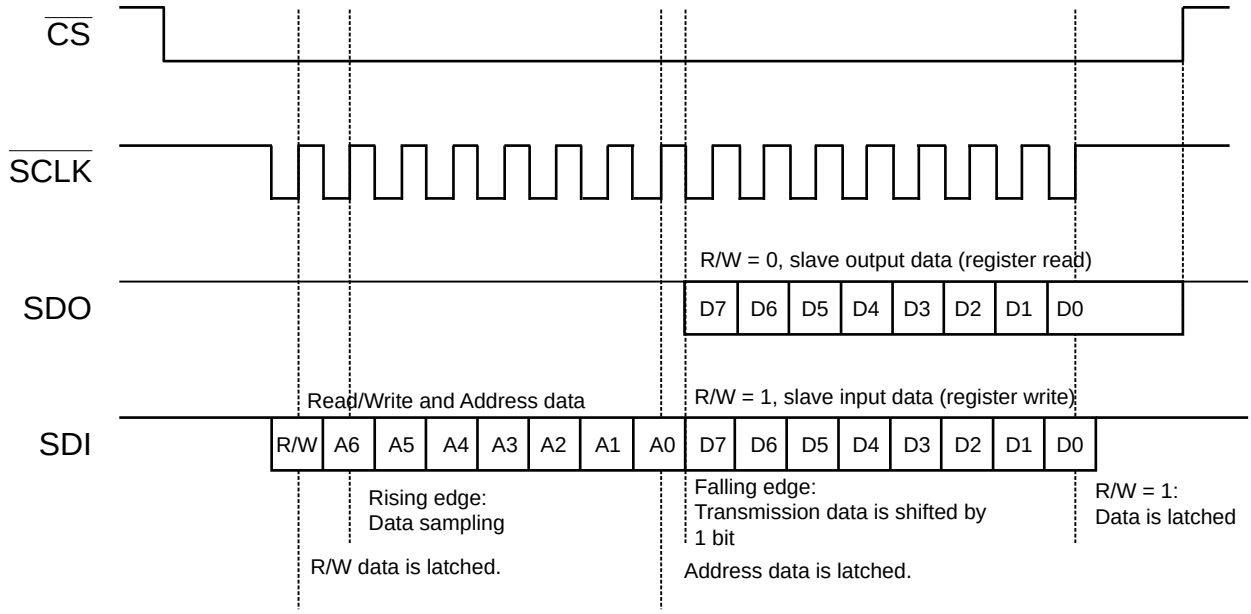


Table 5-1. SPI Control Registers

Address	SPI Control Register	R/W	After Reset
00H	AMP and comparator control register 1 (ACC1)	R/W	00H
01H	AMP and comparator control register 2 (ACC2)	R/W	00H
02H	AMP and comparator control register 3 (ACC3)	R/W	00H
03H	AMP and comparator control register 4 (ACC4)	R/W	00H
04H	DAC control register 1 (DAC1C)	R/W	80H
05H	DAC control register 2 (DAC2C)	R/W	80H
06H	DAC control register 3 (DAC3C)	R/W	80H
07H	DAC control register 4 (DAC4C)	R/W	80H
08H	DAC control register 5 (DAC5C)	R/W	80H
09H	DAC reference voltage control register (DACRC)	R/W	00H
0AH	Power control register 1 (PC1)	R/W	00H
0BH	Power control register 2 (PC2)	R/W	00H
0CH	Reset control register (RC)	R/W	00H[Note1]
0DH	TEST register[Note2]	R/W	00H

Notes1. The reset control register (RC) is not initialized to 00H by generating internal reset of the reset control register (RC). For details, see **6. Reset**.

2. Rewriting to the TEST register is prohibited.

<R> 6. Reset Function

6.1 Overview of Reset Function

The RAA730502 has an on-chip reset function. The SPI control registers are initialized by reset. A reset can be generated in the following three ways:

- External reset by inputting an external reset signal to the $\overline{\text{RESET}}$ pin
- Internal reset by writing 1 to the RESET bit of the reset control register (RC)
- Internal reset by power-on-reset (POR) circuit.

The functions of the external reset and the internal reset are described below.

- After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{RESET}}$ pin before starting SPI communication.
- During reset, each function is shifted to the status shown in Table 6-1. The status of each SPI control register after reset has been acknowledged is shown in Table 6-2. After reset, the status of each pin is shown in Table 6-3.
- External reset is generated when a low-level signal is input to the $\overline{\text{RESET}}$ pin. On the other hand, internal reset is generated when 1 is written to the RESET bit of the reset control register (RC) or when the lower power supply voltage is detected by POR circuit.
- External reset is subsequently cancelled by inputting a high-level signal to $\overline{\text{RESET}}$ pin after a low-level signal is input to this pin. On the other hand, internal reset is subsequently cancelled by writing 0 to the RESET bit of the reset control register (RC) after 1 is written to the same bit of this register, or by detecting the normal power supply voltage in POR circuit after the lower power supply voltage is detected.
- The procedure of internal reset by POR circuit is described as follows. A reset occurs when the power supply voltage (AV_{DD1} to AV_{DD5}, DV_{DD}) is falling down to reach the detection voltage (V_{PDR}) or less and the reset is subsequently canceled when the power supply voltage (AV_{DD1} to AV_{DD5}, DV_{DD}) is rising up to reach the detection voltage (V_{POR}) or more. For details about the detection voltage, see 7. 4. (5) POR circuit characteristics.

Caution When generating an external reset, input a low-level signal to the $\overline{\text{RESET}}$ pin for at least 10 μs.

Table 6-1. Statuses During Reset

Function Block	External Reset from $\overline{\text{RESET}}$ Pin or Internal Reset by POR Circuit	Internal Reset by Reset Control Register (RC)
High-speed instrumentation amplifier with comparator	Operation stops.	
D/A converter	Operation stops.	
SPI	Operation stops.	Operation is enabled.

Table 6-2. Statuses of SPI Control Registers After a Reset Is Acknowledged

Address	SPI Control Register	Status After a Reset Is Acknowledged	
		External Reset Internal Reset (by POR circuit)	Internal Reset (by RC register)
00H	AMP and comparator control register 1 (ACC1)	00H	00H
01H	AMP and comparator control register 2 (ACC2)	00H	00H
02H	AMP and comparator control register 3 (ACC3)	00H	00H
03H	AMP and comparator control register 4 (ACC4)	00H	00H
04H	DAC control register 1 (DAC1C)	80H	80H
05H	DAC control register 2 (DAC2C)	80H	80H
06H	DAC control register 3 (DAC3C)	80H	80H
07H	DAC control register 4 (DAC4C)	80H	80H
08H	DAC control register 5 (DAC5C)	80H	80H
09H	DAC reference voltage control register (DACRC)	00H	00H
0AH	Power control register 1 (PC1)	00H	00H
0BH	Power control register 2 (PC2)	00H	00H
0CH	Reset control register (RC)	00H	01H[Note1]
0DH	TEST register[Note2]	00H	00H

Notes1. The reset control register (RC) is not initialized by generating internal reset of the reset control register (RC), but it can be done to 00H by generating external reset from $\overline{\text{RESET}}$ pin, or by generating internal reset in POR circuit, or by writing 0 to the RESET bit of the reset control register (RC).

2. Rewriting to the TEST register is prohibited.

Table 6-3 Pin Statuses After a Reset

Pin Name	External Reset from $\overline{\text{RESET}}$ Pin or Internal Reset by POR Circuit	Internal Reset by Reset Control Register (RC)
DAC2_OUT/VREFIN2	Pull-down input	Pull-down input
AMPINP2	Hi-Z	Hi-Z
AMPINM2	Hi-Z	Hi-Z
AMP2_OUT	Pull-down	Pull-down
CMP2_OUT	Hi-Z (open drain)	Hi-Z (open drain)
AMPINP4	Hi-Z	Hi-Z
AMPINM4	Hi-Z	Hi-Z
DAC5_OUT/VREFIN5	Pull-down input	Pull-down input
AMP4_OUT	Pull-down	Pull-down
CMP4_OUT	Hi-Z (open drain)	Hi-Z (open drain)
CMP3_OUT	Hi-Z (open drain)	Hi-Z (open drain)
AMP_OUT3	Pull-down	Pull-down
DAC4_OUT/VREFIN4	Pull-down input	Pull-down input
AMPINM3	Hi-Z	Hi-Z
AMPINP3	Hi-Z	Hi-Z
CMP1_OUT	Hi-Z (open drain)	Hi-Z (open drain)
DAC3_OUT/VREFIN3	Pull-down input	Pull-down input
AMP1_OUT	Pull-down	Pull-down
TEMP_OUT	Pull-down	Pull-down
AMPINP1	Hi-Z	Hi-Z
AMPINM1	Hi-Z	Hi-Z
DAC1_OUT/VREFIN1	Pull-down input	Pull-down input
$\overline{\text{SCLK}}$	Pull-up input	Pull-up input
SDO	Hi-Z (open drain)	Hi-Z (open drain)
SDI	Pull-up input	Pull-up input
$\overline{\text{CS}}$	Pull-up input	Pull-up input

6.2 Registers Controlling the Reset Function

(1) Reset control register (RC)

This register is used to control the reset function.

An internal reset can be generated by writing 1 to the RESET bit. The reset control register (RC) is initialized to 00H by generating external reset from $\overline{\text{RESET}}$ pin, or by generating internal reset in POR circuit, or by writing 0 to the RESET bit of the reset control register (RC).

Address: 0CH After reset: 00H[Note] R/W

Symbol	7	6	5	4	3	2	1	0
RC	0	0	0	0	0	0	0	RESET

RESET	Reset request by internal reset signal
0	Do not make a reset request by using the internal reset signal, or cancel the reset.
1	Make a reset request by using the internal reset signal, or the reset signal is currently being input.

Note The reset control register (RC) is not initialized by generating internal reset of the reset control register (RC), but it can be done to 00H by generating external reset from $\overline{\text{RESET}}$ pin, or by generating internal reset in POR circuit, or by writing 0 to the RESET bit of the reset control register (RC).

Caution When the RESET bit is 1, writing to any register other than the reset control register (RC) is ignored. Initializing the reset control register (RC) to 00H by external reset or by internal reset in POR circuit enable writing to all the registers, and also writing 0 to the RESET bit enable writing to all the registers.

Remark Bits 7 to 1 are fixed at 0. (Prohibited to be set to 1.)

7. Electrical Specifications

7.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	AV_{DD}	AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, AV_{DD5}	-0.3 to +6.0	V
	DV_{DD}	DV_{DD}	-0.3 to +6.0	V
	AGND	AGND1, AGND2, AGND3, AGND4, AGND5, AGND6, AGND7	-0.3 to +0.3	V
	DGND	DGND	-0.3 to +0.3	V
Input voltage	V_{I1}	AMPINP1, AMPINP2, AMPINP3, AMPINP4, AMPINM1, AMPINM2, AMPINM3, AMPINM4, VREFIN1, VREFIN2, VREFIN3, VREFIN4, VREFIN5, $\overline{RESET}$	-0.3 to AV_{DD} + 0.3[Note]	V
	V_{I2}	$\overline{SCLK}$, SDI, $\overline{CS}$	-0.3 to DV_{DD} + 0.3[Note]	V
Output voltage	V_{O1}	AMP1_OUT, AMP2_OUT, AMP3_OUT, AMP4_OUT, CMP1_OUT, CMP2_OUT, CMP3_OUT, CMP4_OUT, TEMP_OUT, DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, DAC5_OUT	-0.3 to AV_{DD} + 0.3[Note]	V
	V_{O2}	SDO	-0.3 to DV_{DD} + 0.3[Note]	V
Output current	I_{O1}	AMP1_OUT, AMP2_OUT, AMP3_OUT, AMP4_OUT, TEMP_OUT, DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, DAC5_OUT	1	mA
	I_{O2}	CMP1_OUT, CMP2_OUT, CMP3_OUT, CMP4_OUT	5	mA
	I_{O3}	SDO	-10	mA
Operating ambient temperature	T_A		-40 to +105	°C
<R> Storage temperature	T_{stg}		-40 to +125	°C

Note Must be 6.0 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

<R> 7.2 Operating Condition

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Power supply voltage range	V_{DDOP}	AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, AV_{DD5}, DV_{DD}	3.0	–	5.5	V
Operating temperature range	T_{OP}		-40	–	105	°C

7.3 Supply Current Characteristics

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = DV_{DD} = 5.0 V, R_{IREFR} = 56 kΩ)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Supply current	I_{stby1} Note	PC1 = 00H, PC2 = 00H	–	340	520	μA
	I_{m11} Note	PC1 = FFH, PC2 = 3FH CCn1, CCn2 = 0, 0	–	11.1	18.5	mA
	I_{m12} Note	PC1 = FFH, PC2 = 3FH CCn1, CCn2 = 0, 1	–	9.8	16.8	mA
	I_{m21} Note	PC1 = FFH, PC2 = 3FH CCn1, CCn2 = 1, 0	–	8.5	15.0	mA
	I_{m22} Note	PC1 = FFH, PC2 = 3FH CCn1, CCn2 = 1, 1	–	7.7	13.9	mA

Remark n = 1 to 4

Note Total current flowing to internal power supply pins AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, AV_{DD5}, and DV_{DD}. Current flowing through the pull-up resistor is not included. The input leakage current flowing when the level of the input pin is fixed to AV_{DD1}, AV_{DD2}, AV_{DD3}, AV_{DD4}, AV_{DD5} or DV_{DD}, or AGND1, AGND2, AGND3, AGND4, AGND5, AGND6, AGND7, or DGND is included.

7.4 Electrical Specifications of Each Block

(1) High-speed instrumentation amplifier with comparator (high-speed instrumentation amplifier block)

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = DV_{DD} = 5.0 V, VREFINn = 1.75 V, AMPnOF = 1, CMPnOF = 0, R_{IREFR} = 56 kΩ)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CCn1, CCn0 = 0, 0	–	2.04	2.82	mA
	Icc01	CCn1, CCn0 = 0, 1	–	1.7	2.36	mA
	Icc10	CCn1, CCn0 = 1, 0	–	1.28	1.88	mA
	Icc11	CCn1, CCn0 = 1, 1	–	1.02	1.58	mA
<R> Input voltage	VINL		AGND+0.72	–	–	V
	VINH		–	–	AV_{DD} - 2.0	V
Output voltage	VOUTL	IOL = -0.2 mA, CCn1, CCn0 = 0, 0	–	–	AGND+0.2	V
	VOUTH	IOH = +0.2 mA, CCn1, CCn0 = 0, 0	AV_{DD} - 0.2	–	–	V
Settling time	t_{SET_AMP00}	CCn1, CCn0 = 0, 0 GCn3, GCn2, GCn1, GCn0 = 0, 0, 0, 0 (10 dB) CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	0.6	µs
	t_{SET_AMP01}	CCn1, CCn0 = 0, 1 GCn3, GCn2, GCn1, GCn0 = 0, 0, 0, 0 (10 dB) CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	0.7	µs
	t_{SET_AMP10}	CCn1, CCn0 = 1, 0 GCn3, GCn2, GCn1, GCn0 = 0, 0, 0, 0 (10 dB) CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	1.0	µs
	t_{SET_AMP11}	CCn1, CCn0 = 1, 1 GCn3, GCn2, GCn1, GCn0 = 0, 0, 0, 0 (10 dB) CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	1.8	µs
Gain bandwidth	GBW00	RL = no load, CL = 30 pF, VREFINn = 1.5 to 1.75 V CCn1, CCn0 = 0, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	10	–	MHz
	GBW01	RL = no load, CL = 30 pF, VREFINn = 1.5 to 1.75 V CCn1, CCn0 = 0, 1 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	8.5	–	MHz
	GBW10	RL = no load, CL = 30 pF, VREFINn = 1.5 to 1.75 V CCn1, CCn0 = 1, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	7	–	MHz
	GBW11	RL = no load, CL = 30 pF, VREFINn = 1.5 to 1.75 V CCn1, CCn0 = 1, 1 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	5	–	MHz

Note These are the values for one channel of high-speed instrumentation amplifier when comparators are powered off.

Remark n = 1 to 4

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Equivalent input noise	En00	f = 1 kHz,CCn1, CCn0 = 0, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	125	–	nV/√Hz
	En01	f = 1 kHz CCn1, CCn0 = 0, 1 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	130	–	nV/√Hz
	En10	f = 1 kHz CCn1, CCn0 = 1, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	135	–	nV/√Hz
	En11	f = 1 kHz CCn1, CCn0 = 1, 1 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	155	–	nV/√Hz
Input conversion offset voltage	VOFF	CCn1, CCn0 = 0, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	-10	–	+10	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	µV/°C
Slew rate	SR00	CL = 30 pF, CCn1, CCn0 = 0, 0 GCn3, GCn2, GCn1, GCn0 = 0, 0, 0, 0 (10 dB)	–	20	–	V/µs
	SR01	CL = 30 pF, CCn1, CCn0 = 0, 1 GCn3, GCn2, GCn1, GCn0 = 0, 0, 0, 0 (10 dB)	–	15	–	V/µs
	SR10	CL = 30 pF, CCn1, CCn0 = 1, 0 GCn3, GCn2, GCn1, GCn0 = 0, 0, 0, 0 (10 dB)	–	10	–	V/µs
	SR11	CL = 30 pF, CCn1, CCn0 = 1, 1 GCn3, GCn2, GCn1, GCn0 = 0, 0, 0, 0 (10 dB)	–	5	–	V/µs
Common mode rejection ratio	CMRR00	f = 1 kHz, CCn1, CCn0 = 0, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	75	–	dB
	CMRR01	f = 1 kHz CCn1, CCn0 = 0, 1 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	74	–	dB
	CMRR10	f = 1 kHz CCn1, CCn0 = 1, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	73	–	dB
	CMRR11	f = 1 kHz CCn1, CCn0 = 1, 1 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB)	–	72	–	dB

Remark n = 1 to 4

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Power supply rejection ratio	PSRR00	f = 1 kHz, CCn1, CCn0 = 0, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB) VCM = AGND + 0.72 V to AV_{DD} - 2.5 V	–	60	–	dB
	PSRR01	f = 1 kHz, CCn1, CCn0 = 0, 1 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB) VCM = AGND + 0.72 V to AV_{DD} - 2.5 V	–	63	–	dB
	PSRR10	f = 1 kHz, CCn1, CCn0 = 1, 0 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB) VCM = AGND + 0.72 V to AV_{DD} - 2.5 V	–	65	–	dB
	PSRR11	f = 1 kHz, CCn1, CCn0 = 1, 1 GCn3, GCn2, GCn1, GCn0 = 1, 0, 0, 0 (26 dB) VCM = AGND + 0.72 V to AV_{DD} - 2.5 V	–	65	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C VCM = AGND + 0.72 V to AV_{DD} - 2.5 V	-0.8	–	0.8	dB
	GAIN_Accu2	T_A = -40 to 105°C VCM = AGND + 0.72 V to AV_{DD} - 2.5 V	-1.2	–	1.2	dB

Remark n = 1 to 4

(2) High-speed instrumentation amplifier with comparator (comparator block)

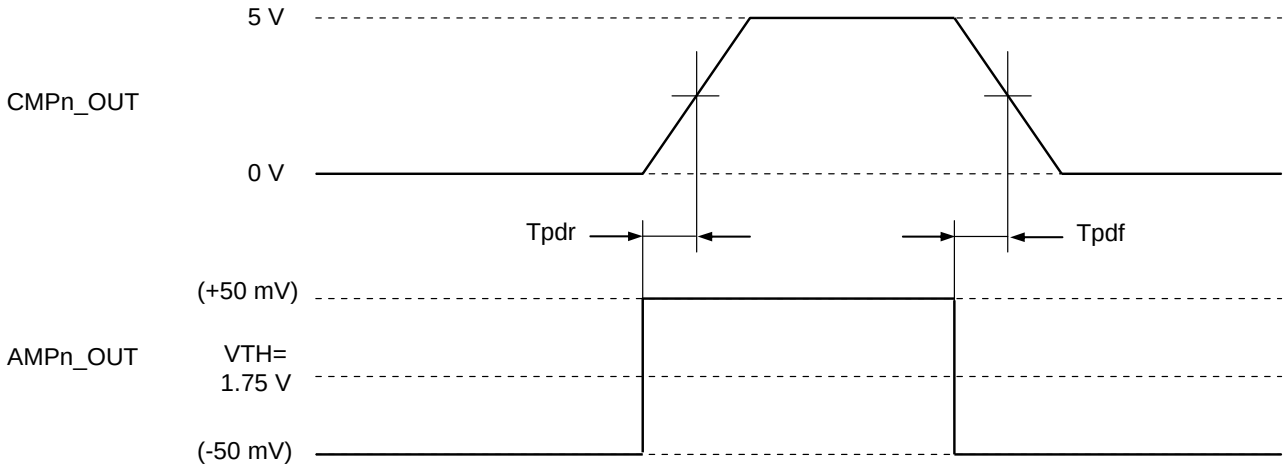
(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = DV_{DD} = 5.0V, VREFINn = 1.75 V, AMPnOF = 0, CMPnOF = 1, R_{IREFR} = 56 kΩ)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00		–	68	92	μA
Common mode input voltage	VIL	HYSn1, HYSn0 = 1, 1	AGND + 0.1	–	–	V
	VIH	HYSn1, HYSn0 = 1, 1	–	–	AV_{DD} - 2.0	V
Output voltage range	VOL	RL = 2.2 kΩ ± 1 %	–	AGND + 0.1	AGND + 0.2	V
Response time	Tpdr	VREFIN5 = 1.0V, HYSn1, HYSn0 = 1, 1, CL = 20 pF, RL = 2.2 kΩ, Overdrive voltage = 100 mV	–	100	150	ns
	Tpdf		–	40	100	ns
Hysteresis	HYST00	HYSn1, HYSn0 = 0, 0	100	200	305	mV
	HYST01	HYSn1, HYSn0 = 0, 1	45	100	151	mV
	HYST10	HYSn1, HYSn0 = 1, 0	19	50	78	mV
Input offset voltage	VOFF	VREFIN5 = 1.75 V	-10	–	10	mV

Note These are the values for one channel of comparator when high-speed instrumentation amplifiers are powered off.

Remark n = 1 to 5

Comparator response timing



Remark n=1 to 4

(3) D/A converter

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = DV_{DD} = 5.0 V, DACnOF = 1, R_{IREFR} = 56 kΩ)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	$I_{\_DAC1}$	VR2, VR1, VR0 = 0, 0, 0	–	1.37	1.72	mA
	$I_{\_DAC2}$	VR2, VR1, VR0 = 0, 1, 0	–	2.13	2.7	mA
Resolution	RES		–	–	8	bit
Settling time	t_{SET}		–	–	100	µs
Differential non-linearity error Note	DNL	VR2, VR1, VR0 = 0, 0, 0	-2	–	2	LSB
Integral non-linearity error	INL	VR2, VR1, VR0 = 0, 0, 0	-2	–	2	LSB

Note Guaranteed monotonic.

(4) Temperature sensor

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = DV_{DD} = 5.0 V, TEMPOF = 1, R_{IREFR} = 56 kΩ)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	320	650	µA
Output voltage	V_O	Ta = 25°C	–	1.67	–	V
Temperature sensitivity	T_{SE}		–	-5.0	–	mV/°C

(5) POR circuit characteristics

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = DV_{DD} = 5.0 V, TEMPOF = 1, R_{IREFR} = 56 kΩ)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Detection voltage	V_{POR}	When power supply voltage is rising	1.45	2.19	2.8	V
	V_{PDR}	When power supply voltage is falling	1.3	1.98	2.55	V
Minimum pulse width	T_{PW}		200	–	–	µs

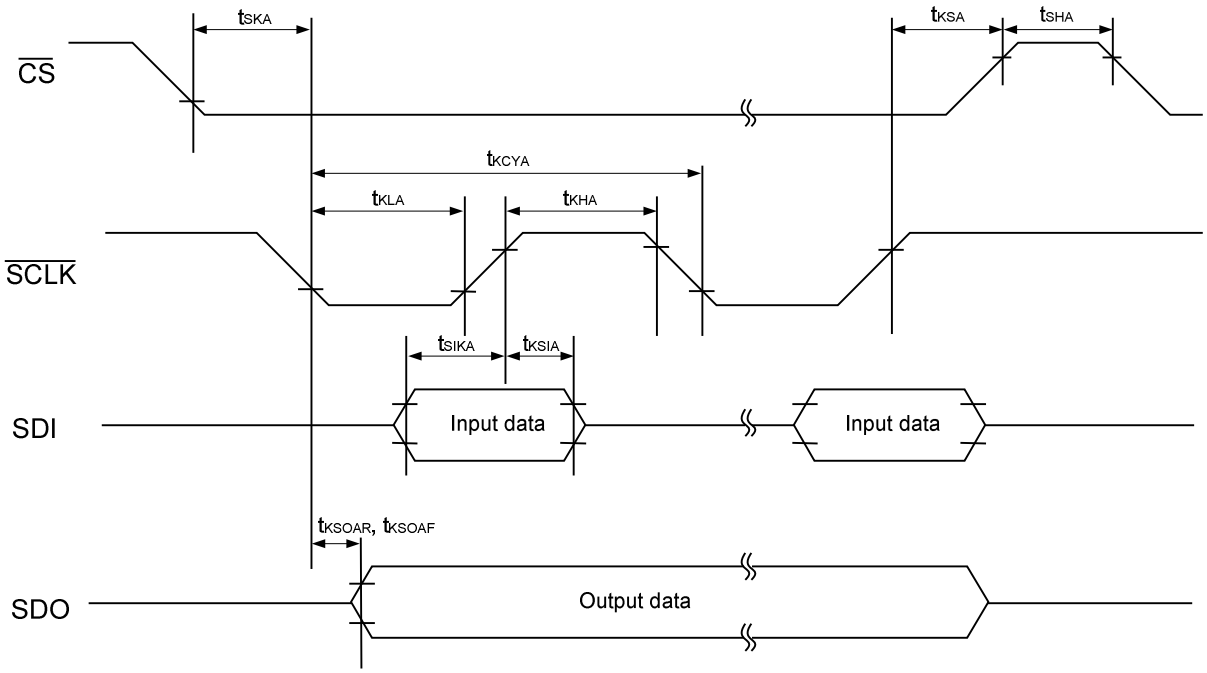
(6) SPI

(-40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = AV_{DD5} = DV_{DD} = 5.0 V)

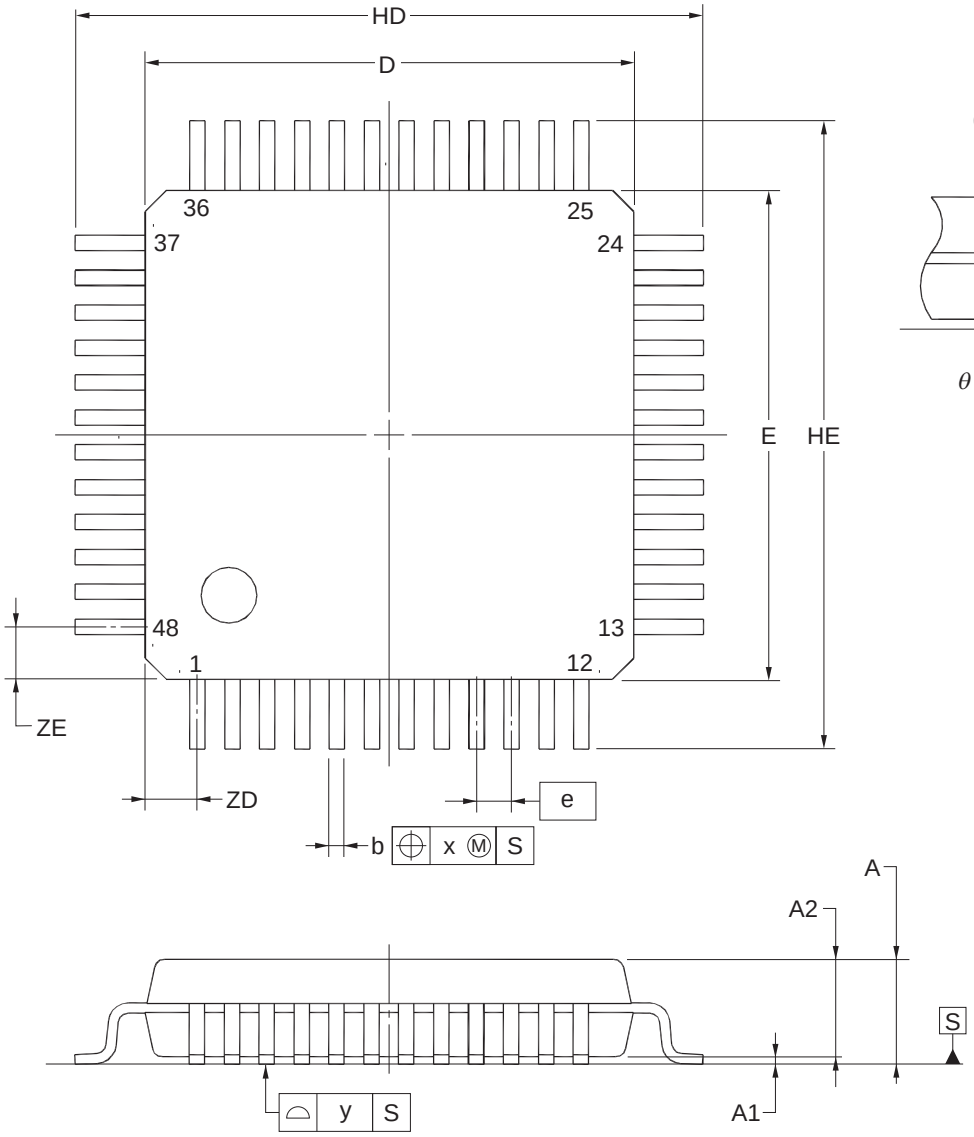
Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input voltage, high	V_{IH}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin, $\overline{RESET}$ pin	2.0	DV_{DD}	DV_{DD} + 0.1	V
Input voltage, low	V_{IL}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin, $\overline{RESET}$ pin	-0.1	DGND	0.7	V
Leakage current during high level input	I_{leak_Hi1}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	-1	–	2	µA
	I_{leak_Hi2}	$\overline{RESET}$ pin	-1	–	2	µA
Leakage current during low level input	I_{leak_Lo1}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	50	100	200	µA
	I_{leak_Lo2}	$\overline{RESET}$ pin	-1	–	2	µA
<R> Low-level output voltage at SDO pin	V_{SDO_Lo}	Io = -5 mA	–	120	300	mV
Leakage current when SDO pin is off	I_{leak_SDO}		-1	–	2	µA
Pull-up resistance	R_{SPI}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	32.5	50	67.5	kΩ
$\overline{SCLK}$ cycle time	t_{KCYA}		100	–	–	ns
$\overline{SCLK}$ high-level width low-level width	t_{KHA}, t_{KLA}		0.9t_{KCYA}/2	–	–	ns
SDI setup time (to $\overline{SCLK}$ ↑)	t_{SIKA}		40	–	–	ns
<R> SDI hold time (from $\overline{SCLK}$ ↑)	t_{KSIA}		10	–	–	ns
Delay time from $\overline{SCLK}$ ↓ to SDO output	t_{KSOAR}	Pull-up resistance = 10 kΩ, CL = 5 pF, VSDO = 5 V	–	250	300	ns
	t_{KSOAF}	Pull-up resistance = 10 kΩ, CL = 5 pF, VSDO = 5 V	–	–	20	ns
$\overline{CS}$ high-level width	t_{SHA}		200	–	–	ns
Delay time from CS ↓ to $\overline{SCLK}$ ↓	t_{SKA}		200	–	–	ns
Delay time from $\overline{SCLK}$ ↑ to CS ↑	t_{KSA}		200	–	–	ns

Note Including the current flowing into each pull-up resistor

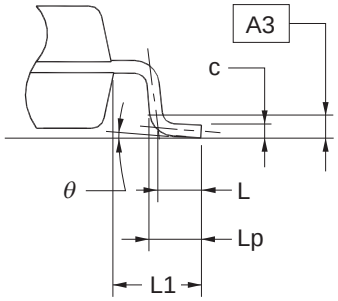
SPI transfer clock timing



8. Package Drawing



detail of lead end



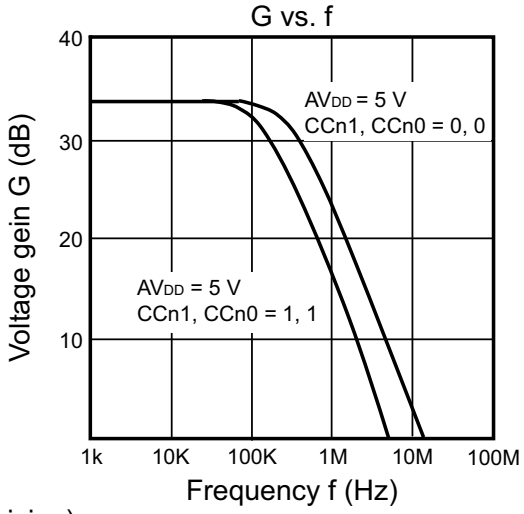
(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

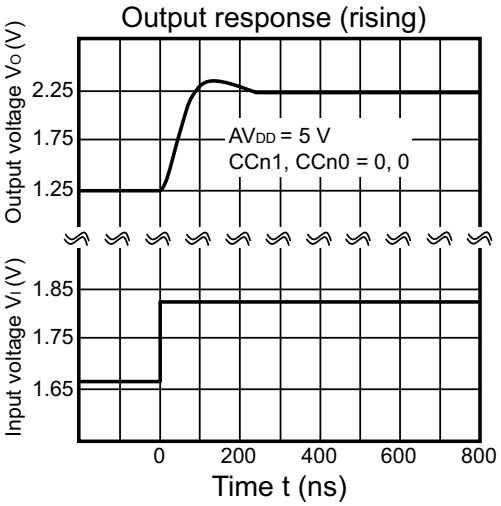
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

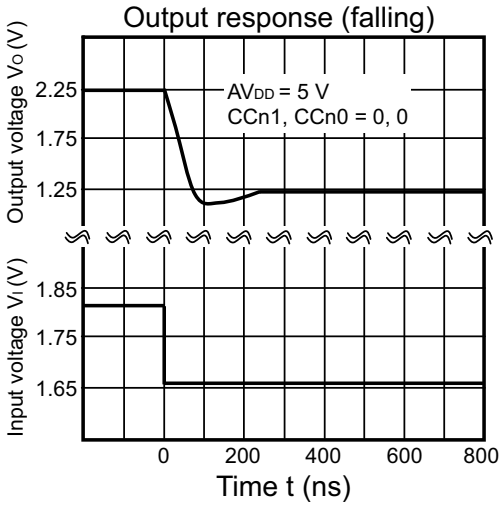
Characteristics Curve (T_A = 25°C, TYP.) (reference value)

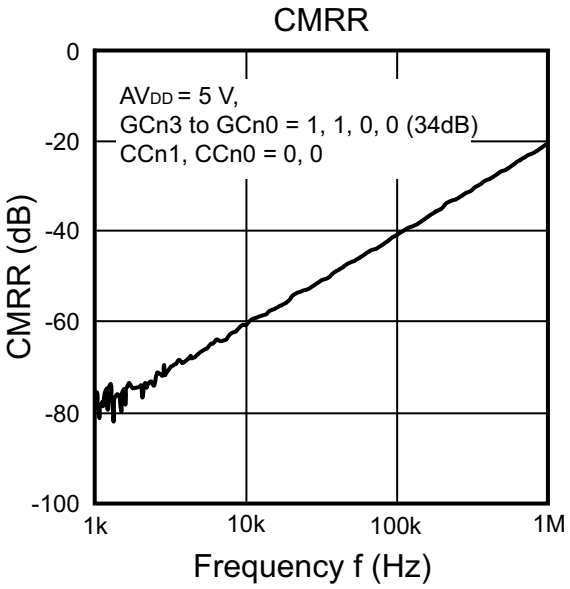
- **High-speed instrumentation amplifier with comparator (High-speed instrumentation amplifier block)**

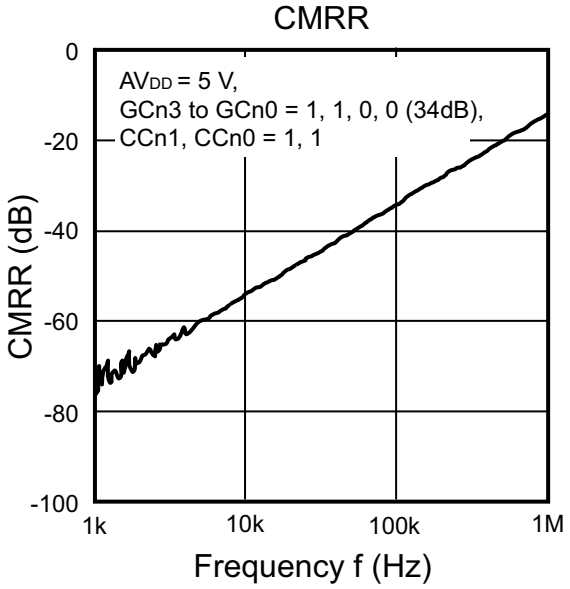


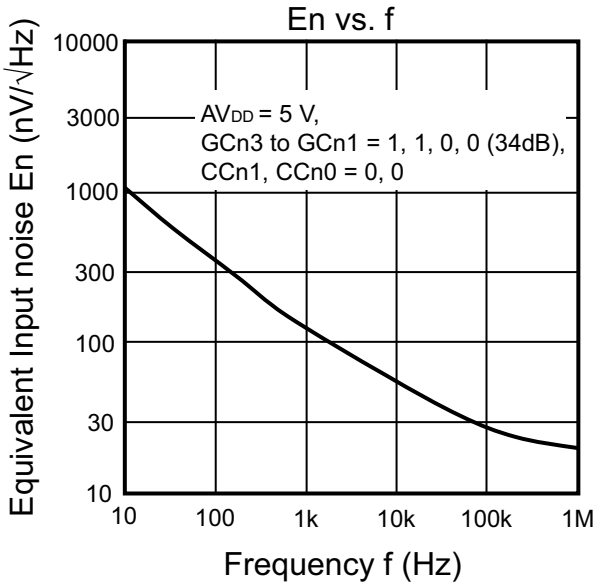
Remark: n=1 to 4





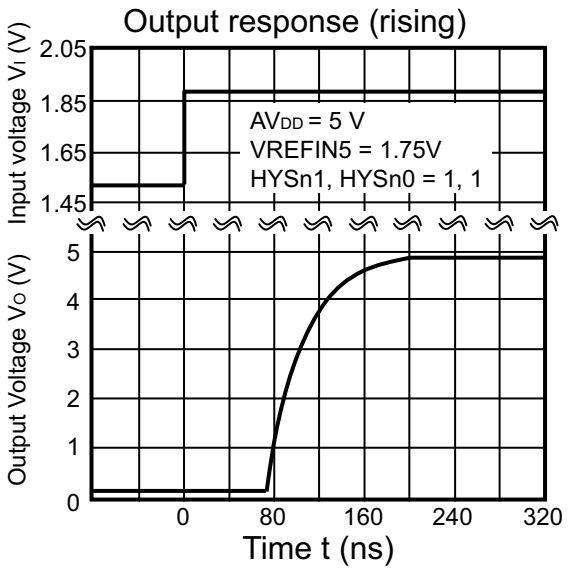


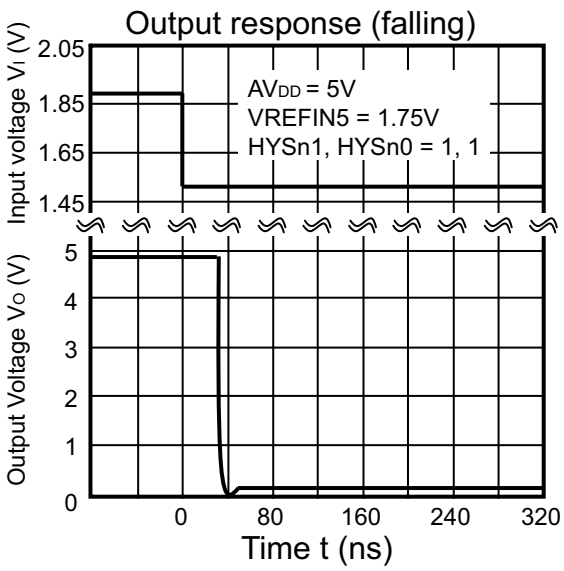




Remark: n=1 to 4

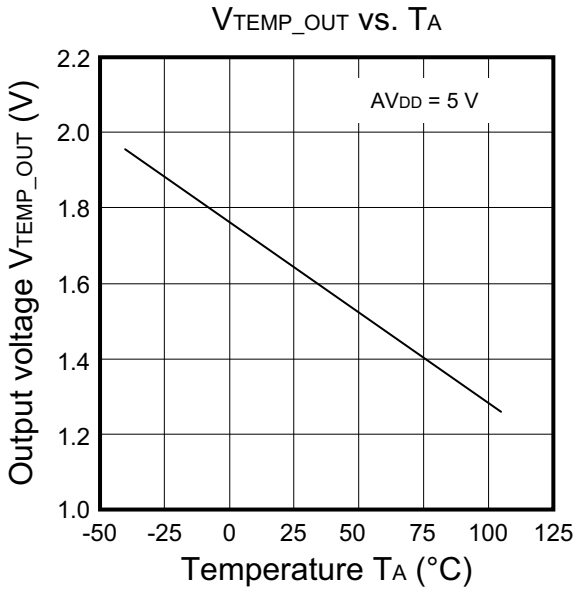
- **High-speed instrumentation amplifier with comparator (comparator block)**





Remark: n=1 to 4

- **Temperature sensor**



Rev.	Date	Description	
		Page	Summary
0.01	Sep. 5, 2011	–	First edition issued.
0.02	Mar. 9, 2012	7	Addition of pin ($\overline{\text{RESET}}$) to *Table 1-2 Connection of Unused Pins*
		11	Change of equivalent circuit diagrams in *Figure 1-1 Pin I/O Circuit Type (4/5)*
		27	Change of description in *5.2 SPI Communication* and change of *Figure 5-2 SPI Communication Timing*
		28	Change of *Table 6-1 Statuses During Reset*
		30	Addition of *Table 6-3 Pin Statuses After a Reset*
		32	Change of unit of output current I_{O1} in *7.1 Absolute Maximum Ratings*
			Addition of output current I_{O3} to *7.1 Absolute Maximum Ratings*
		33	Addition of new conditions (AV_{DD1} to AV_{DD5} and DV_{DD}) to *7.2 Power supply voltage*
		35	Change of ratings in *7.4 (1) Gain bandwidth*
		36	Addition of input conversion offset voltage temperature coeffifient VOTC to *(1) High-speed instrumentation amplifier with comparator (high-speed instrumentation amplifier block)*
			Deletion of GAIN_Accu2 from *(1) High-speed instrumentation amplifier with comparator (high-speed instrumentation amplifier block)*
		39	Change of unit and ratings of integral non-linearity error in *7.4 (3) Settling time*
		40	Addition of lieak_Hi2 and lieak_Lo2 to *7.4 (5) SPI interface*
			Change of ratings of t_{KSOAR} in *7.4 (5) SPI interface*
			Addition of Note to *7.4 (5) SPI interface*
1.00	Aug. 31, 2012	2	Addition of Ordering Information and Part No.
		13	Change of equivalent circuit diagrams in *Figure 1-1 Pin I/O Circuit Type (5/5)*
		31	Detection of I/O from *Table 6-3 Pin statuses After a Reset*
		44	Addition of characteristics curve (T_A = 25°C, TYP.) (reference)
1.01	Sep. 07, 2012	41	Change of ratings in *7.4 (6) SPI interface*
1.10	Jan. 31, 2013	39	Change of ratings of Response time in *7. 4. (2) High-speed instrumentation amplifier with comparator (comparator block)*
		41	Detection of F_{SCLK} in *7. 4. (6) SPI*
			Addition of Pull-up resistance in *7. 4. (6) SPI*
1.20	May. 31, 2014	14	Change of description about reference voltage in *2. 1 Overview of High-Speed Instrumentation Amplifiers with Comparators*
		18	Change of the calculating formula about output voltage in *3. 1 Overview of D/A Converter Features*
		19	Change of description in *3. 3 (2) DAC reference voltage control register (DACRC)*
		26	Addition of Caution about external reset to *5. SPI*
		28	Change of description in *6. Reset*
		32	Deletion of Junction temperature from *7. 1 Absolute Maximum Ratings*
		33	Change of the title to "*Operation condition"* in *7. 2*
		34	Addition of the value for gain setting error in *7. 4 (1)*
		39	Correction of the value (TYP.) for low-level output voltage at SDO pin and of the value for SDI hold time in *7. 4 (6)*

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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