# DDR2 SDRAM SORDIMM

## MT18HTS25672RHZ – 2GB

## Features

- 200-pin, small-outline registered dual in-line memory module (SORDIMM)
- Fast data transfer rates: PC2-4200, PC2-5300, or PC2-6400
- 2GB (256 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD}$ = 1.8V
- $V_{DDSPD}$ = 3.0–3.6V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- $4n$-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 $^tCK$
- Programmable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Phase-lock loop (PLL) to reduce system clock line loading
- Gold edge contacts
- Dual rank, using 2Gb TwinDie™ devices
- Halogen-free
- Combination Temp Sensor/EEPROM

### Figure 1: 200-Pin SORDIMM (R/C B)

Module height: 30mm (1.181 in)
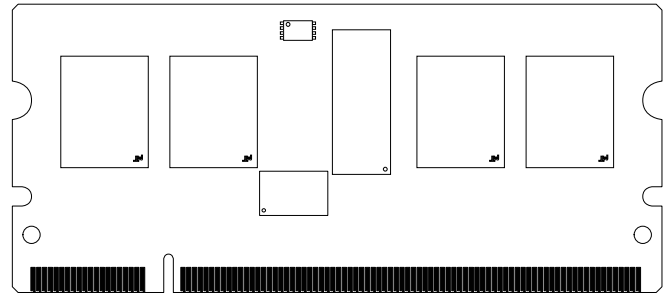


## Options / Marking

- Operating temperature
  - Commercial (0°C ≤ $T_A$ ≤ +70°C) — None
  - Industrial (–40°C ≤ $T_A$ ≤ +85°C)[1] — I
- Package
  - 200-pin DIMM (Halogen-free) — Z
- Frequency/CL[2]
  - 2.5 @ CL = 5 (DDR2-800) — -80E
  - 2.5 @ CL = 6 (DDR2-800) — -800
  - 3.0ns @ CL = 5 (DDR2-667) — -667

Notes: 1. Contact Micron for industrial temperature module offerings.
2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

## Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | | $^tRCD$ (ns) | $^tRP$ (ns) | $^tRC$ (ns) |
|---|---|---|---|---|---|---|---|---|
| | | CL = 6 | CL = 5 | CL = 4 | CL = 3 | | | |
| -80E | PC2-6400 | 800 | 800 | 533 | 400 | 12.5 | 12.5 | 55 |
| -800 | PC2-6400 | 800 | 667 | 533 | 400 | 15 | 15 | 55 |
| -667 | PC2-5300 | – | 667 | 553 | 400 | 15 | 15 | 55 |
| -53E | PC2-4200 | – | – | 553 | 400 | 15 | 15 | 55 |
| -40E | PC2-3200 | – | – | 400 | 400 | 15 | 15 | 55 |

Products and specifications discussed herein are subject to change by Micron without notice.

**Table 2: Addressing**

| Parameter | 1GB |
|---|---|
| Refresh count | 8K |
| Row address | 16K A[13:0] |
| Device bank address | 8 BA[2:0] |
| Device configuration | 2Gb TwinDie (256 Meg x 8) |
| Column address | 1K A[9:0] |
| Module rank address | 2 S#[1:0] |

**Table 3: Part Numbers and Timing Parameters – 2GB Modules**

Base device: MT47H256M8,[1] 2Gb DDR2 TwinDie SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-tRCD-tRP) |
|---|---|---|---|---|---|
| MT18HTS25672RH(I)Z-80E__ | 2GB | 256 Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 5-5-5 |
| MT18HTS25672RH(I)Z-800__ | 2GB | 256Meg x 72 | 6.4 GB/s | 2.5ns/800 MT/s | 6-6-6 |
| MT18HTS25672RH(I)Z-667__ | 2GB | 256 Meg x 72 | 5.3 GB/s | 3.0ns/667 MT/s | 5-5-5 |

Notes: 1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT18HTS25672RHZ-80EM1.

# Pin Assignments

### Table 4: Pin Assignments

| 200-Pin SORDIMM Front | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | $V_{REF}$ | 51 | DQ18 | 101 | $V_{DD}$ | 151 | $V_{SS}$ |
| 3 | DQ0 | 53 | DQ19 | 103 | A5 | 153 | DQS5# |
| 5 | $V_{SS}$ | 55 | $V_{SS}$ | 105 | A3 | 155 | DQS5 |
| 7 | DQ1 | 57 | DQ24 | 107 | A2 | 157 | $V_{SS}$ |
| 9 | DQS0# | 59 | DQ25 | 109 | $V_{DD}$ | 159 | DQ42 |
| 11 | DQS0 | 61 | $V_{SS}$ | 111 | A10 | 161 | DQ43 |
| 13 | $V_{SS}$ | 63 | DQS3# | 113 | BA0 | 163 | $V_{SS}$ |
| 15 | DQ2 | 65 | DQS3 | 115 | RAS# | 165 | DQ48 |
| 17 | DQ3 | 67 | $V_{SS}$ | 117 | $V_{DD}$ | 167 | DQ49 |
| 19 | $V_{SS}$ | 69 | DQ26 | 119 | CAS# | 169 | $V_{SS}$ |
| 21 | DQ8 | 71 | DQ27 | 121 | S1# | 171 | DQS6# |
| 23 | DQ9 | 73 | $V_{SS}$ | 123 | $V_{DD}$ | 173 | DQS6 |
| 25 | $V_{SS}$ | 75 | CB0 | 125 | ODT1 | 175 | $V_{SS}$ |
| 27 | DQS1# | 77 | CB1 | 127 | NC | 177 | DQ50 |
| 29 | DQS1 | 79 | $V_{SS}$ | 129 | DQ32 | 179 | DQ51 |
| 31 | $V_{SS}$ | 81 | DQS8# | 131 | $V_{SS}$ | 181 | $V_{SS}$ |
| 33 | DQ10 | 83 | DQS8 | 133 | DQ33 | 183 | DQ56 |
| 35 | DQ11 | 85 | $V_{SS}$ | 135 | DQS4# | 185 | DQ57 |
| 37 | $V_{SS}$ | 87 | CKE0 | 137 | DQS4 | 187 | $V_{SS}$ |
| 39 | DQ16 | 89 | CKE1 | 139 | $V_{SS}$ | 189 | DQS7# |
| 41 | DQ17 | 91 | EVENT# | 141 | DQ34 | 191 | DQS7 |
| 43 | $V_{SS}$ | 93 | $V_{DD}$ | 143 | DQ35 | 193 | DQ58 |
| 45 | DQS2# | 95 | A12 | 145 | $V_{SS}$ | 195 | $V_{SS}$ |
| 47 | DQS2 | 97 | A9 | 147 | DQ40 | 197 | DQ59 |
| 49 | $V_{SS}$ | 99 | A7 | 149 | DQ41 | 199 | $V_{DDSPD}$ |

| 200-Pin SORDIMM Back | | | | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 2 | $V_{SS}$ | 52 | $V_{SS}$ | 102 | A6 | 152 | $V_{SS}$ |
| 4 | DQ4 | 54 | DQ28 | 104 | A4 | 154 | DM5 |
| 6 | DQ5 | 56 | DQ29 | 106 | $V_{DD}$ | 156 | $V_{SS}$ |
| 8 | $V_{SS}$ | 58 | $V_{SS}$ | 108 | A1 | 158 | DQ46 |
| 10 | DM0 | 60 | DM3 | 110 | A0 | 160 | DQ47 |
| 12 | $V_{SS}$ | 62 | $V_{SS}$ | 112 | BA1 | 162 | $V_{SS}$ |
| 14 | DQ6 | 64 | DQ30 | 114 | $V_{DD}$ | 164 | DQ52 |
| 16 | DQ7 | 66 | DQ31 | 116 | WE# | 166 | DQ53 |
| 18 | $V_{SS}$ | 68 | $V_{SS}$ | 118 | S0# | 168 | $V_{SS}$ |
| 20 | DQ12 | 70 | CB4 | 120 | ODT0 | 170 | DM6 |
| 22 | DQ13 | 72 | CB5 | 122 | A13 | 172 | $V_{SS}$ |
| 24 | $V_{SS}$ | 74 | $V_{SS}$ | 124 | $V_{DD}$ | 174 | DQ54 |
| 26 | DM1 | 76 | DM8 | 126 | CK0 | 176 | DQ55 |
| 28 | $V_{SS}$ | 78 | $V_{SS}$ | 128 | CK0# | 178 | $V_{SS}$ |
| 30 | DQ14 | 80 | CB6 | 130 | $V_{SS}$ | 180 | DQ60 |
| 32 | DQ15 | 82 | CB7 | 132 | DQ36 | 182 | DQ61 |
| 34 | $V_{SS}$ | 84 | $V_{SS}$ | 134 | DQ37 | 184 | $V_{SS}$ |
| 36 | DQ20 | 86 | CB2 | 136 | $V_{SS}$ | 186 | DM7 |
| 38 | DQ21 | 88 | CB3 | 138 | DM4 | 188 | DQ62 |
| 40 | $V_{SS}$ | 90 | $V_{SS}$ | 140 | $V_{SS}$ | 190 | $V_{SS}$ |
| 42 | RESET# | 92 | BA2 | 142 | DQ38 | 192 | DQ63 |
| 44 | DM2 | 94 | NC | 144 | DQ39 | 194 | SDA |
| 46 | $V_{SS}$ | 96 | A11 | 146 | $V_{SS}$ | 196 | SCL |
| 48 | DQ22 | 98 | $V_{DD}$ | 148 | DQ44 | 198 | SA1 |
| 50 | DQ23 | 100 | A8 | 150 | DQ45 | 200 | SA0 |

## Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR2 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

**Table 5: Pin Descriptions**

| Symbol | Type | Description |
|---|---|---|
| Ax | Input | **Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information. |
| BAx | Input | **Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command. |
| CKx, CK#x | Input | **Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. |
| CKEx | Input | **Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DDR2 SDRAM. |
| DMx | Input | **Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. |
| ODTx | Input | **On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command. |
| Par_In | Input | **Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#. |
| RAS#, CAS#, WE# | Input | **Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| RESET# | Input | **Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z. |
| S#x | Input | **Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder. |
| SAx | Input | **Serial address inputs:** Used to configure the SPD EEPROM address range on the I$^2$C bus. |
| SCL | Input | **Serial clock for SPD EEPROM:** Used to synchronize communication to and from the SPD EEPROM on the I$^2$C bus. |
| CBx | I/O | **Check bits.** Used for system error detection and correction. |
| DQx | I/O | **Data input/output:** Bidirectional data bus. |
| DQSx, DQS#x | I/O | **Data strobe:** Travels with the DQ and is used to capture DQ at the DRAM or the controller. Output with read data; input with write data for source synchronous operation. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command. |

**Table 5: Pin Descriptions (Continued)**

| Symbol | Type | Description |
|---|---|---|
| SDA | I/O | **Serial data:** Used to transfer addresses and data into and out of the SPD EEPROM on the $I^2C$ bus. |
| RDQSx, RDQS#x | Output | **Redundant data strobe (x8 devices only):** RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, RDQS becomes data mask (see DMx). RDQS# is only used when RDQS is enabled and differential data strobe mode is enabled. |
| Err_Out# | Output (open drain) | **Parity error output:** Parity error found on the command and address bus. |
| $V_{DD}/V_{DDQ}$ | Supply | **Power supply:** 1.8V ±0.1V. The component $V_{DD}$ and $V_{DDQ}$ are connected to the module $V_{DD}$. |
| $V_{DDSPD}$ | Supply | **SPD EEPROM power supply:** 1.7–3.6V. |
| $V_{REF}$ | Supply | **Reference voltage:** $V_{DD}/2$. |
| $V_{SS}$ | Supply | Ground. |
| NC | – | **No connect:** These pins are not connected on the module. |
| NF | – | **No function:** These pins are connected within the module, but provide no functionality. |
| NU | – | **Not used:** These pins are not used in specific module configurations/operations. |
| RFU | – | Reserved for future use. |

# Functional Block Diagram

## Figure 2: Functional Block Diagram
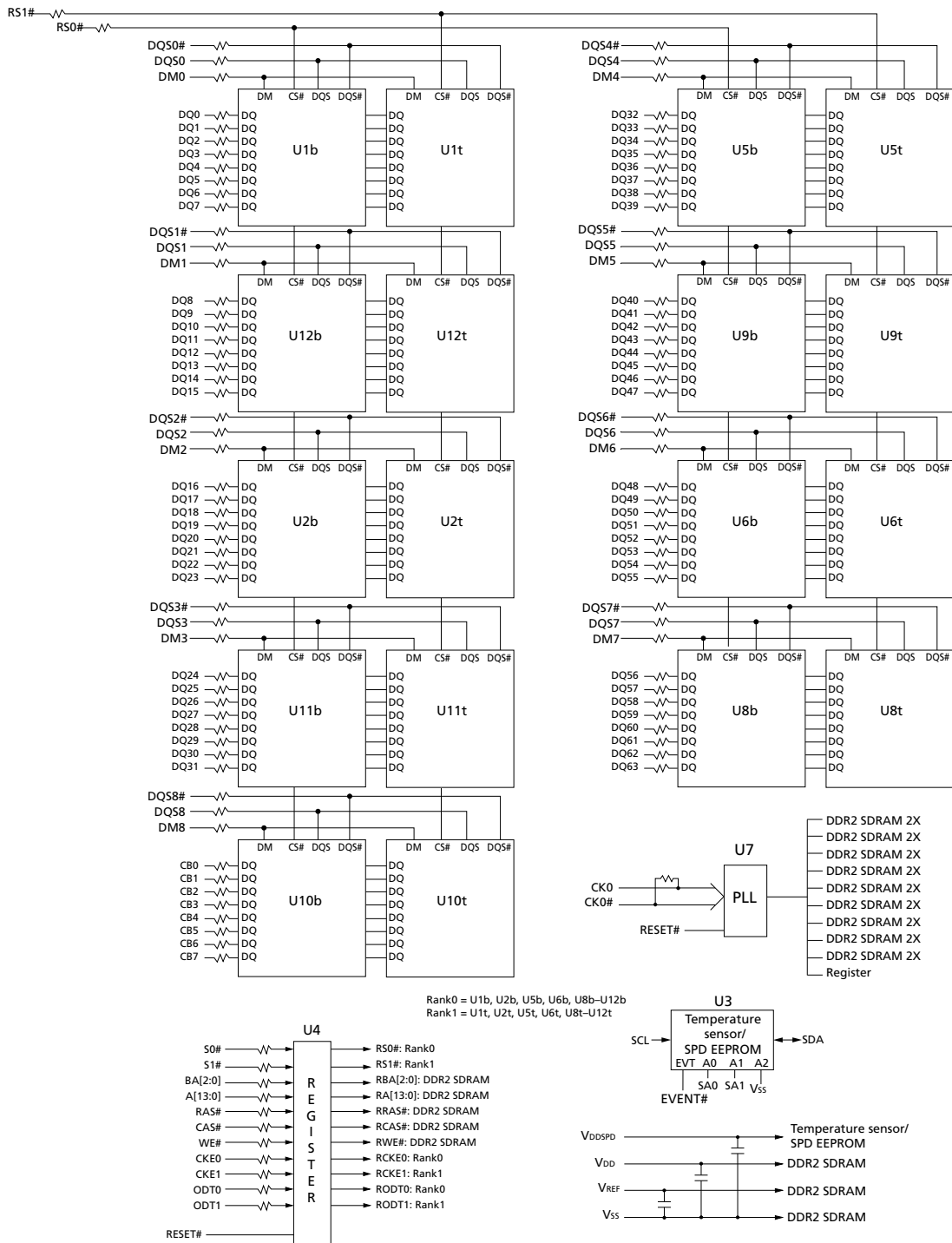
# General Description

DDR2 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 4 or 8-bank DDR2 SDRAM devices. DDR2 SDRAM modules use DDR architecture to achieve high-speed operation. DDR2 architecture is essentially a $4n$-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding $n$-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR2 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals. A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

## Serial Presence-Detect EEPROM Operation

DDR2 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard $I^2C$ bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to $V_{SS}$, permanently disabling hardware write protection.

# Register and PLL Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The registers and PLL minimize system and clock loading. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

## Temperature Sensor

An on-board temperature sensor provides the ability to monitor the module temperature along with monitoring alarms. Programmable registers can be used to specify temperature events and critical boundaries. An EVENT# pin is used to signal when different conditions occur based on how the registers are defined.

# Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 6: Absolute Maximum Ratings**

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage relative to $V_{SS}$ | | −0.5 | 2.3 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | | −0.5 | 2.3 | V |
| $I_I$ | Input leakage current; Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$; $V_{REF}$ input 0V ≤ $V_{IN}$ ≤ 0.95V; (All other pins not under test = 0V) | Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA | −5 | 5 | µA |
| | | CK0, CK0# | −250 | 250 | |
| | | DM | −10 | 10 | |
| $I_{OZ}$ | Output leakage current; 0V ≤ $V_{OUT}$ ≤ $V_{DDQ}$; DQ and ODT are disabled | DQ, DQS, DQS# | −10 | 10 | µA |
| $I_{VREF}$ | $V_{REF}$ leakage current; $V_{REF}$ = valid $V_{REF}$ level | | −36 | 36 | µA |
| $T_A$ | Module ambient operating temperature | Commercial | 0 | 70 | °C |
| | | Industrial | −40 | 85 | °C |
| $T_C$[1] | DDR2 SDRAM component operating temperature[2] | Commercial | 0 | 85 | °C |
| | | Industrial | −40 | 95 | °C |

Notes: 1. The refresh rate is required to double when $T_C$ exceeds 85°C.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

# DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades.

**Table 7: Module and Component Speed Grades**

DDR2 components may exceed the listed module speed grades; module may not be available in all listed speed grades

| Module Speed Grade | Component Speed Grade |
|---|---|
| -1GA | -187E |
| -80E | -25E |
| -800 | -25 |
| -667 | -3 |
| -53E | -37E |
| -40E | -5E |

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

# IDD Specifications

### Table 8: DDR2 $I_{DD}$ Specifications and Conditions – 2GB (Die Revision H)

Values shown for MT47H256M8 DDR2 SDRAM only and are computed from values specified in the 2Gb TwinDie(256 Meg x 8) component data sheet

| Parameter | | Combined Symbol | -80E | -667 | Units |
|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^tCK = {}^tCK$ ($I_{DD}$), $^tRC = {}^tRC$ ($I_{DD}$), $^tRAS = {}^tRAS$ MIN ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{CDD0}$ | 648 | 603 | mA |
| **Operating one bank active-read-precharge current:** $I_{OUT} = 0mA$; BL = 4, CL = CL ($I_{DD}$), AL = 0; $^tCK = {}^tCK$ ($I_{DD}$), $^tRC = {}^tRC$ ($I_{DD}$), $^tRAS = {}^tRAS$ MIN ($I_{DD}$), $^tRCD = {}^tRCD$ ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as $I_{DD4W}$ | | $I_{CDD1}$ | 738 | 693 | mA |
| **Precharge power-down current:** All device banks idle; $^tCK = {}^tCK$ ($I_{DD}$); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{CDD2P}$ | 126 | 126 | mA |
| **Precharge quiet standby current:** All device banks idle; $^tCK = {}^tCK$ ($I_{DD}$); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | | $I_{CDD2Q}$ | 279 | 279 | mA |
| **Precharge standby current:** All device banks idle; $^tCK = {}^tCK$ ($I_{DD}$); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{CDD2N}$ | 315 | 279 | mA |
| **Active power-down current:** All device banks open; $^tCK = {}^tCK$ ($I_{DD}$); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | $I_{CDD3P}$ | 243 | 198 | mA |
| | Slow PDN exit MR[12] = 1 | | 153 | 153 | |
| **Active standby current:** All device banks open; $^tCK = {}^tCK$ ($I_{DD}$), $^tRAS = {}^tRAS$ MAX ($I_{DD}$), $^tRP = {}^tRP$ ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{CDD3N}$ | 360 | 333 | mA |
| **Operating burst write current:** All device banks open; Continuous burst writes; BL = 4, CL = CL ($I_{DD}$), AL = 0; $^tCK = {}^tCK$ ($I_{DD}$), $^tRAS = {}^tRAS$ MAX ($I_{DD}$), $^tRP = {}^tRP$ ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{CDD4W}$ | 1188 | 1098 | mA |
| **Operating burst read current:** All device banks open; Continuous burst read, $I_{OUT} = 0mA$; BL = 4, CL = CL ($I_{DD}$), AL = 0; $^tCK = {}^tCK$ ($I_{DD}$), $^tRAS = {}^tRAS$ MAX ($I_{DD}$), $^tRP = {}^tRP$ ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | $I_{CDD4R}$ | 1143 | 1053 | mA |
| **Burst refresh current:** $^tCK = {}^tCK$ ($I_{DD}$); REFRESH command at every $^tRFC$ ($I_{DD}$) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | $I_{CDD5}$ | 1368 | 1323 | mA |
| **Self refresh current:** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating | | $I_{CDD6}$ | 126 | 126 | mA |

**Table 8: DDR2 I$_{DD}$ Specifications and Conditions – 2GB (Die Revision H) (Continued)**

Values shown for MT47H256M8 DDR2 SDRAM only and are computed from values specified in the 2Gb TwinDie(256 Meg x 8) component data sheet

| Parameter | Combined Symbol | -80E | -667 | Units |
|---|---|---|---|---|
| **Operating bank interleave read current:** All device banks interleaving reads; I$_{OUT}$ = 0mA; BL = 4, CL = CL (I$_{DD}$), AL = $^t$RCD (I$_{DD}$) - 1 × $^t$CK (I$_{DD}$); $^t$CK = $^t$CK (I$_{DD}$), $^t$RC = $^t$RC (I$_{DD}$), $^t$RRD = $^t$RRD (I$_{DD}$), $^t$RCD = $^t$RCD (I$_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | I$_{CDD7}$ | 1953 | 1728 | mA |

**Table 9: DDR2 I$_{DD}$ Specifications and Conditions – 2GB (Die Revision M)**

Values shown for MT47H256M8 DDR2 SDRAM only and are computed from values specified in the 2Gb TwinDie(256 Meg x 8) component data sheet

| Parameter | | Combined Symbol | -80E | -667 | Units |
|---|---|---|---|---|---|
| **Operating one bank active-precharge current:** $^t$CK = $^t$CK (I$_{DD}$), $^t$RC = $^t$RC (I$_{DD}$), $^t$RAS = $^t$RAS MIN (I$_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | I$_{CDD0}$ | 720 | 675 | mA |
| **Operating one bank active-read-precharge current:** I$_{OUT}$ = 0mA; BL = 4, CL = CL (I$_{DD}$), AL = 0; $^t$CK = $^t$CK (I$_{DD}$), $^t$RC = $^t$RC (I$_{DD}$), $^t$RAS = $^t$RAS MIN (I$_{DD}$), $^t$RCD = $^t$RCD (I$_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I$_{DD4W}$ | | I$_{CDD1}$ | 810 | 764 | mA |
| **Precharge power-down current:** All device banks idle; $^t$CK = $^t$CK (I$_{DD}$); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | | I$_{CDD2P}$ | 180 | 180 | mA |
| **Precharge quiet standby current:** All device banks idle; $^t$CK = $^t$CK (I$_{DD}$); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating | | I$_{CDD2Q}$ | 306 | 306 | mA |
| **Precharge standby current:** All device banks idle; $^t$CK = $^t$CK (I$_{DD}$); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching | | I$_{CDD2N}$ | 387 | 351 | mA |
| **Active power-down current:** All device banks open; $^t$CK = $^t$CK (I$_{DD}$); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating | Fast PDN exit MR[12] = 0 | I$_{CDD3P}$ | 360 | 342 | mA |
| | Slow PDN exit MR[12] = 1 | | 270 | 270 | |
| **Active standby current:** All device banks open; $^t$CK = $^t$CK (I$_{DD}$), $^t$RAS = $^t$RAS MAX (I$_{DD}$), $^t$RP = $^t$RP (I$_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | | I$_{CDD3N}$ | 432 | 405 | mA |
| **Operating burst write current:** All device banks open; Continuous burst writes; BL = 4, CL = CL (I$_{DD}$), AL = 0; $^t$CK = $^t$CK (I$_{DD}$), $^t$RAS = $^t$RAS MAX (I$_{DD}$), $^t$RP = $^t$RP (I$_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | | I$_{CDD4W}$ | 1260 | 1170 | mA |

**Table 9: DDR2 $I_{DD}$ Specifications and Conditions – 2GB (Die Revision M) (Continued)**

Values shown for MT47H256M8 DDR2 SDRAM only and are computed from values specified in the 2Gb TwinDie(256 Meg x 8) component data sheet

| Parameter | Combined Symbol | -80E | -667 | Units |
|---|---|---|---|---|
| **Operating burst read current:** All device banks open; Continuous burst read, $I_{OUT}$ = 0mA; BL = 4, CL = CL ($I_{DD}$), AL = 0; $^tCK$ = $^tCK$ ($I_{DD}$), $^tRAS$ = $^tRAS$ MAX ($I_{DD}$), $^tRP$ = $^tRP$ ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching | $I_{CDD4R}$ | 1215 | 1125 | mA |
| **Burst refresh current:** $^tCK$ = $^tCK$ ($I_{DD}$); REFRESH command at every $^tRFC$ ($I_{DD}$) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching | $I_{CDD5}$ | 1530 | 1485 | mA |
| **Self refresh current:** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating | $I_{CDD6}$ | 126 | 126 | mA |
| **Operating bank interleave read current:** All device banks interleaving reads; $I_{OUT}$ = 0mA; BL = 4, CL = CL ($I_{DD}$), AL = $^tRCD$ ($I_{DD}$) - 1 × $^tCK$ ($I_{DD}$); $^tCK$ = $^tCK$ ($I_{DD}$), $^tRC$ = $^tRC$ ($I_{DD}$), $^tRRD$ = $^tRRD$ ($I_{DD}$), $^tRCD$ = $^tRCD$ ($I_{DD}$); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching | $I_{CDD7}$ | 2025 | 1800 | mA |

# Register and PLL Specifications

## Table 10: Register Specifications

SSTU32872 devices or equivalent

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---|---|---|---|---|---|---|
| DC high-level input voltage | $V_{IH(DC)}$ | Control, command, address | SSTL_18 | $V_{REF(DC)}$ + 125 | $V_{DDQ}$ + 250 | mV |
| DC low-level input voltage | $V_{IL(DC)}$ | Control, command, address | SSTL_18 | 0 | $V_{REF(DC)}$ - 125 | mV |
| AC high-level input voltage | $V_{IH(AC)}$ | Control, command, address | SSTL_18 | $V_{REF(DC)}$ + 250 | $V_{DD}$ | mV |
| AC low-level input voltage | $V_{IL(AC)}$ | Control, command, address | SSTL_18 | 0 | $V_{REF(DC)}$ - 250 | mV |
| Output high voltage | $V_{OH}$ | Parity output | SSTL_18 | 1.2 | – | V |
| Output low voltage | $V_{OL}$ | Parity output | SSTL_18 | – | 0.5 | V |
| Input current | $I_I$ | All pins | $V_I = V_{DDQ}$ or $V_{SSQ}$ | –5 | 5 | µA |
| Static standby | $I_{DD}$ | All pins | RESET# = $V_{SSQ}$ ($I_O$ = 0) | – | 200 | µA |
| Static operating | $I_{DD}$ | All pins | RESET# = $V_{SSQ}$; $V_I$ = $V_{IH(AC)}$ or $V_{IL(DC)}$ $I_O$ = 0 | – | 80 | mA |
| Dynamic operating (clock tree) | $I_{DDD}$ | N/A | RESET# = $V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $I_O$ = 0; CK and CK# switching 50% duty cycle | – | Varies by manufacturer | µA |
| Dynamic operating (per each input) | $I_{DDD}$ | N/A | RESET# = $V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, $I_O$ = 0; CK and CK# switching 50% duty cycle; One data input switching at $^tCK/2$, 50% duty cycle | – | Varies by manufacturer | µA |
| Input capacitance (per device, per pin) | $C_I$ | All inputs except RESET# | $V_I = V_{REF}$ ±250mV; $V_{DDQ}$ = 1.8V | 2.5 | 3.5 | pF |
| Input capacitance (per device, per pin) | $C_I$ | RESET# | $V_I = V_{DDQ}$ or $V_{SSQ}$ | – | Varies by manufacturer | pF |

## Table 11: PLL Specifications

CUA845 device or JEDEC82-21 equivalent

| Parameter | Symbol | Pins | Condition | Min | Max | Units |
|---|---|---|---|---|---|---|
| DC high-level input voltage | $V_{IH}$ | OE, OS, CK, CK# | LVCMOS | $0.65 \times V_{DD}$ | – | V |
| DC low-level input voltage | $V_{IL}$ | OE, OS, CK, CK# | LVCMOS | – | $0.35 \times V_{DD}$ | V |
| Input voltage (limits) | $V_{IN}$ | | | –0.3 | $V_{DD} + 0.3$ | V |
| Input differential-pair cross voltage | $V_{IX}$ | | Differential input | $(V_{DD}/2) - 0.15$ | $(V_{DD}/2) + 0.15$ | V |
| Input differential voltage | $V_{ID(DC)}$ | | Differential input | 0.3 | $V_{DD} + 0.4$ | V |
| Input differential voltage | $V_{ID(AC)}$ | | Differential input | 600 | $V_{DD} + 0.4$ | V |
| Input current | $I_I$ | OE, OS, FBIN, FBIN# | $V_I = V_{DD}$ or $V_{SS}$ | –10 | 10 | µA |
| | | CK, CK# | $V_I = V_{DD}$ or $V_{SS}$ | –250 | 250 | µA |
| Output disabled current | $I_{ODL}$ | | OE = L, $V_{ODL}$ = 100mV | 100 | – | µA |
| Static supply current | $I_{DDLD}$ | | $C_L$ = 0pf | – | 500 | µA |
| Dynamic supply | $I_{DD}$ | N/A | CK and CK# = 410 MHz, all outputs open (not connected to PCB) | – | 300 | mA |
| Input capacitance | $C_{IN}$ | Each input | $V_I = V_{DD}$ or $V_{SS}$ | 2 | 3 | pF |

## Table 12: PLL Clock Driver Timing Requirements and Switching Characteristics

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Stabilization time | $^tL$ | – | 6.0 | µs |
| Input clock slew rate | slr(i) | 1.0 | 4.0 | V/ns |
| SSC modulation frequency | – | 30 | 33.0 | kHz |
| SSC clock input frequency deviation | – | 0.0 | –0.5 | % |
| PLL loop bandwidth (–3dB from unity gain) | – | 2.0 | – | MHz |

Note: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC Standard JESD82.

# Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I$^2$C bus shared with the SPD EEPROM.

## Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

**Table 13: Temperature Sensor with SPD EEPROM Operating Conditions**

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply voltage | $V_{DDSPD}$ | 3.0 | 3.6 | V |
| Supply current: $V_{DD}$ = 3.3V | $I_{DD}$ | – | 2.0 | mA |
| Input high voltage: Logic 1; SCL, SDA | $V_{IH}$ | 1.45 | $V_{DDSPD}$ + 1 | V |
| Input low voltage: Logic 0; SCL, SDA | $V_{IL}$ | – | 0.55 | V |
| Output low voltage: $I_{OUT}$ = 2.1mA | $V_{OL}$ | – | 0.4 | V |
| Input current | $I_{IN}$ | –5.0 | 5.0 | µA |
| Temperature sensing range | – | –40 | 125 | °C |
| Temperature sensor accuracy (class B) | – | –1.0 | 1.0 | °C |

**Table 14: Temperature Sensor and SPD EEPROM Serial Interface Timing**

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Time bus must be free before a new transition can start | $^tBUF$ | 4.7 | – | µs |
| SDA fall time | $^tF$ | 20 | 300 | ns |
| SDA rise time | $^tR$ | – | 1000 | ns |
| Data hold time | $^tHD{:}DAT$ | 200 | 900 | ns |
| Start condition hold time | $^tH{:}STA$ | 4.0 | – | µs |
| Clock HIGH period | $^tHIGH$ | 4.0 | 50 | µs |
| Clock LOW period | $^tLOW$ | 4.7 | – | µs |
| SCL clock frequency | $^tSCL$ | 10 | 100 | kHz |
| Data setup time | $^tSU{:}DAT$ | 250 | – | ns |
| Start condition setup time | $^tSU{:}STA$ | 4.7 | – | µs |
| Stop condition setup time | $^tSU{:}STO$ | 4.0 | – | µs |

## EVENT# Pin

The temperature sensor also adds the EVENT# pin (open drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register,

respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.
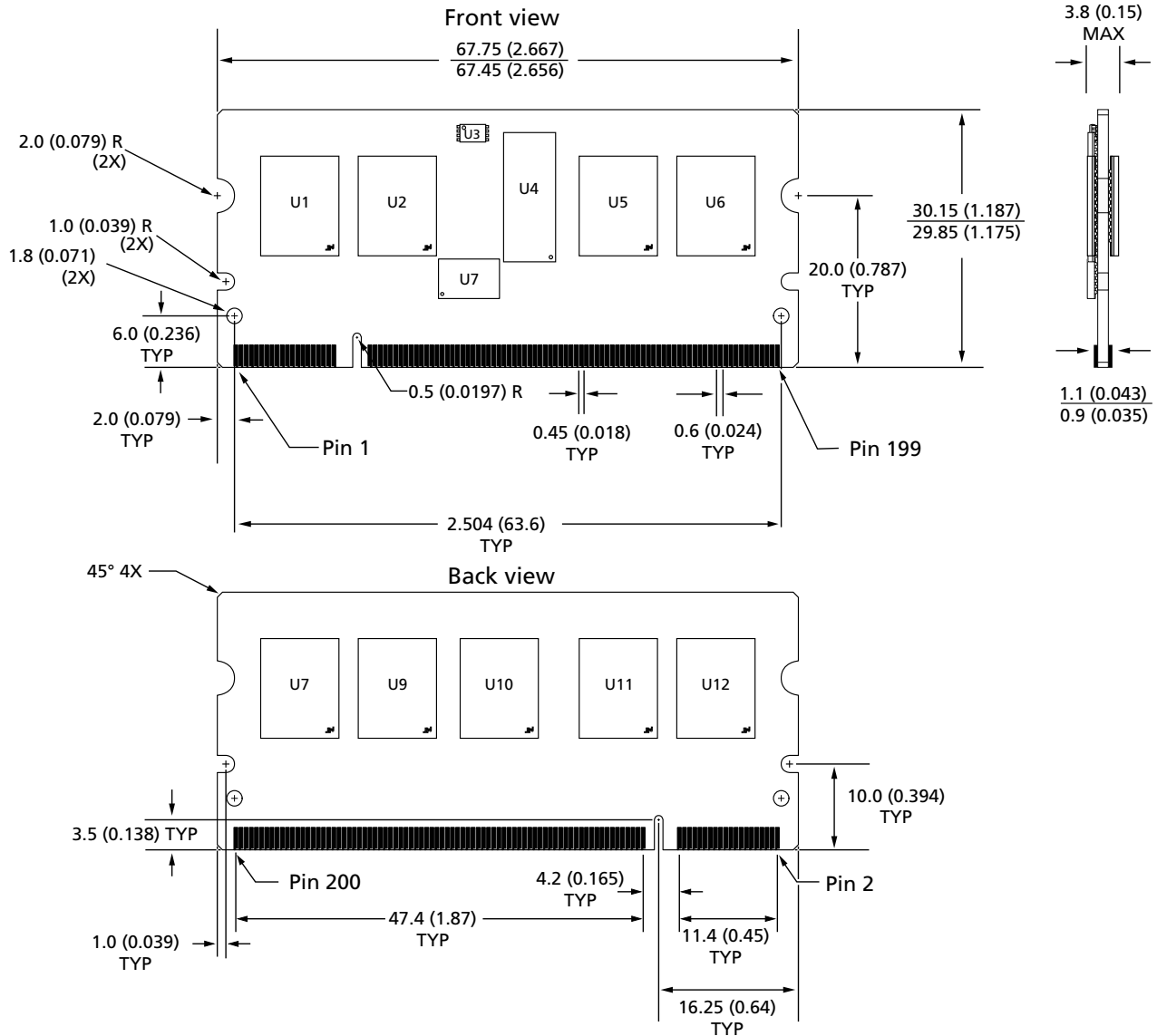
The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and only returns to the logic HIGH state when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

# Module Dimensions

**Figure 3: 200-Pin DDR2 SORDIMM**

Front view

67.75 (2.667)
67.45 (2.656)

3.8 (0.15) MAX

2.0 (0.079) R (2X)

U3

U1 U2 U4 U5 U6

30.15 (1.187)
29.85 (1.175)

1.0 (0.039) R (2X)

1.8 (0.071) (2X)

U7

20.0 (0.787) TYP

6.0 (0.236) TYP

0.5 (0.0197) R

2.0 (0.079) TYP

Pin 1

0.45 (0.018) TYP

0.6 (0.024) TYP

Pin 199

1.1 (0.043)
0.9 (0.035)

2.504 (63.6) TYP

45° 4X

Back view

U7 U9 U10 U11 U12

10.0 (0.394) TYP

3.5 (0.138) TYP

Pin 200

4.2 (0.165) TYP

Pin 2

1.0 (0.039) TYP

47.4 (1.87) TYP

11.4 (0.45) TYP

16.25 (0.64) TYP

Notes:  1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.