GV7704

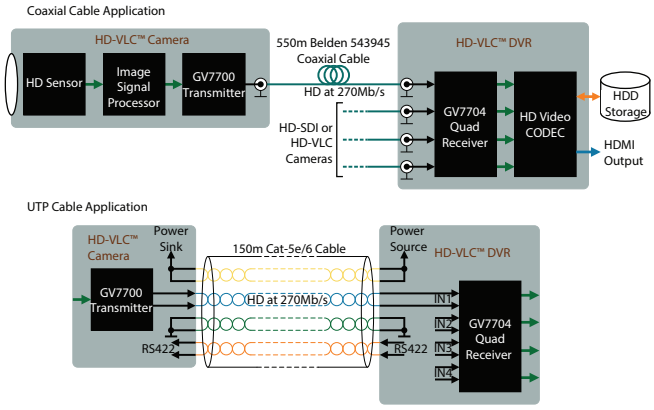
Quad HD-VLC™ Receiver

Key Features

- Quad channel serial digital video receiver for HD and 3G video surveillance and HDcctv applications
- Quad rate operation: 270Mb/s, 540Mb/s, 1.485Gb/s, and 2.97Gb/s
- Supports HDcctv 1.0, HD-SDI (ST 292), 3G-SDI (ST 424), and SD-SDI (ST 259)*
- Four independent receiver channels with high performance cable equalization, with support for 50/75Ω coaxial and twisted pair cable transmission
- Integrated High Definition Visually Lossless CODEC (HD-VLC™) for extended cable reach:
  - HD over 550m of Belden 543945 CCTV coax at 270Mb/s
  - Full HD over 300m of Belden 543945 CCTV coax at 540Mb/s
  - HD over 150m of Cat-5e/6 UTP cable at 270Mb/s
- Serial digital loop-though output per channel
- Integrated audio de-embedder for the extraction of up to 4 channels of I^2S serial digital audio at 32kHz, 44.1kHz and 48kHz sample rates, per video channel
- Supports both 720p and 1080p HD formats:
  - Full HD: 1080p50/59.94/60fps
  - HD: 1080p25/29.97/30fps
  - HD: 720p25/29.97/30/50/59.94/60fps
- Four 8/10-bit BT.1120 compliant output video interfaces, with embedded TRS and external HVF timing outputs
- Automatic independent detection of HD-SDI and HD-VLC video input data streams per channel
- Downstream ancillary data detection and extraction
- Automatic HDcctv Stream ID detection
- 4-wire Gennum Serial Peripheral Interface (GSPI 2.0) for external host command and control
- JTAG test interface
- 1.2V core voltage power supplies
- 1.8V digital I/O power supply
- Small footprint 169-BGA (11mm x 11mm)
- Low power operation, typically 810mW
- Wide operating temperature range: -20°C to + 85°C
- Pb-free and RoHS compliant

Applications

- Digital video recorders (DVR)
- Video servers
- Video multiplexers
- Video PC capture cards
- HDcctv peripherals



Description

The GV7704 is a quad channel serial digital video receiver for High Definition component video. With integrated high performance cable equalizer technology, the GV7704 is capable of receiving compressed video at 270Mb/s or 540Mb/s, or uncompressed at 1.485Gb/s or 2.97Gb/s, over 75Ω coaxial cable, or differentially over a 100Ω twisted pair cable.

The GV7704 integrates the High Definition Visually Lossless CODEC (HD-VLC™) technology, which has been developed specifically to reduce the transmission data rate of HD video over both coaxial and unshielded twisted pair (UTP) cable. This is achieved by encoding the HD video, normally transmitted at a serial data rate of 1.485Gb/s, to the same rate as Standard Definition (SD) video, at 270Mb/s serial data rate.

At 270Mb/s, the effect of cable loss is greatly reduced, resulting in much longer cable transmission. For 75Ω

coaxial cable, cable reach can be extended up to 3x the normal reach when transmitting encoded HD at 270Mb/s. In typical video over coaxial installations, cable distances of up to 550m are possible.

Similarly, a 2.97Gb/s 3G signal can be transmitted at 540Mb/s using HD-VLC.

The GV7704 can also be configured to receive HD and 3G video over UTP cable, such as Cat-5e and Cat-6 cable, when HD-VLC encoded at 270Mb/s and 540Mb/s, respectively.

The device supports the reception of both 8-bit and 10-bit per pixel YCbCr 4:2:2 BT.1120 component digital video. A single 10-bit wide parallel digital video output bus per channel is provided, with associated pixel clock and timing signal outputs. The GV7704 supports direct interfacing of HD video formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE ST 296 for 750-line formats.

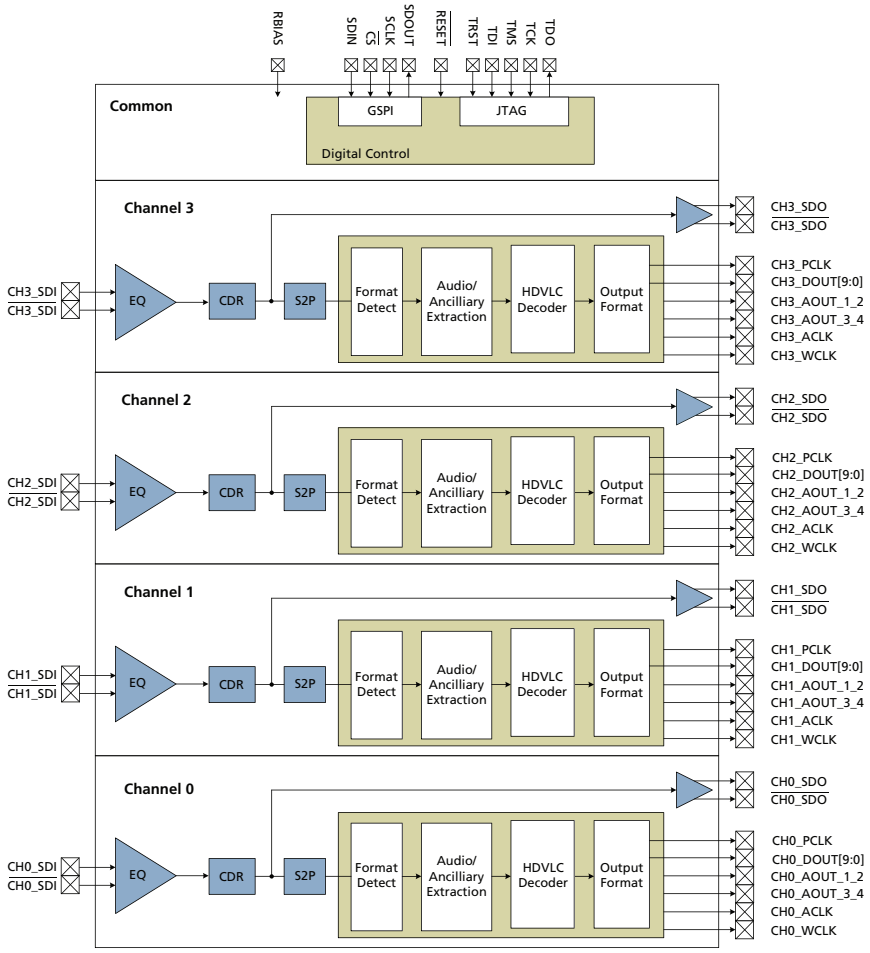
The GV7704 supports the extraction of ancillary data from the horizontal blanking of the input video data stream. Ancillary data packets can be accessed via the GSPI, allowing downstream communication from the video source to sink device. The GV7704 recognizes data packets formatted in compliance with the HDcctv 2.0 communications protocol.

The GV7704 features an audio de-embedding core, which provides the extraction of up to 4 channels of I^2S serial digital audio from the ancillary data space of the input video data stream. The audio de-embedding core supports 32kHz, 44.1kHz, and 48kHz sample rates.

Packaged in a space saving 169 ball 11 x 11mm BGA, the GV7704 is ideal for high density, multi-channel video recorder architectures. Typically requiring only 810mW of power, the device does not require any special heat sinking or air flow, reducing the over cost of HD DVR designs.

**Frame structure with encoded HD only. Does not support SD/D1 video.*

Functional Block Diagram



Revision History

Version	ECO	PCN	Date	Description
5	031801	—	June 2016	Table 2-3: AC Electrical Characteristics VDD18_A, VDD18_D = 1.8V±5% and T_A = -20°C to +85°C unless otherwise stated was updated
4	029083	—	March 2016	Updated to Final Data Sheet. Updated Table 2-3 with added Input Jitter Tolerance and changes to values in Rise/Fall Time, Rise/Fall Time Matching, and Output Total Jitter.
3	027518	—	September 2015	Updated to Preliminary Data Sheet. Updated Section 2.1, Section 2.2, Section 2.3, Section 4., and Figure 6-2. Added Figure 6-3. Various updates throughout document.
2	027065	—	July 2015	Updated cable reach values. Updated Table 2-2 and Table 2-3.
1	024435	—	March 2015	Updated Section 2.2, Section 2.3, Section 5., and Figure 6-1. Added Section 3., Section 4.11 and Section 4.12. Various updates throughout document.
0	021239	—	October 2014	New Document

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1. Pin Out

1.1 GV7704 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	CH3_SDI	$\overline{\text{CH3\_SDI}}$	GND	CH3_SDO	TCK	CH3_WCLK	CH2_WCLK	CH3_HOUT	CH3_PCLK	CH3_DOUT_5	CH3_DOUT_3	CH3_DOUT_1	CH3_DOUT_0
B	GND	GND	VDD18_A	$\overline{\text{CH3\_SDO}}$	TMS	CH3_ACLK	CH2_ACLK	CH3_VOUT	CH3_DOUT_8	CH3_DOUT_6	CH3_DOUT_4	CH3_DOUT_2	CH2_VOUT
C	N/C	N/C	VDD18_A	TDI	TDO	CH3_AOUT_1_2	CH2_AOUT_1_2	CH3_FOUT	CH3_DOUT_9	CH3_DOUT_7	CH2_HOUT	CH2_FOUT	CH2_PCLK
D	CH2_SDI	$\overline{\text{CH2\_SDI}}$	GND	TRST	EXT_FW	CH3_AOUT_3_4	CH2_AOUT_3_4	GND	GND	GND	CH2_DOUT_9	CH2_DOUT_8	CH2_DOUT_7
E	GND	GND	VDD18_A	VDD12_A	RSVD	GND	VDD18_D	VDD18_D	GND	GND	CH2_DOUT_6	CH2_DOUT_5	CH2_DOUT_4
F	CH2_SDO	$\overline{\text{CH2\_SDO}}$	VDD18_A	VDD12_A	GND	VDD12_D	VDD12_D	VDD12_D	VDD18_D	GND	CH2_DOUT_3	CH2_DOUT_2	CH2_DOUT_1
G	GND	GND	VDD18_A	VDD12_A	GND	VDD12_D	VDD12_D	VDD12_D	VDD18_D	GND	GND	CH1_HOUT	CH2_DOUT_0
H	CH1_SDO	$\overline{\text{CH1\_SDO}}$	VDD18_A	VDD12_A	GND	VDD12_D	VDD12_D	VDD12_D	VDD18_D	GND	CH1_VOUT	CH1_FOUT	CH1_PCLK
J	GND	GND	VDD18_A	VDD12_A	GND	GND	VDD18_D	VDD18_D	GND	GND	CH1_DOUT_9	CH1_DOUT_8	CH1_DOUT_7
K	CH1_SDI	$\overline{\text{CH1\_SDI}}$	GND	$\overline{\text{RESET}}$	RSVD	CH0_WCLK	CH1_WCLK	GND	GND	GND	CH1_DOUT_6	CH1_DOUT_5	CH1_DOUT_4
L	RBIAS	VDD18_A	GND	SDIN	SDOUT	CH0_ACLK	CH1_ACLK	CH0_DOUT_2	CH0_DOUT_5	CH0_DOUT_8	CH1_DOUT_3	CH1_DOUT_2	CH1_DOUT_1
M	GND	GND	VDD18_A	$\overline{\text{CH0\_SDO}}$	$\overline{\text{CS}}$	CH0_AOUT_1_2	CH1_AOUT_1_2	CH0_DOUT_1	CH0_DOUT_4	CH0_DOUT_7	CH0_DOUT_9	CH0_VOUT	CH1_DOUT_0
N	CH0_SDI	$\overline{\text{CH0\_SDI}}$	GND	CH0_SDO	SCLK	CH0_AOUT_3_4	CH1_AOUT_3_4	CH0_DOUT_0	CH0_DOUT_3	CH0_DOUT_6	CH0_PCLK	CH0_HOUT	CH0_FOUT

Figure 1-1: GV7704 Pin Out

1.2 Pin Descriptions

Table 1-1: GV7704 Pin Descriptions

Pin Number	Name	Type	Description
Analog High-Speed Inputs			
N1, N2	CH0_SDI, $\overline{\text{CH0\_SDI}}$	Analog High-Speed Input	Differential high-speed data input 0. (75Ω nominal input impedance)
K1, K2	CH1_SDI, $\overline{\text{CH1\_SDI}}$	Analog High-Speed Input	Differential high-speed data input 1. (75Ω nominal input impedance)
D1, D2	CH2_SDI, $\overline{\text{CH2\_SDI}}$	Analog High-Speed Input	Differential high-speed data input 2. (75Ω nominal input impedance)
A1, A2	CH3_SDI, $\overline{\text{CH3\_SDI}}$	Analog High-Speed Input	Differential high-speed data input 3. (75Ω nominal input impedance)
Analog High-Speed Outputs			
N4, M4	CH0_SDO, $\overline{\text{CH0\_SDO}}$	Analog High-Speed Output	Differential high-speed test output 0. (75Ω nominal output impedance)
H1, H2	CH1_SDO, $\overline{\text{CH1\_SDO}}$	Analog High-Speed Output	Differential high-speed test output 1. (75Ω nominal output impedance)
F1, F2	CH2_SDO, $\overline{\text{CH2\_SDO}}$	Analog High-Speed Output	Differential high-speed test output 2. (75Ω nominal output impedance)
A4, B4	CH3_SDO, $\overline{\text{CH3\_SDO}}$	Analog High-Speed Output	Differential high-speed test output 3. (75Ω nominal output impedance)
Analog Bias			
L1	RBIAS	Input/Output	External 10kΩ resistor for bias reference. Connect the resistor to ground.
Digital Video Outputs			
L8, L9, L10, M8, M9, M10, M11, N8, N9, N10	CH0_DOUT_[9:0]	Output	Parallel digital video output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
N12	CH0_HOUT	Output	Horizontal blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
M12	CH0_VOUT	Output	Vertical blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
N13	CH0_FOUT	Output	Frame indication output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
N11	CH0_PCLK	Output	Pixel clock output (148.5MHz or 148.5/1.001 MHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
J[11:13], K[11:13], L[11:13], M13	CH1_DOUT_[9:0]	Output	Parallel digital video output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
G12	CH1_HOUT	Output	Horizontal blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
H11	CH1_VOUT	Output	Vertical blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
H12	CH1_FOUT	Output	Frame indication output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
H13	CH1_PCLK	Output	Pixel clock output (148.5MHz or 148.5/1.001 MHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
D[11:13], E[11:13], F[11:13], G13	CH2_DOUT_[9:0]	Output	Parallel digital video output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
C11	CH2_HOUT	Output	Horizontal blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
B13	CH2_VOUT	Output	Vertical blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
C12	CH2_FOUT	Output	Frame indication output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
C13	CH2_PCLK	Output	Pixel clock output (148.5MHz or 148.5/1.001 MHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
A[10:13], B[9:12], C9, C10	CH3_DOUT_[9:0]	Output	Parallel digital video output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
A8	CH3_HOUT	Output	Horizontal blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
B8	CH3_VOUT	Output	Vertical blanking output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
C8	CH3_FOUT	Output	Frame indication output. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
A9	CH3_PCLK	Output	Pixel clock output (148.5MHz or 148.5/1.001 MHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE). Drive strength may be adjusted using register PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG.
Digital Audio Outputs			
K6	CH0_WCLK	Output	Channel 0 word clock (32kHz, 44.1kHz, or 48kHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
L6	CH0_ACLK	Output	Channel 0 I^2S Audio clock (64 x word clock). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
M6	CH0_AOUT_1_2	Output	Channel 0 I^2S Audio output 1 & 2. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
N6	CH0_AOUT_3_4	Output	Channel 0 I^2S Audio output 3 & 4. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
K7	CH1_WCLK	Output	Channel 1 word clock (32kHz, 44.1kHz, or 48kHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
L7	CH1_ACLK	Output	Channel 1 I^2S Audio clock (64 x word clock). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
M7	CH1_AOUT_1_2	Output	Channel 1 I^2S Audio output 1 & 2. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
N7	CH1_AOUT_3_4	Output	Channel 1 I^2S Audio output 3 & 4. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
A7	CH2_WCLK	Output	Channel 2 word clock (32kHz, 44.1kHz, or 48kHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
B7	CH2_ACLK	Output	Channel 2 I^2S Audio clock (64 x word clock). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
C7	CH2_AOUT_1_2	Output	Channel 2 I^2S Audio output 1 & 2. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
D7	CH2_AOUT_3_4	Output	Channel 2 I^2S Audio output 3 & 4. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
A6	CH3_WCLK	Output	Channel 3 word clock (32kHz, 44.1kHz, or 48kHz). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
B6	CH3_ACLK	Output	Channel 3 I^2S Audio clock (64 x word clock). High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
C6	CH3_AOUT_1_2	Output	Channel 3 I^2S Audio output 1 & 2. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).
D6	CH3_AOUT_3_4	Output	Channel 3 I^2S Audio output 3 & 4. High impedance when signal is not present or user disables the lane (DISABLE_VIDEO_LANE) or user disables audio (DISABLE_AUDIO).

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
JTAG Interface			
B5	TMS	Input	Dedicated JTAG pin – Test Mode Select. This pin is used to control the operation of the JTAG test. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin may be left floating.
C4	TDI	Input	Dedicated JTAG pin – Test data input. This pin is used to shift JTAG test data into the device. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin may be left floating.
C5	TDO	Output	Dedicated JTAG pin – Test data output. This pin is used to shift results from the device.
A5	TCK	Input	Dedicated JTAG pin – Serial data clock signal. This pin is the JTAG clock. Schmitt Trigger Input. If JTAG is not used this pin must be pulled LOW.
D4	TRST	Input	Dedicated JTAG pin – Test Reset. When set LOW, the JTAG logic will be reset. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin must be pulled LOW.
General I/O and Host Interface			
K4	$\overline{\text{RESET}}$	Input	Digital active–low reset input. Used to reset the internal. operating conditions to default settings. Schmitt Trigger Input.
M5	$\overline{\text{CS}}$	Input	Used to initiate and terminate GSPI commands. Active-low.
L4	SDIN	Input	Serial input data, clocked in on the rising edge of SCLK.
L5	SDOUT	Output	Serial data output. Only used in GSPI mode. Clocked out on the falling edge of SCLK. Drive strength may be adjusted using register GSPI_SDOUT_DRV_STRENGTH_SEL_REG.
N5	SCLK	Input	Serial clock. The rising edge is used to latch the SDIN bits and the falling edge to drive SDOUT bits.
D5	EXT_FW	Input	External firmware loading control: When HIGH, indicates to the GV7704 that the host will download firmware to the GV7704. When LOW, indicates to the GV7704 to boot with internal firmware.

Table 1-1: GV7704 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
Supply Pins			
B3, C3, E3, F3, G3, H3, J3, L2, M3	VDD18_A	Power	Analog 1.8V Power Supply. Connect to 1.8V.
E7, E8, F9, G9, H9, J7, J8	VDD18_D	Power	Digital 1.8V Power Supply. Connect to 1.8V.
E4, F4, G4, H4, J4	VDD12_A	Power	Analog 1.2V Power Supply. Connect to 1.2V.
F6, F7, F8, G6, G7, G8, H6, H7, H8	VDD12_D	Power	Digital 1.2V Power Supply. Connect to 1.2V.
A3, B1, B2, D3, D8, D9, D10, E1, E2, E6, E9, E10, F5, F10, G1, G2, G5, G10, G11, H5, H10, J1, J2, J5, J6, J9, J10, K3, K8, K9, K10, L3, M1, M2, N3	GND	Power	Connect to GND.
C1, C2	N/C	—	Do not Connect.
E5, K5	RSVD	—	Connect to GND.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
1.8V I/O and Analog Supply Voltage	–0.5V to +2.5V DC
1.2V Analog and Core Supply Voltage	–0.3V to +1.5V DC
DC Input Voltage, VIN (Not to exceed 2.5V)	–0.5V to (VDD18 + 0.5V)
DC Output Voltage, VOUT (Not to exceed 2.5V)	–0.5V to (VDD18 + 0.5V)
Input ESD Voltage (HBM)	2kV
Input ESD Voltage (CDM)	500V
Storage Temperature Range (T_S)	-50°C to 125°C
Operating Temperature Range (T_A)	-20°C to 85°C
Solder Reflow Temperature (4s)	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC and DC Electrical Characteristics is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

T_A = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
+1.2V Supply Current	I_{1V2}	270Mb/s	—	172	—	mA	
		1.485Gb/s	—	250	—	mA	
+1.8V Supply Current	I_{1V8}	270Mb/s	—	440	—	mA	
		1.485Gb/s	—	456	—	mA	
+1.8V Power Supply Range	VDD18	At the device pin (nominal ±5%)	1.71	1.8	1.89	V	
+1.2V Power Supply Range	VDD12	At the device pin (nominal ±5%)	1.14	1.2	1.26	V	
External RBIAS Resistor	—		9.9	10	10.1	kΩ	
Power Supply Noise Mask +1.2V	—	0-200kHz	—	—	100	mV_{pp}	1
	—	200kHz to 1MHz	—	—	100	mV_{pp}	1
	—	>1MHz	—	—	100	mV_{pp}	1
Power Supply Noise Mask +1.8V	—	0 to 200kHz	—	—	10	mV_{pp}	1
	—	200kHz to 1MHz	—	—	30	mV_{pp}	1
	—	>1MHz	—	—	100	mV_{pp}	1
Total Power Consumption	P_{total}	270Mb/s, All Cable Drivers Enabled	—	950	1030	mW	
		270Mb/s, All Cable Drivers Disabled	—	810	910	mW	
		540Mb/s All Cable Drivers Enabled	—	1065	1180	mW	
		540Mb/s All Cable Drivers Disabled	—	925	1040	mW	
		1.485Gb/s, All Cable Drivers Enabled	—	1070	1160	mW	
		1.485Gb/s, All Cable Drivers Disabled	—	900	1020	mW	
		2.97Gb/s, All Cable Drivers Enabled	—	1200	1370	mW	
		2.97Gb/s, All Cable Drivers Disabled	—	1030	1200	mW	
Digital Logic Input	V_{IL}	Input LOW	-0.3	—	0.63	V	
	V_{IH}	Input HIGH	1.17	—	1.89	V	

Table 2-2: DC Electrical Characteristics (Continued)

T_A = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Digital Logic Output	V_{OL}	Output LOW	—	—	0.45	V	2
	V_{OH}	Output HIGH	1.35	—	—	V	2
	C_{LOAD}	148.5MHz	—	—	12	pF	

Notes:

1. Using recommended supply decoupling. See Figure 6-1: Typical Application Circuit (Part 1).
2. All digital outputs.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VDD18_A, VDD18_D = 1.8V±5% and T_A = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Conditions							
Input Return Loss	—	1MHz to 5MHz	23	—	—	dB	
	—	5MHz to 1.485GHz	12	—	—	dB	
	—	1.485GHz to 2.25GHz	10	—	—	dB	
Input Jitter Tolerance	—	Data rate = 270Mb/s	0.29	—	—	UI	
	—	Data rate = 540Mb/s	0.29	—	—	UI	
	—	Data rate = 1.485Gb/s	0.20	—	—	UI	
	—	Data rate = 2.97Gb/s	0.20	—	—	UI	
Clock and Data Output Conditions							
Output PCLK Clock Frequency	f_{PCLK}		—	148.5 or 148.5/1.001	—	MHz	
SDO Output Impedance	—	75Ω single-ended	66	75	84	Ω	
	—	100Ω differential	88	100	112	Ω	
Output Return loss	—	1MHz to 5MHz	25	—	—	dB	
	—	5MHz to 1.485GHz	6	—	—	dB	
	—	1.485GHz to 2.25GHz	6	—	—	dB	
Amplitude	—	75Ω single-ended	0.36	0.8	0.9	V_{pp}	
	—	100Ω differential	0.36	0.8	0.9	V_{ppd}	

Table 2-3: AC Electrical Characteristics (Continued)

VDD18_A, VDD18_D = 1.8V±5% and T_A = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Rise/Fall Time	—	100Ω differential 20% - 80%	—	85	95	ps	
	—	75Ω single-ended 20% - 80%	—	102	150	ps	
Rise/Fall Time Mismatch	—	20% - 80%	—	—	50	ps	
Overshoot	—		—	—	10	%	
Output Total Jitter	—	Data rate = 270Mb/s	—	0.08	—	UI_{pp}	
	—	Data rate = 540Mb/s	—	0.1	—	UI_{pp}	
	—	Data rate = 1.485Gb/s	—	0.12	—	UI_{pp}	
	—	Data rate = 2.97Gb/s	—	0.17	—	UI_{pp}	
GSPI Digital Control							
GSPI Read/Write Clock Frequency	—		—	—	55	MHz	
Reset Time	—		10	—	—	ms	
Register Access Time	—		—	—	300	ns	

3. Input/Output Circuits

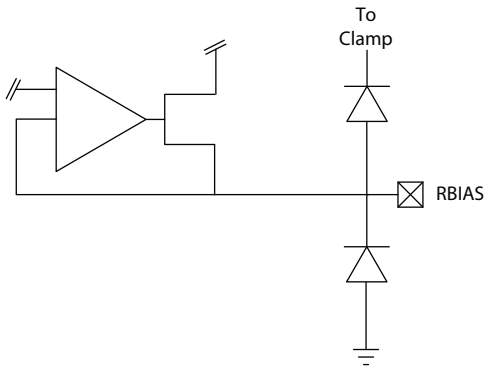


Figure 3-1: RBIAS

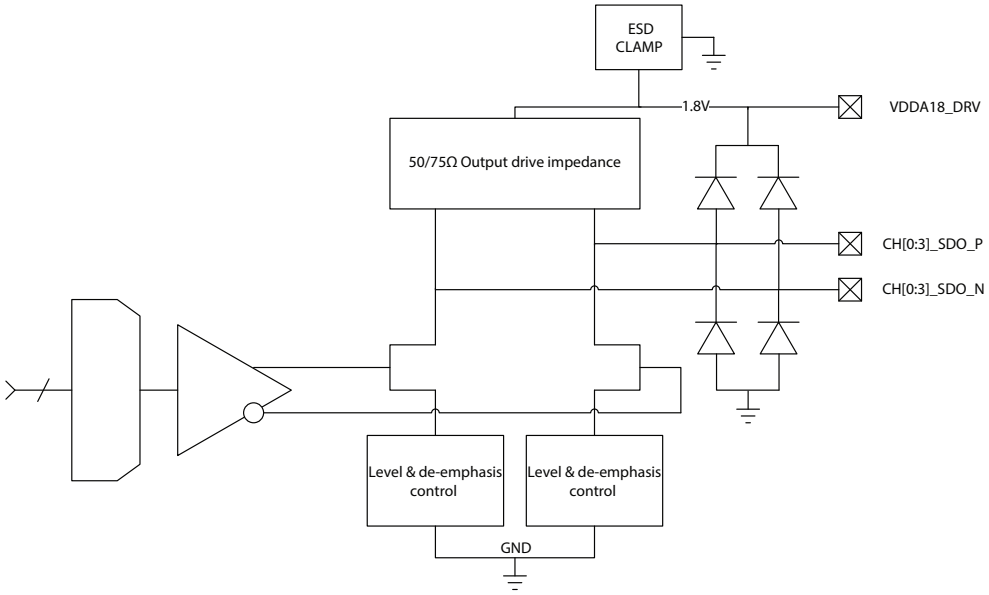


Figure 3-2: Serial Output Driver

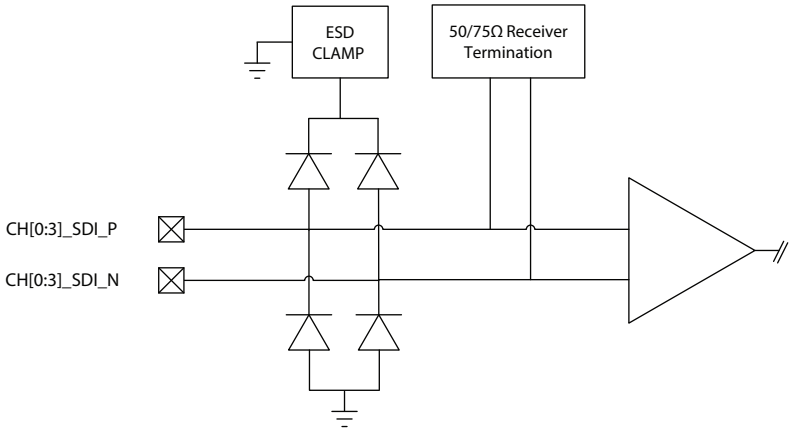


Figure 3-3: Serial Input Receiver

4. Detailed Description

4.1 Functional Overview

The GV7704 is a low cost, quad channel HD-VLC receiver of compressed or uncompressed high-definition video. With integrated cable equalizer technology, the GV7704 is capable of receiving compressed video at 270Mb/s or 540Mb/s, or uncompressed video at 1.485Gb/s or 2.97Gb/s over 75Ω coaxial cable. Compressed signals can also be received differentially over 100Ω twisted pair cable.

The High Definition Visually Lossless CODEC (HD-VLC™) technology is integrated in order to reduce the transmission data rate of HD video over both coaxial and unshielded twisted pair (UTP) cable. This is achieved by encoding the HD-SDI video, normally transmitted at a serial data rate of 1.485Gb/s, to the same rate as Standard Definition (SD-SDI) video, at 270Mb/s serial data rate. This provides extended cable reach for HD video up to 550m over Belden 543945 CCTV coax or 150m over Cat-5e/6 UTP cable. Similarly, 3G-SDI normally transmitted at 2.97Gb/s can be encoded down to 540Mb/s.

The GV7704 features an audio de-embedding core, which provides the extraction of up to 4 channels of I^2S serial digital audio from the ancillary data space of the input video data stream. The audio de-embedding core supports 32kHz, 44.1kHz and 48kHz sample rates.

The device supports the reception of both 8-bit and 10-bit per pixel YCbCr 4:2:2 BT.1120 component digital video. A single 10-bit wide parallel digital video output bus per channel is provided, with associated pixel clock and H/V/F timing signal inputs.

The GV7704 supports the extraction of ancillary data from the horizontal blanking of the input video data stream. Ancillary data packets can be accessed via the GSPI, allowing downstream communication from the video source to sink device. The GV7704 recognizes data packets formatted in compliance with the HDcctv 2.0 communications protocol.

The device includes a 4-wire Gennum Serial Peripheral Interface (GSPI 2.0) for external host command and control. All read or write access to the GV7704 is initiated and terminated by the application host processor. The host interface is provided to allow optional configuration of some of the functions and operating modes of the GV7704.

4.2 Serial Digital Inputs

The GV7704 can accept up to four separate channels of serial digital input signals compliant with ITU-R BT.709, and ITU-R BT.1120-6. The four differential input channels are CH0_SDI/$\overline{\text{CH0\_SDI}}$, CH1_SDI/$\overline{\text{CH1\_SDI}}$, CH2_SDI/$\overline{\text{CH2\_SDI}}$ and CH3_SDI/$\overline{\text{CH3\_SDI}}$.

The GV7704 integrates adaptive 75Ω coaxial cable equalizer technology which is capable of >50dB for HD-VLC encoded input signals and >35dB for HD uncompressed signals.

Table 4-1: Typical Cable Length Performance

Data Rate	Belden 543945 CCTV Coaxial	Cat-5e/6 UTP
HD data @ 1.485Gb/s	150m	N/A
HD-VLC encoded data @ 270Mb/s	550m	150m
3G data @ 2.97Gb/s	50m	N/A
HD-VLC encoded data @ 540Mb/s	300m	75m*

*Theoretical

The Serial Data Signal may be connected to the input pins of any of the four channels in either a differential or single ended configuration. Only AC coupling of the inputs is supported, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

Note: The serial data output should be disabled to achieve maximum SDI cable reach.

4.2.1 Input Termination Selection

Each of the four channels can be individually configured to work in either 50Ω or 75Ω input termination. Please refer to Register Map for details.

4.2.2 Automatic Signal Rate Detection

The device is able to automatically detect the rate of the incoming video signal. There are four data rates which are supported:

- HD-VLC encoded 270Mb/s (including 270x1.001Mb/s)
- HD-VLC encoded 540Mb/s (including 540x1.001Mb/s)
- HD-SDI 1.485Gb/s (including 1.485/1.001Gb/s)
- 3G-SDI 2.97Gb/s (including 2.97/1.001Gb/s)

The detected rate is indicated by bits SD_HDB, THREEG_HDB, and OUT_THREEG_HDB in register GEN_VIDEO_CFG_0_REG which specify whether the incoming signal is HD-VLC encoded (270Mb/s), HD-VLC encoded (540Mb/s), HD (1.485Gb/s), or 3G (2.97Gb/s). Table 4-2 describes how these three bits are used in combination to indicate the input signal rate.

Table 4-2: Input Rate Detection

Rate	GEN_VIDEO_CFG_0_REG		
	SD_HDB	THREEG_HDB	OUT_THREEG_HDB
HD 1.485Gb/s	0	0	0
HD-VLC 270Mb/s	1	0	0
3G 2.97Gb/s	0	1	1
HD-VLC 540MB/s	1	0	1

4.3 Serial Digital Outputs

The GV7704's serial data output pins, SDO and $\overline{\text{SDO}}$, provide complementary outputs, each capable of driving at least 800mV into a 75Ω single-ended load.

Compliance with all requirements defined in Section 4.3.1 through Section 4.3.2 is guaranteed when measured across a 75Ω terminated load at the output of 1m of Belden 543945 cable, including the effects of the BNC and coaxial cable connection, except where otherwise stated.

Figure 4-1 illustrates this requirement.

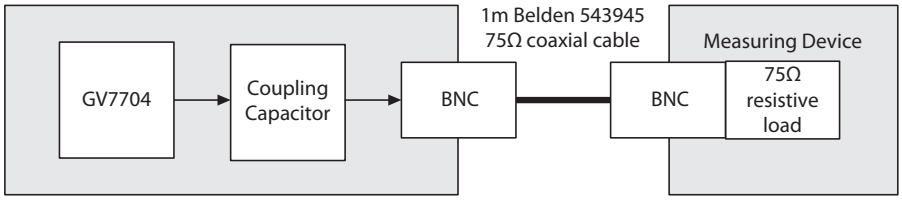


Figure 4-1: BNC and Coaxial Cable Connection

4.3.1 Output Signal Interface Levels

The Serial Data Output signals (SDO and $\overline{\text{SDO}}$ pins), of the device meet the amplitude requirements as defined in ITU-R BT.656 and BT.1120 for an unbalanced generator (single-ended).

These requirements are met across all ambient temperature and power supply operating conditions described in 2. Electrical Characteristics.

4.3.2 Serial Data Output Signal

The device supports two output termination modes (75Ω and 50Ω). The user can program the SDO_50_EN_REG to make that selection, on a per channel basis. Please refer to Register Map for details.

4.3.2.1 Serial Data Output Signal Procedure

To enable the serial data output, the user must do a series of GSPI write transactions. The order is very important and must be followed exactly. The sequence is as shown below:

1. Write 03 to the POWER_UP_DRIVER_REG
2. Write 01 to the P2S_CLK_EN_REG
3. Write 01 to the TX_WORD_CLK_ENABLE_REG
4. Write 01 to the CDR_TX_CLK_EN_REG
5. Write 01 to the P2S_RSTB_REG
6. Write 09 to the DATALANE_FIFO_CTRL_REG
7. Write 08 to the DATALANE_FIFO_CTRL_REG

Please refer to Section 5. Register Map for detailed register information.

Refer to Section 4.10 for GSPI timing requirements.

Note: The serial data output should be disabled to achieve maximum SDI cable reach.

4.4 Video Functionality

4.4.1 Descrambling and Word Alignment

The GV7704 performs NRZI to NRZ decoding and data descrambling according to ITU-R BT.1120, and word aligns the data to TRS sync words.

The GV7704 carries out descrambling and word alignment to enable the detection of TRS sync words. When two consecutive valid TRS words (SAV and EAV), with the same bit alignment have been detected, the device word-aligns the data to the TRS ID words.

Note: Both 8-bit and 10-bit TRS headers are identified by the device.

4.4.2 HD-VLC Decoding

The GV7704 integrates the High Definition Visually Lossless CODEC (HD-VLC) decoder for extended reach video reception. When used in conjunction with the GV7700 HD-VLC transmitter, HD video transmission can be extended significantly over existing HD serial digital video systems. HD-VLC is based on a simple visually lossless implementation of the Dirac compression tool kit (http://diracvideo.org/) The visually lossless decoder is used to reduce the video bandwidth, using a very low latency mode, from a transmission rate of 1.485Gb/s (HD-SDI) to 270Mb/s (SD-SDI).

At a data rate of 270Mb/s, the serial digital encoded HD video can be transmitted over longer runs of coaxial cable. Table 4-3 below shows a comparison of cable distances between HD video transmission at 1.485Gb/s and HD-VLC encoded at 270Mb/s for various common coaxial cable types.

Table 4-3: Cable Reach for Various Cable Types (In Metres)

Cable Type	HD-VLC: 270Mb/s (m)	HD-VLC: 540Mb/s (m)	HD-SDI: 1.485Gb/s (m)	3G-SDI: 2.97Gb/s (m)
Belden 1694A / Canare L-4.5CHD	710	400	230	80
Belden 543945	550	300	150	50
KW-Link SYV 75-5	500	275	140	50
Canare L-3C2V	300	160	95	30
KW-Link SYV 75-3	300	160	85	30

Note: These values apply for new, properly terminated cables. Actual performance may vary.

Note 1: Longer cable reach performance at both 3G and 540M is possible; up to 100m at 3G and 400m at 540M can be achieved using Belden 543945. However, GV7704 lock times can increase significantly at these cable ranges, and may exceed the lock time requirements of the intended application.

Note 2: The serial data output should be disabled to achieve maximum SDI cable reach.

After transmission over the coaxial cable, the 270Mb/s or 540Mb/s serial data is recovered using the GV7704 and the data is decoded back into the native HD or 3G format. The encoding and decoding process has a total latency of 12-14 HD/3G lines which makes the CODEC ideal for low latency real-time applications. Table 4-4 below shows the total encode/decode latency through the GV7704 and the GV7700.

Table 4-4: Encode and Decode Total Latency (GV7704 + GV7700)

Video Format	Delay (µs)	Delay (HD/3G Lines)
1080p25	422.2	11.9
1080p29.97	368.8	12.4
1080p30	368.4	12.4
1080p50	211.1	11.9
1080p59.94	184.4	12.4
1080p60	184.2	12.4
720p25	635.1	11.9
720p29.97	546.6	12.2
720p30	546.6	12.2
720p50	368.6	13.8
720p59.94	324.2	14.5
720p60	324.2	14.5

The 270Mb/s data stream uses the same timing and frame structure as Standard Definition SDI (SD-SDI), and can be monitored using standard SD-SDI test equipment to check signal integrity. However, the data contained within the active picture area of the

SD-SDI stream contains only encoded HD packets. The HD video content can only be viewed after the HD-VLC decoding process.

When the GV7704 is HD-VLC encoding video formats at “true” 30 or 60 frames per second, the 270Mb/s (540Mb/s) serial data input will actually be incoming at a rate of 270x1.001Mb/s (540x1.001Mb/s). This multiplication factor is to account for the fractional increase in the original HD video frame rate. For all other HD frame rates, the incoming serial data will be exactly 270Mb/s.

4.4.3 High Definition Output Video Format

ITU-R BT.1120 describes the serial and parallel format for 1080-line interlaced and progressive digital video. The field/frame blanking period (V), the line blanking period (H), and the field identification (F), are embedded as digital timing codes (TRS) within the video. After deserialization, a single 10-bit bus carrying the C'B, Y', C'R, Y', etc. data pattern is output on the 10-bit parallel data interface, operating at a pixel clock rate of 148.5MHz or 148.5/1.001MHz.

For 3G formats the parallel interface uses a DDR pixel clock at 148.5MHz or 148.5/1.001MHz.

The following figures show horizontal and vertical timing for 1080-line interlaced systems.

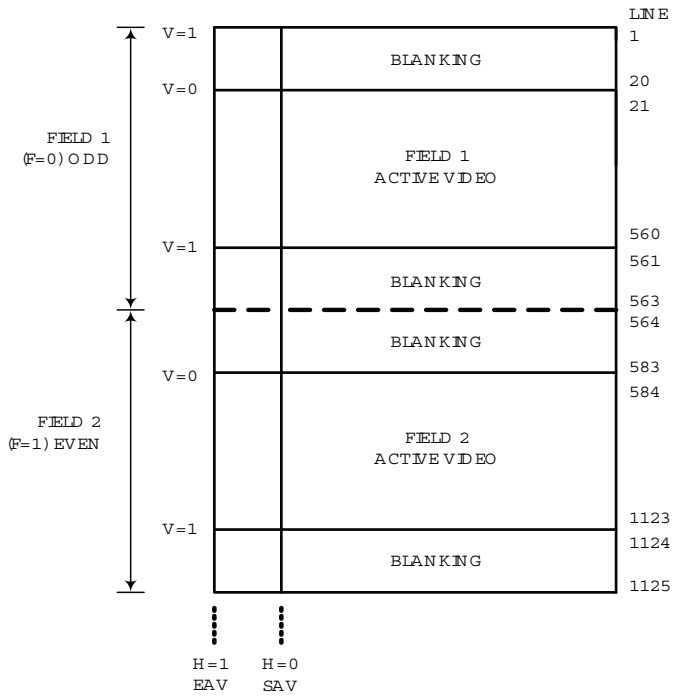


Figure 4-2: Field Timing Relationship for 1080-line Interlaced Systems

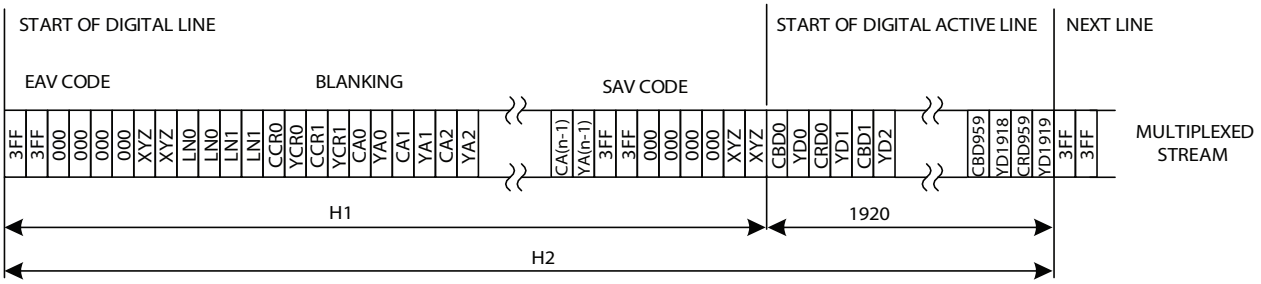


Figure 4-3: Multiplexed Luma and Chroma Over One Video Line - 1080i

Table 4-5: 1080-line Interlaced Horizontal Timing

Interlaced	60 or 60/1.001 Hz	50Hz
H1	560	1440
H2	4400	5280

4.4.3.1 High Definition 1080p Output Formats

ITU-R BT.1120 also includes progressive scan formats with 1080 active lines, with $Y'C'_BC'_R$ 4:2:2 sampling at pixel rates of 74.25MHz or 74.25/1.001 MHz. The following diagrams show horizontal and vertical timing for 1080-line progressive systems. The GV7704 provides a 10-bit multiplexed output interface, doubling the pixel clock output rate to 148.5MHz or 148.5/1.001 MHz.

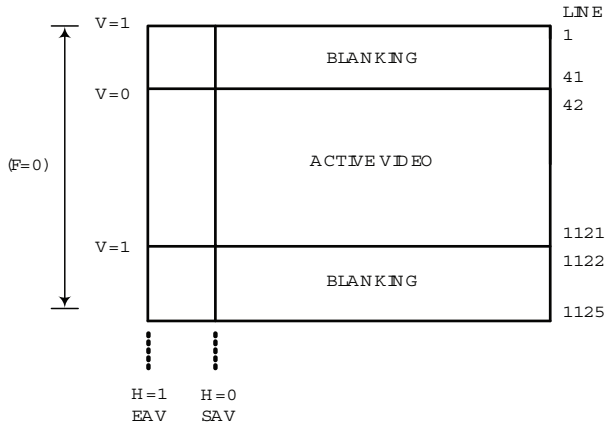


Figure 4-4: Frame Timing Relationship For 1080-line Progressive Systems

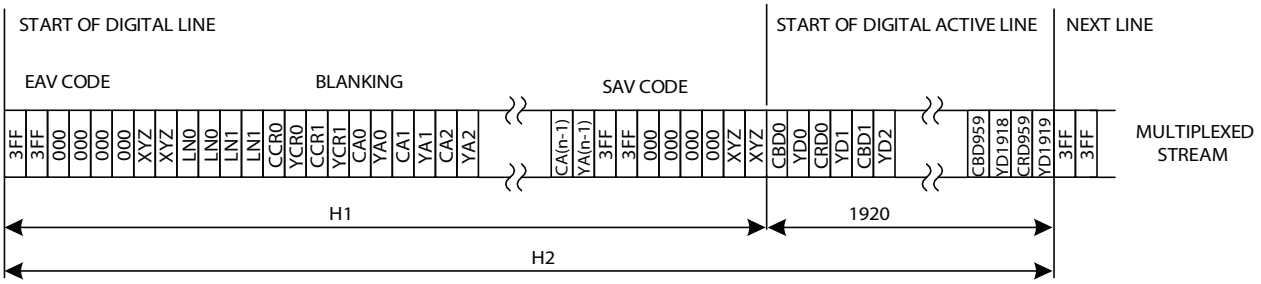


Figure 4-5: Multiplexed Luma and Chroma Over One Video Line - 1080p

Table 4-6: 1080-line Progressive Horizontal Timing

Progressive	30Hz, 30/1.001Hz, 60Hz, 60/1.001Hz	25Hz or 50Hz	24Hz or 24/1.001Hz
H1	560	1440	1660
H2	4400	5280	5500

4.4.3.2 High Definition 720p Output Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for progressive scan 720-line HD image formats. SMPTE ST 296-2001 specifies the representation for 720p digital $Y'C'_BC'_R$ 4:2:2 signals at pixel rates of 74.25MHz or 74.25/1.001 MHz. The GV7704 provides a 10-bit multiplexed output interface, doubling the pixel clock output rate to 148.5MHz or 148.5/1.001 MHz.

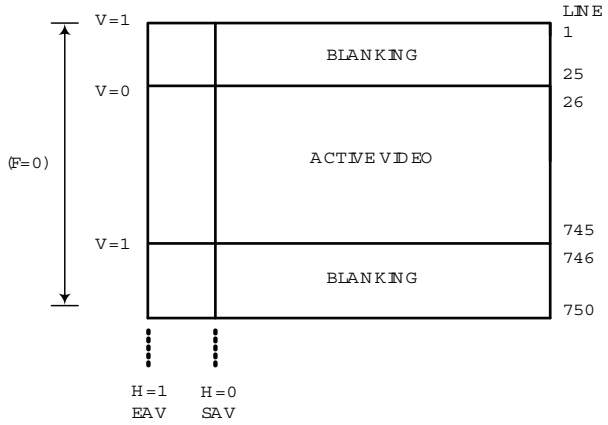


Figure 4-6: 720p Digital Vertical Timing

The frame rate determines the horizontal timing, which is shown in Table 4-7.

Table 4-7: 720p Horizontal Timing

Frame Rate	H = 1 Sample Number	H = 0 Sample Number	Total Samples Per Line
25	2560	0	7920
30 or 30/1.001	2560	0	6600
50	2560	0	3960
60 or 60/1.001	2560	0	3300

4.4.3.3 BT.656 Video Output Timing Mode

By default, the 10-bit parallel video output will contain two embedded TRS words, as defined in ITU-R BT.1120. Some commercially available CODEC devices cannot detect the presence of the double TRS in the HD video stream, and require that the 8/10-bit HD video contain only one TRS word, as per the ITU-R BT.656 Standard Definition format. When the BT656_ENABLE bit is HIGH, the GV7704 will re-format the parallel video

output to conform with BT.656 embedded TRS. The device will replace all data words from the second TRS, line number and line CRC with blanking values, as shown in Figure 4-7. Note that when BT.656 output mode is enabled, any embedded ancillary data in the horizontal balking will remain unchanged, and will not be contiguous from the EAV. This is shown in Figure 4-8 below.

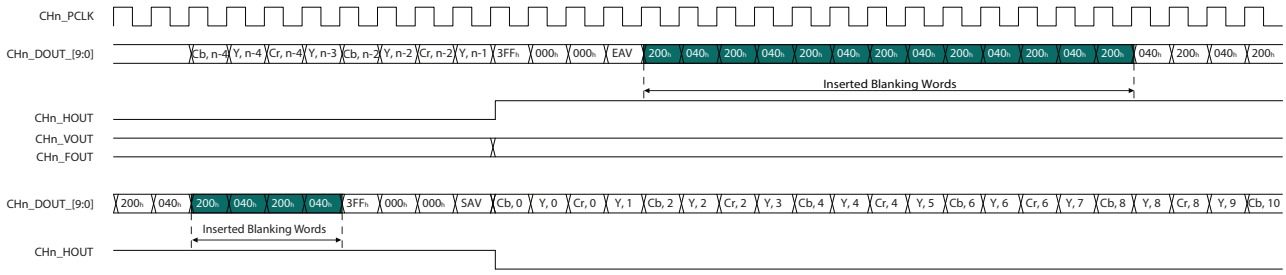


Figure 4-7: BT.656 Video Output Timing

Figure 4-8: Ancillary Data in BT.656 Video Output Timing Mode

4.4.3.4 3G-SDI 1080p Input Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for 3G-SDI image formats in ST 425. The GV7700 supports 1080p50/60 Y'C'BC'R 4:2:2 8/10 bit. For 3G formats the parallel interface uses a DDR pixel clock at 148.5MHz or 148.5/1.001MHz.

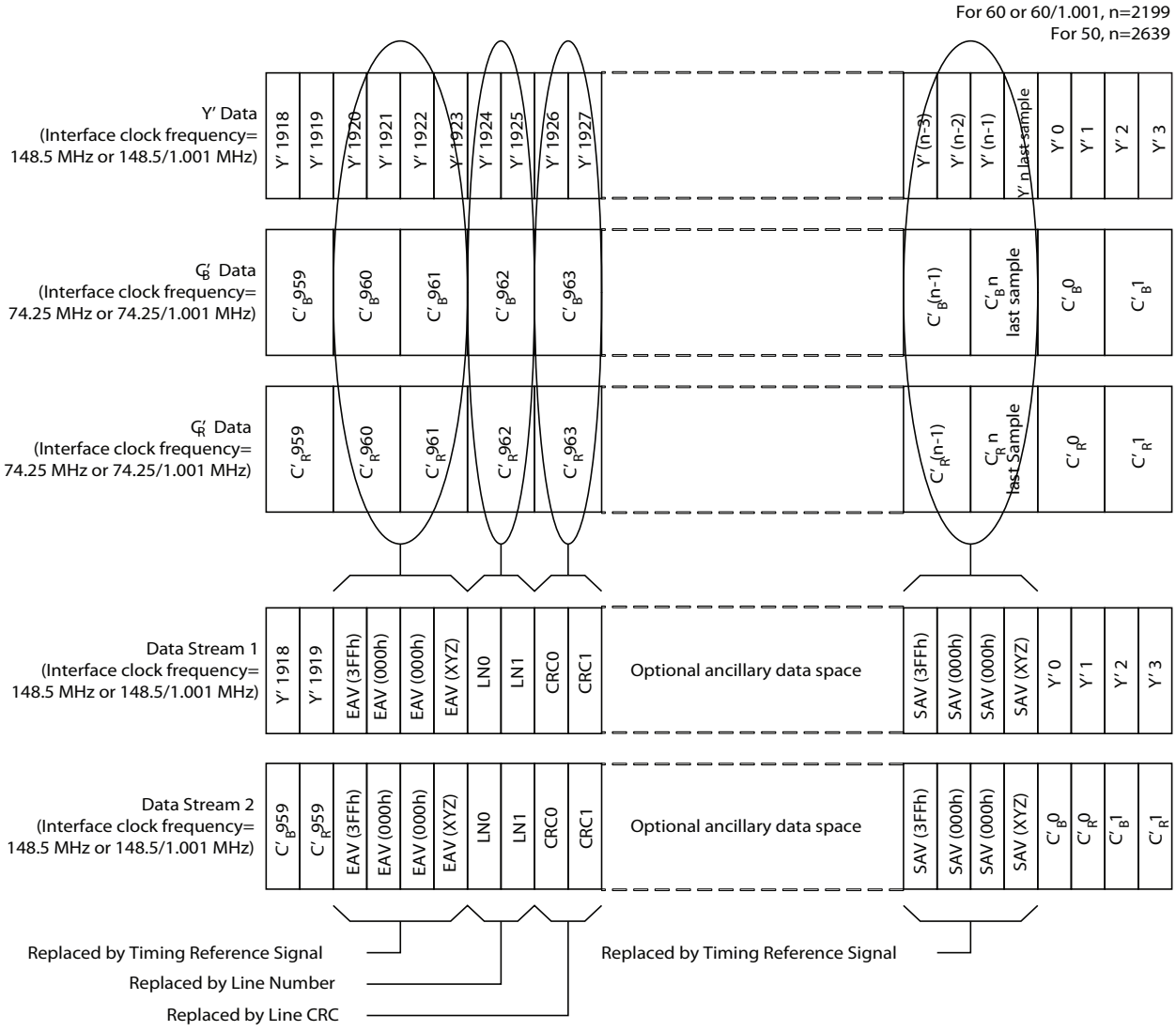


Figure 4-9: 20-bit Mapping Structure for 1920 x 1080 50/60Hz Progressive 4:2:2 ($Y'C'_BC'_R$) 8/10-bit Signals

Table 4-8: 1080p $Y'C'_BC'_R$ 4:2:0 & 4:2:2 10-bit Bit Structure Mapping

Data Stream	Bit Number									
	9	8	7	6	5	4	3	2	1	0
DS1	$Y'[9:0]$									
DS2	$C'_BC'_R[9:0]$									

Note: For 8-bit systems, the data should be justified to the most significant bit ($Y'9$ and $C'_BC'_R9$), with the two least significant bits ($Y'[1:0]$ and $C'_BC'_R[1:0]$) set to zero.

4.5 Parallel Video Data Outputs CHn_DOUT_[9:0]

A 10-bit video output bus is provided for each received video channel. For HD formats the parallel data outputs are aligned to the rising edge of PCLK. For 3G formats the parallel data outputs are aligned to both rising and falling edge of PCLK. Each output provides a 10-bit multiplexed ITU-R BT.1120 compliant video bus with embedded TRS. The drive strength of the parallel video output pins (PCLK, HOUT, VOUT, FOUT, DOUT[9:0]) can be adjusted using the PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL bit. The device uses the low drive strength setting by default. For PCB trace longer than 6 inches the high drive strength setting should be used.

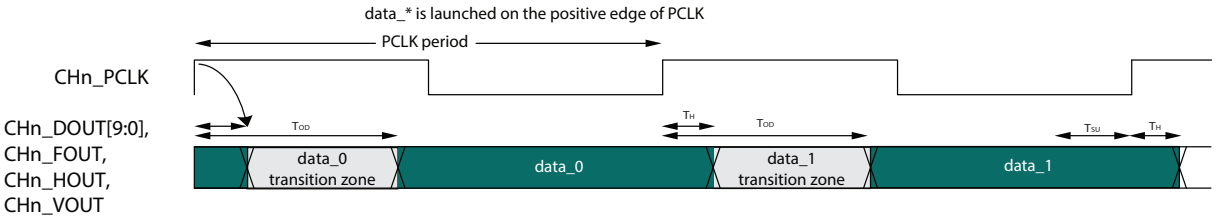


Figure 4-10: SDR Parallel Video Output Timing Diagram

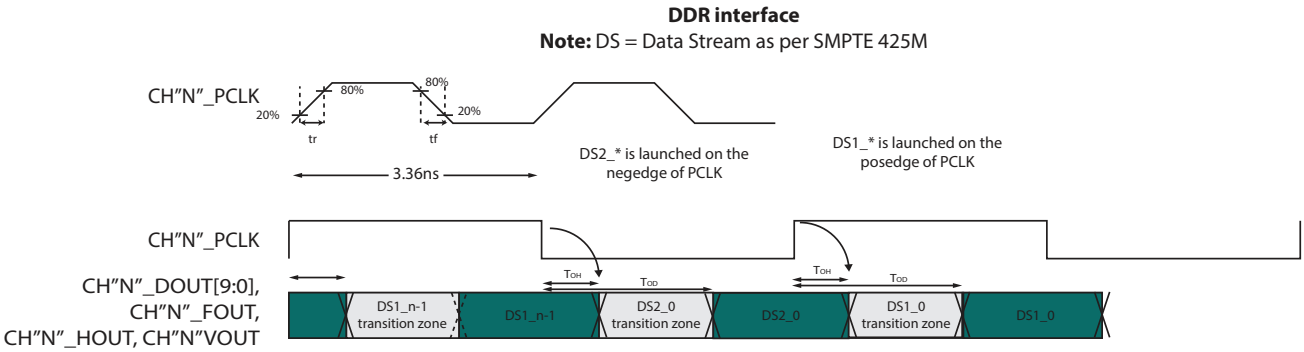


Figure 4-11: DDR Parallel Video Output Timing Diagram

Table 4-9: Digital Output Specifications

Digital Parallel Video Output Interface	Symbol	Conditions	Min	Typ	Max	Units	Notes
Parallel Clock Frequency	f_{PCLK}	—	—	148.5	—	MHz	—
Parallel Clock Duty Cycle	DC_{PCLK}	—	40	—	60	%	
Output Data Hold Time	t_{OH}	1.89V operation, 6pF C_{LOAD}, 0°C	0.4	—	—	ns	—
Output Data Delay Time	t_{OD}	1.71V operation, 6pF C_{LOAD}, 85°C	—	—	2.66	ns	—

Table 4-9: Digital Output Specifications (Continued)

Digital Parallel Video Output Interface	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output Data Rise/Fall Time	t_r/t_f	1.89V operation, 6 pF C_{LOAD}, 0°C	—	—	0.4	ns	—
		1.71V operation, 15 pF C_{LOAD}, 85°C	—	—	1.4	ns	—

4.6 PCLK Control

The CLOCKS_CFG_CFG_1_REG register can be used to control the phase of the output PCLK. PCLK_SELECT bits shift the phase of the clock according to Table 4-10. The clock can be inverted using the PCLK_INVERT bit.

Table 4-10: PCLK Control

PCLK_SELECT[2:1]	PCLK Phase Adjustment for HD Formats	PCLK Phase Adjustment for 3G Formats
0	0	0
1	90	90
2	180	N/A
3	270	N/A

4.7 Stream ID Packet Extraction

The GV7704 will automatically detect and extract HDcctv Stream ID packets from all four video channels. Each channel's 6 byte packet can be read from the host interface through the bits EXTRACT_STREAM_ID_BYTE[1:6] located in registers EXTRACT_STREAM_ID_REG[1:6] respectively. There are independent registers for each of the four channels.

When the GV7704 is decoding HD-VLC streams, the device will automatically re-insert the correct Stream ID in the HD parallel video output. Only bytes 1 and 2 of the Stream ID packet will be updated, with all other bytes set to all zero. The re-inserted byte 1 and 2 data can be read from registers INS_ID_BYTE1_REG and INS_ID_BYTE_2_REG. Bytes 1 and 2 can be programmed from bits INS_ID_BYTE[1:2] located in registers INS_ID_BYTE_REG[1:2] respectively.

Byte 1 of the Stream ID packet is interpreted according to Table 4-11 below.

Table 4-11: Stream ID Packet Extraction Byte 1

Input Video Standard	HD-VLC Encoding	Byte 1 Value	Original Video Standard
720p25	OFF	14h	720p25
625i25	ON	94h	720p25
720p29.97	OFF	12h	720p29.97
525i29.97	ON	92h	720p29.97
720p30	OFF	11h	720p30
525i30	ON	91h	720p30
1080i50	OFF	E3h	1080i50
720p50	OFF	13h	720p50
625i25	ON	93h	720p50
1080i59.94	OFF	E2h	1080i59.94
720p59.94	OFF	16h	720p59.94
525i29.97	ON	96h	720p59.94
1080i60	OFF	E1h	1080i60
720p60	OFF	15h	720p60
525i30	ON	95h	720p60
1080p25	OFF	23h	1080p25
625i25	ON	A3h	1080p25
1080p29.97	OFF	22h	1080p29.97
525i29.97	ON	A2h	1080p29.97
1080p30	OFF	21h	1080p30
525i30	ON	A1h	1080p30
625i25	ON	F3h	1080i50
525i29.97	ON	F2h	1080i59.94
525i30	ON	F1h	1080i60
1080p50	OFF	26h	1080p50
625i50	ON	A6h	1080p50
1080p59.94	OFF	25h	1080p59.94
525i59.94	ON	A5h	1080p59.94
1080p60	OFF	24h	1080p60
525i60	ON	A4h	1080p60

Note: When the GV7704 is receiving HD-VLC encoded HD video formats at "true" 30 or 60 frames per second, the 270Mb/s serial data rate will be at 270 x 1.001 Mb/s. This multiplication factor is to account for the fractional increase in the original HD video frame rate. For all other HD frame rates, the HD-VLC encoded serial data rate will be exactly 270Mb/s.

4.8 Ancillary Data Extraction

The GV7704 is capable of extracting ancillary data packets, with the type of packet specified by the user on a programmable 10 bit DID. The 2 MSBs of the DID are written to ANC_PACKET_DID_9_8 in register ANC_PACKET_DID_9_8_REG, and the next 8 bits are written to ANC_PACKET_DID_7_0 in register ANC_PACKET_DID_7_0_REG.

Up to 16 User Data Words can be extracted per ancillary data packet. The chip will extract the DID-SDID/DBN-DC-UDWs-CS bytes, and they are available in 10-bit pairs (ANC_PACKET_UD W0_9_8, ANC_PACKET_UDW0_7_0) through to (ANC_PACKET_UD W15_9_8, ANC_PACKET_UDW15_7_0).

The GV7704 looks for packets in the horizontal blanking region of a digital video signal. The vertical blanking region is used by the HD-VLC encoder of the GV7000 which inserts compression coefficients that cannot be overwritten. The payload of the ancillary data packet can be used to carry user-defined or proprietary data, which can be sent between an Aviia transmitter and receiver.

The ancillary data packet is formatted according to the Figure 4-12 below. The packet must always begin with the Ancillary Data Flag (ADF), defined as the following 10-bit word sequence: 000_h, $3FF_h$, $3FF_h$.
The next data word is the 8-bit Data ID (DID), used to define the contents of the packet. For example, a unique DID can be used to denote alarm data, with another DID to denote status data.

After the DID, there are two possible options, as shown in Figure 4-12.

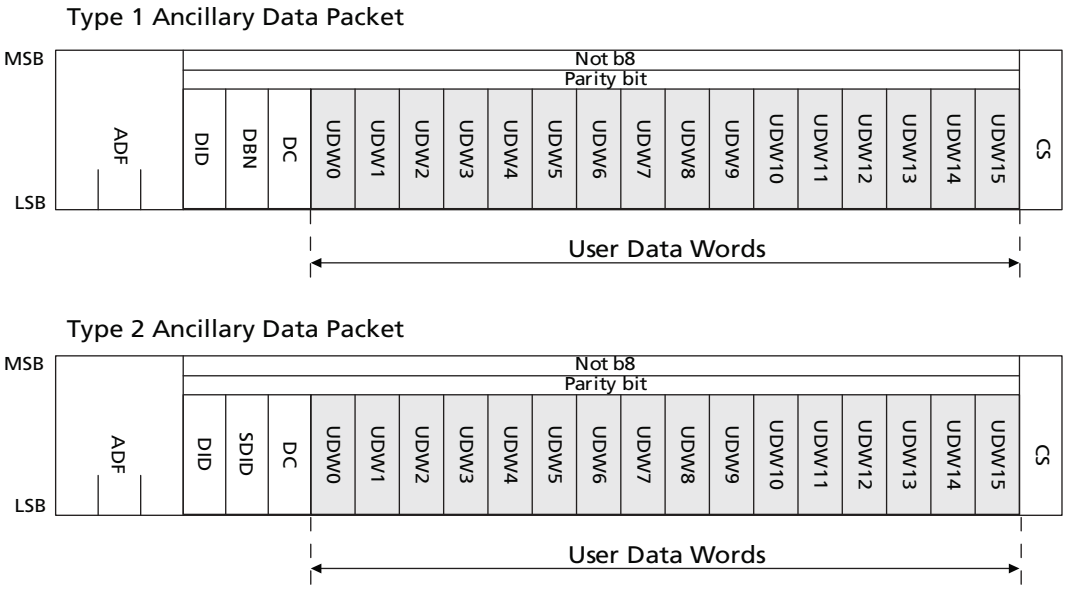


Figure 4-12: Ancillary Data Packets

A Type 1 packet defines an 8-bit Data Block Number (DBN) sequence, used to distinguish successive packets with the same DID. The DBN simply increments with each packet of the same DID, between 0 and 15.

For a Type 2 packet, an 8-bit Secondary Data ID (SDID) word is defined, which can be used to denote variants of payloads with the same DID. For example, packets with a DID to denote error data may distinguish different error types using unique SDID's.

After the DBN or SDID, the next data word is the 8-bit Data Count (DC). This word must be set to the number of user data words (UDW) that follow the DC, and must not exceed 16 (maximum payload size).

The final word of the ancillary data packet is the 9-bit Checksum (CS). The CS value must be equal to the nine least significant bits of the sum of the nine least significant bits of the DID, the DBN or the SDID, the DC and all user data words (UDW) in the packet.

For HD video formats, ancillary data packets are only extracted from the Luma channel.

4.9 Audio Extraction

The GV7704 will de-embed audio from both HD and HD-VLC encoded data. The GV7704 can extract up to four channels of serial digital audio at an audio sampling rate of 32kHz, 44.1kHz, or 48kHz. By default, audio extraction for each channel is enabled, and it can be disabled on any channel by setting DISABLE_AUDIO to 01 in the AUDIO_CTRL_OVERRRIDE_REG register from the host interface.

By default, the device will process audio at a sampling rate of 48kHz. When using a GV7700 to GV7704 chip set, audio sampled at 44.1kHz and 32kHz will be automatically detected by the GV7704. The GV7704 reads the Stream ID packet byte 3 to determine the audio sampling frequency.

When receiving from a signal not transmitted by the GV7700, the audio sampling rate must be manually specified if different than 48kHz, first by setting AUDIO_SAMP_FREQ_MANUAL_MODE to 1, and then by specifying the sampling frequency through AUDIO_SAMP_FREQ. Refer to Table 4-12 below.

Table 4-12: Register Settings for Manual Audio Sampling Frequency

AUDIO_SAMP_FREQ	Sampling Frequency
00 (default)	48khz
01	44.1kHz
10	32kHz
11	Reserved

The device will continuously look for the programmable audio group DID and updates the audio packets present on every rising edge of the vertical blanking interval. If several audio groups are present in the video signal, the device will extract the lower Audio Group number (ex: Audio Group 2, Audio Group 8: Audio Group 2 will be extracted). As such, the programmable audio group DID is offered to the user as a method of selecting

the audio group of his choice for extraction or for specifying an audio DID that would be different from the 8 HD audio group DIDs specified in the SMPTE standards.

The audio packet format is SMPTE ST 299-1, regardless of the input signal rate (270Mb/s or 1.485Gb/s). The GV7704 will compute ECC (Error Correcting Codes) and compare them to the ECC embedded in the audio packets, and it will correct errors wherever possible as well as report any errors found. Error correction can be disabled by setting DISABLE_ECC to 01 in the AUD_EXT_CONFIG_REG register, and the audio samples will be bypassed as found in the packets.

The audio samples will be buffered and output on the four I^2S channels via CHn_ACLK, CHn_WCLK, CHn_AIN_1_2, and CHn_AIN_3_4 pins. They will be formatted according to the standard I^2S bus specifications, and the timing for this interface is shown in Figure 4-13 below.

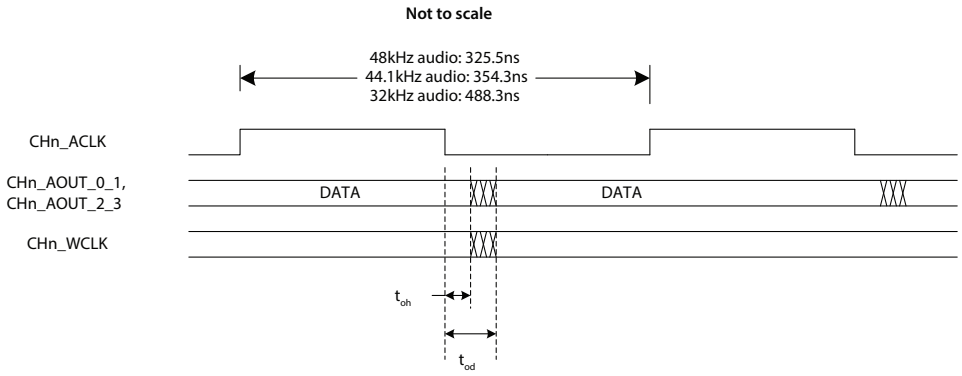


Figure 4-13: ACLK to Audio Data and WCLK Signal Output Timing

Table 4-13: GV7704 Serial Audio Data Outputs - AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Data Hold Time	t_{OH}	50% levels; 1.8V operation	1.5	—	—	ns
Output Data Delay Time	t_{OD}		—	—	7.0	ns

4.9.1 Serial I^2S Audio Data Format

The GV7704 supports the I^2S serial audio data format, as shown in Figure 4-14 below.

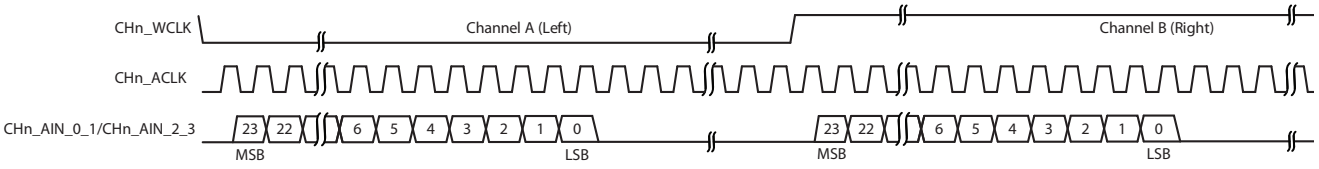


Figure 4-14: I^2S Audio Output Format

4.9.2 Audio Mute

The GV7704 can mute either pair of output audio channels using 2 host interface control bits for each video lane. The bits can mute channels 0 & 1 or channels 2 & 3. Channels 0 & 1 can be muted by asserting the MUTE 0_1 bit in the AUD_EXT_CONFIG_REG for any of the four video lanes. Channels 2 & 3 can be muted by asserting the MUTE_2_3 bit in the AUD_EXT_CONFIG_REG for any of the four video lanes. See Table 4-14.

By default, the 4 channels will not be muted.

Table 4-14: Audio Mute Controls

Address	Register	Parameter	Description
Channel 0: $488D_h$ Channel 1: $548D_h$ Channel 2: $608D_h$ Channel 3: $6C8D_h$	AUD_EXT_CONFIG_REG	MUTE_0_1	HIGH = Channels 0 & 1 are muted LOW = Channels 0 & 1 are not muted
		MUTE_2_3	HIGH = Channels 2 & 3 are muted LOW = Channels 2 & 3 are not muted

4.10 GSPI Host Interface

The GV7704 is controlled via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (SDIN pin), serial data output signal (SDOUT pin), an active-low chip select ($\overline{CS}$ pin) and a burst clock (SCLK pin).

The GV7704 is a slave device, so the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

4.10.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-low signal provided by the host processor to the GV7704.

The HIGH-to-LOW transition of this pin marks the start of serial communication to the GV7704.

The LOW-to-HIGH transition of this pin marks the end of serial communication to the GV7704.

4.10.2 SDIN Pin

The SDIN pin is the GSPI serial data input pin of the GV7704.

The 16-bit Command and Data Words from the host processor are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is LOW.

4.10.3 SDOUT Pin

The SDOUT pin is the GSPI serial data output of the GV7704.

All data transfers out of the GV7704 to the host processor occur from this pin.

By default at power up or after system reset, the SDOUT pin provides a non-clocked path directly from the SDIN pin, only when the $\overline{CS}$ pin is LOW, except during the GSPI Data Word portion for read operations to the device. When the $\overline{CS}$ pin is HIGH, the SDOUT pin will be in a high-impedance state.

For read operations, the SDOUT pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor on the subsequent SCLK rising edge. The current drive strength of the SDOUT pin can be adjusted using the GSPI_SDOUT_DRV_STRENGTH_SEL bit.

4.10.4 SCLK Pin

The SCLK pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GV7704 SDIN pin on the rising edge of SCLK. Serial data is clocked out of the device from the SDOUT pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{CS}$ is HIGH.

4.10.5 Command Word Description

All GSPI accesses are a minimum of 48 bits in length (a 16-bit Command Word, a 16-bit Extended Address field, and a 16-bit Data Word) and the start of each access is indicated by the HIGH-to-LOW transition of the chip select ($\overline{CS}$) pin of the GV7704.

The format of the Command Word and Data Words are shown in Figure 4-15.

Data received immediately following this HIGH-to-LOW transition will be interpreted as a new Command Word.

4.10.5.1 R/$\overline{W}$ bit - B15 Command Word

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated and data is written to the register specified by the ADDRESS field of the Command Word.

4.10.5.2 BROADCAST ALL - B14 Command Word

This bit must always be set to 0.

4.10.5.3 EMEM - B13 Command Word

This bit must always be set to 1.

4.10.5.4 AUTOINC - B12 Command Word

When AUTOINC is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a LOW-to-HIGH transition on the $\overline{CS}$ pin is detected.

When AUTOINC is set to 0, single read or write access is required. Auto-Increment write must not be used to update values in HOST_CONFIG.

4.10.5.5 UNIT ADDRESS - B11:B5 Command Word

The 7 bits of the UNIT ADDRESS field of the Command Word should always be set to 0.

4.10.5.6 ADDRESS - B4:B0 Command Word, B15:B0 Extended Address

The Address Word consists of bits [4:0] of the Command Word, plus another 16 bits [15:0] from the Extended Address Word. The total Command and Data Word format, including the Extended Address, is shown in Figure 4-15 below.

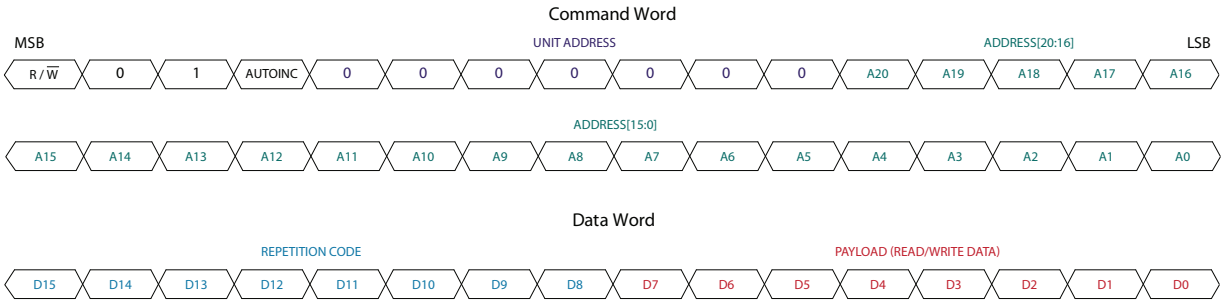


Figure 4-15: Command and Data Word Format

4.10.6 Data Word Description

The Data Word portion of the GSPI access consists of an 8-bit repetition code, followed by an 8-bit Read or Write access Payload. All registers in the GV7704 are 8 bits long, however since GSPI write commands are required to be 16 bits long, the Data Word will have the same byte repeated. For example, to write FC_h to a register within the CSR, the 16-bit Data Word of the GSPI Command should be $FCFC_h$.

4.10.7 GSPI Transaction Timing

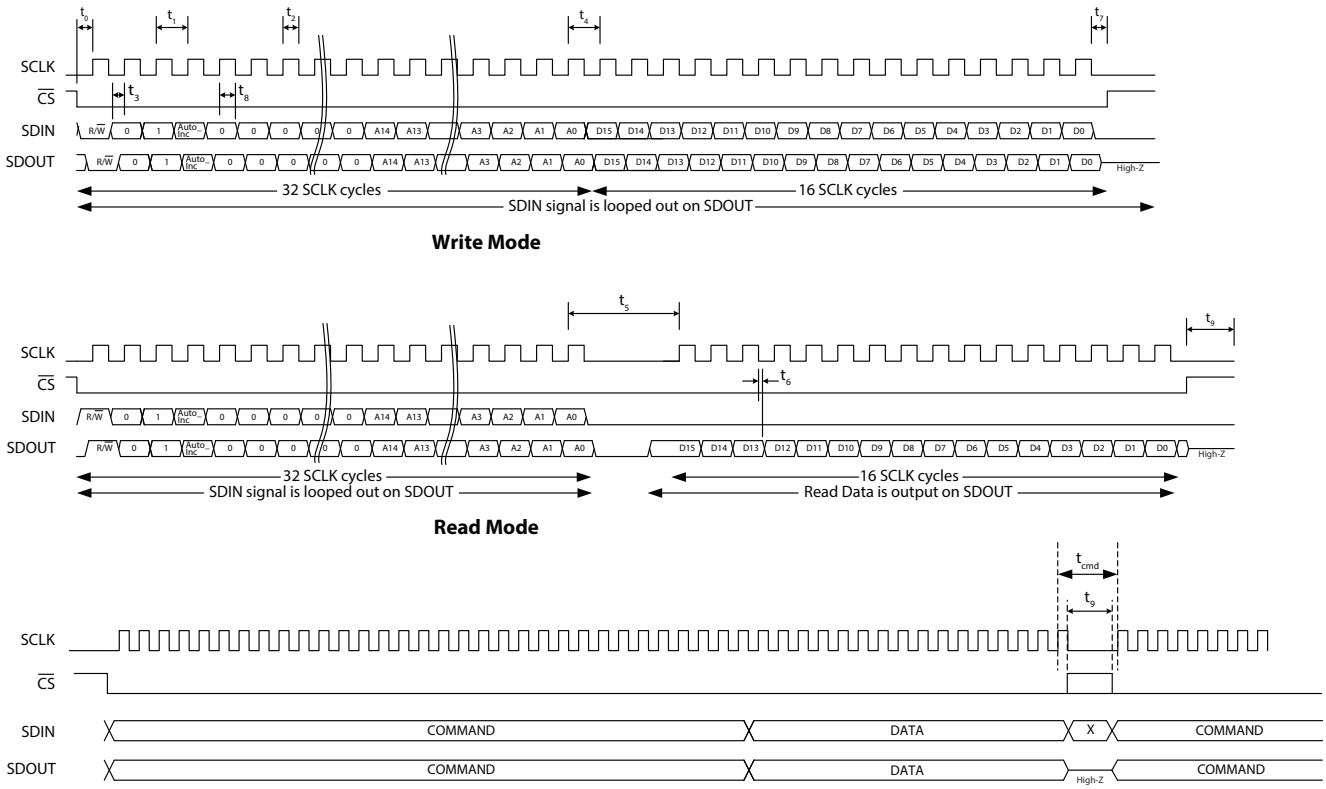


Figure 4-16: GSPI External Interface Timing

Table 4-15: GSPI Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
$\overline{CS}$ LOW before SCLK rising edge	t_0	2.0	—	—	ns
SCLK frequency		—	—	55	MHz
SCLK period	t_1	18.2	—	—	ns
SCLK duty cycle	t_2	40	50	60	%
Input data setup time	t_3	2.7	—	—	ns
SCLK idle time — write	t_4	41.7	—	—	ns
SCLK idle time — read	t_5	162	—	—	ns
Inter-command delay time	t_{cmd}	162	—	—	ns
SDOUT after SCLK falling edge	t_6	—	—	7.5	ns
$\overline{CS}$ HIGH after final SCLK falling edge	t_7	0.0	—	—	ns
Input data hold time	t_8	1.0	—	—	ns

Table 4-15: GSPI Timing Parameters (Continued)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{CS}$ HIGH time	t_9	57.0	—	—	ns
SDIN to SDOUT combinational delay		—	—	5.0	ns

4.10.8 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-17 and Figure 4-18.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 48-bits long, consisting of a Command Word, an Extended Address, and a single Data Word. The read or write cycle begins with a high-to-low transition of the $\overline{CS}$ pin. The read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

The maximum interface clock frequency (SCLK) is 55MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 162ns.

For read access, the time from the last bit of the Command Word to the start of the data output, as defined by t_5, corresponds to no less than 162ns.

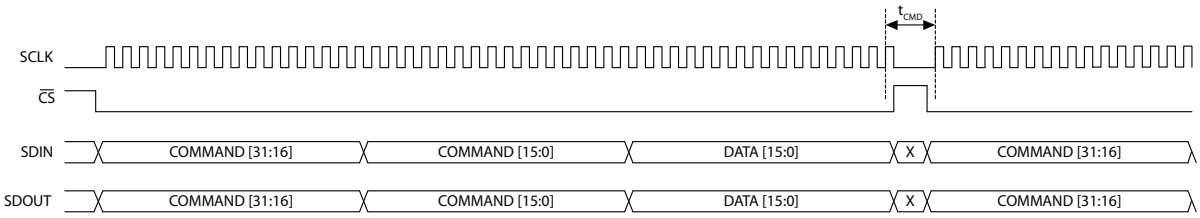


Figure 4-17: GSPI Write Timing – Single Write Access

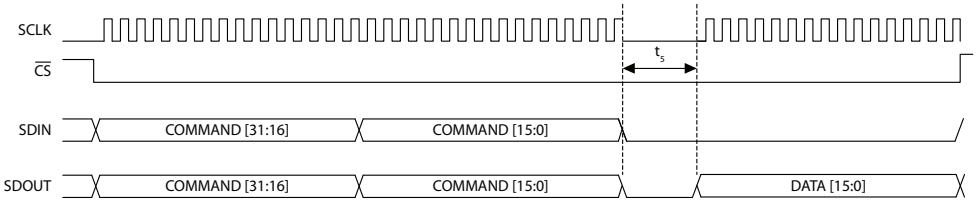


Figure 4-18: GSPI Read Timing – Single Read Access

4.10.9 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-19 and Figure 4-20.

Auto-increment mode is enabled by the setting of the AUTOINC bit of the Command Word.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a HIGH-to-LOW transition of the $\overline{CS}$ pin, and consists of a Command Word and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

Note: Writing to HOST_CONFIG using Auto-increment access is not allowed.

The maximum interface clock frequency (SCLK) is 55MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 162ns.

For read access, the time from the last bit of the first Command Word to the start of the data output of the first Data Word as defined by t_5, will be no less than 162ns. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

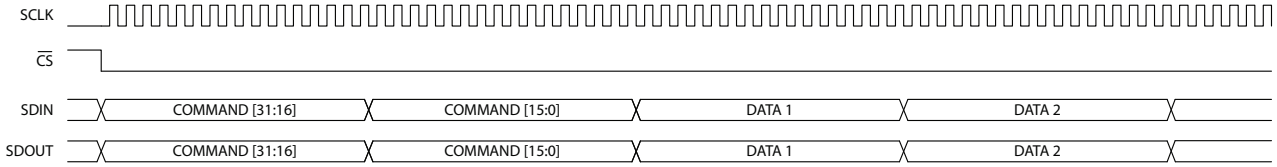


Figure 4-19: GSPI Write Timing – Auto-Increment

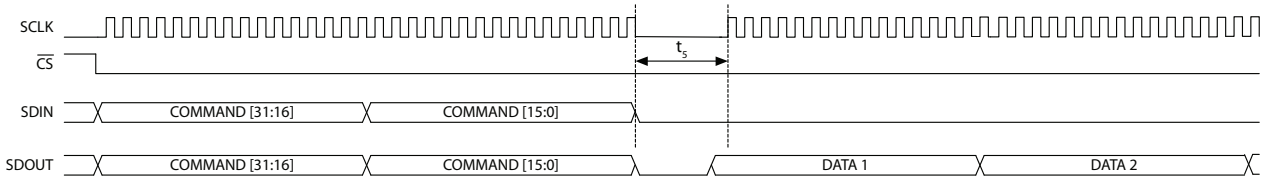


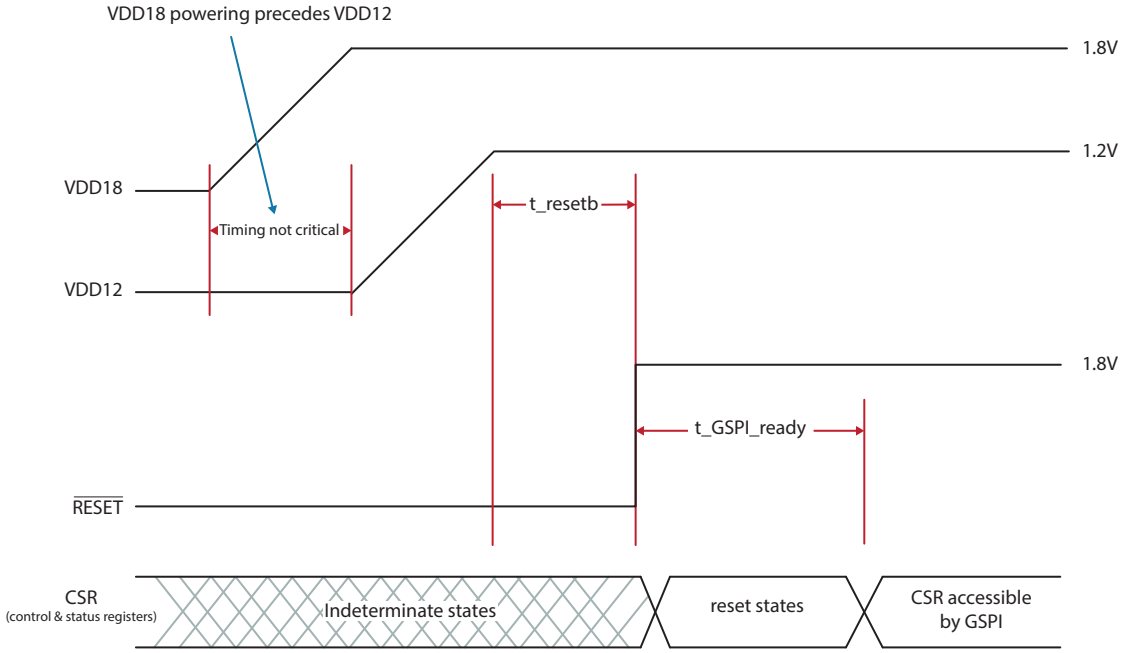
Figure 4-20: GSPI Read Timing – Auto-Increment

4.11 JTAG

The GV7704 provides an IEEE 1149.1-compliant JTAG TAP interface for boundary scan test and debug.

The GV7704 TAP interface consists of the TCK clock input, TRST, TDI and TMS inputs, and the TDO output as defined in the standard. TMS and TDI inputs are clocked with respect to the rising edge of TCK and the TDO output with respect to the falling edge of TCK.

4.12 Power Supply and Reset Timing



T_resetb >= 10ms
T_GSPI_ready = 10µs

Figure 4-21: Power Supply and Reset Timing

Note: To ensure correct digital functionality of the part the 1.8V supply must be powered before the 1.2V supply.

5. Register Map

Table 5-1: GV7704 Register Descriptions — Channel Controls

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
4078_h	GSPI_SDOUT_DRV_STRENGTH_SEL_REG	GSPI_SDOUT_DRV_STRENGTH_SEL	0:0	RW	1_b	GSPI SDOUT drive strength select. 1_b = high drive strength 0_b = low drive strength
$44F1_h$ (Ch 0) $50F1_h$ (Ch 1) $5CF1_h$ (Ch 2) $68F1_h$ (Ch 3)	INPUT_TERMINATION_REG	INPUT_TERMINATION	0:0	RW	1_b	Sets the receive input termination impedance. Termination is to VDD18. 0_b = 50Ω 1_b = 75Ω
$44F2_h$ (Ch 0) $50F2_h$ (Ch 1) $5CF2_h$ (Ch 2) $68F2_h$ (Ch 3)	POWER_UP_DRIVER_REG	PU_DRVN	0:0	RW	0_b	Power up control for the SDO_N path 0_b = Power down 1_b = Power up
		PU_DRVP	1:1	RW	0_b	Power up control for the SDO_P path 0_b = Power down 1_b = Power up
$44F3_h$ (Ch 0) $50F3_h$ (Ch 1) $5CF3_h$ (Ch 2) $68F3_h$ (Ch 3)	P2S_CLK_EN_REG	P2S_CLK_EN	0:0	RW	0_b	Parallel to serial converter in transmit path clock buffer enable 0_b = Clocks in the p2s are turned off 1_b = Clocks in the p2s are enabled
$44F4_h$ (Ch 0) $50F4_h$ (Ch 1) $5CF4_h$ (Ch 2) $68F4_h$ (Ch 3)	P2S_RSTB_REG	P2S_RSTB	0:0	RW	0_b	Parallel to serial converter in transmit path reset 0_b = Hold p2s flops in reset 1_b = P2s not in reset
$44F5_h$ (Ch 0) $50F5_h$ (Ch 1) $5CF5_h$ (Ch 2) $68F5_h$ (Ch 3)	CDR_TX_CLK_EN_REG	CDR_TX_CLK_EN	0:0	RW	0_b	Enable for transmit path clock 0_b = Turn off half rate clock to the p2s in the transmit path 1_b = Turn on half rate clock to the p2s in the transmit path
$44F6_h$ (Ch 0) $50F6_h$ (Ch 1) $5CF6_h$ (Ch 2) $68F6_h$ (Ch 3)	SDO_50_EN_REG	SDO_50_EN	0:0	RW	0_b	SDO_P/N 50Ω termination enable 0_b = 75Ω termination 1_b = 50Ω termination

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
4469_h (Ch 0) 5069_h (Ch 1) $5C69_h$ (Ch 2) 6869_h (Ch 3)	DATALANE_FIFO_CTRL_REG	DATALANE_FIFO_WR_FLUSH	0:0	RW	0_b	Initiates a flush from the writer side on the FIFO. Active HIGH.
		DATALANE_FIFO_RD_START_THRESH	5:1	RW	4_h	Number or items that need to be written to FIFO before the read process starts.
4823_h (Ch 0) 5423_h (Ch 1) 6023_h (Ch 2) $6C23_h$ (Ch 3)	VIDEO_CTRL_OVERRIDE_REG	DISABLE_VIDEO_LANE	5:4	RW	0_h	$X0_b$ = Lane n is enabled 11_b = Lane n is enabled 01_b = Lane n is disabled regardless of the presence of a valid signal
4824_h (Ch 0) 5424_h (Ch 1) 6024_h (Ch 2) $6C24_h$ (Ch 3)	AUDIO_CTRL_OVERRIDE_REG	DISABLE_AUDIO	1:0	RW	0_h	$X0_b$ = Channel n Audio is enabled 11_b = Channel n Audio is enabled 01_b = Channel n Audio is disabled
4825_h (Ch 0) 5425_h (Ch 1) 6025_h (Ch 2) $6C25_h$ (Ch 3)	AUDIO_SAMP_FREQ_OVERRIDE_REG	AUDIO_SAMP_FREQ	2:1	RW	0_h	Manually specifies the audio sampling rate when AUDIO_SAMP_FREQ_MANUAL_MODE = 1 00_b = 48kHz 01_b = 44.1kHz 10_b = 32kHz 11_b = Reserved
		AUDIO_SAMP_FREQ_MANUAL_MODE	0:0	RW	0_b	This mode only needs to be enabled if the audio sampling information is not present in the Stream ID packets. If the incoming signal is transmitted by a GV7700, the information will be present and this mode does not need to be enabled. 1_b = The audio sampling frequency will be manually specified according to AUDIO_SAMP_FREQ. 0_b = The device will automatically detect the audio sampling frequency present within the Stream ID of the video signal.
4829_h (Ch 0) 5429_h (Ch 1) 6029_h (Ch 2) $6C29_h$ (Ch 3)	CLOCKS_CFG_1_REG	PCLK_INVERT	3:3	RW	0	When HIGH, inverts the PCLK.
		PCLK_SELECT	2:1	RW	0	In HD mode, the PCLK can be moved by 0°, 90°, 180°, or 270°. In 3G mode, the PCLK can be moved by 0° or 90°.

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$482C_h$ (Ch 0) $542C_h$ (Ch 1) $602C_h$ (Ch 2) $6C2C_h$ (Ch 3)	GEN_VIDEO_CFG_0_REG	OUT_THREEG_HDB	4:4	RW	0	When HIGH, indicates that the parallel output signal is 3G (Full HD). When LOW, indicates that the output signal is HD.
		THREEG_HDB	2:2	RW	0	When HIGH, indicates that the incoming signal is 3G. When LOW, indicates that the incoming signal is HD.
		SD_HDB	1:1	RO	0_b	When HIGH, indicates that the incoming signal is 270Mb/s. When LOW, indicates that the incoming signal is 1.485Gb/s.
4863_h (Ch 0) 5463_h (Ch 1) 6063_h (Ch 2) $6C63_h$ (Ch 3)	EXTRACT_STREAM_ID_REG1	EXTRACT_STREAM_ID_BYTE1	7:0	RO	0_h	Extract byte 1 information for the packet on DS1 (First UDW in the Stream ID packet)
4864_h (Ch 0) 5464_h (Ch 1) 6064_h (Ch 2) $6C64_h$ (Ch 3)	EXTRACT_STREAM_ID_REG2	EXTRACT_STREAM_ID_BYTE2	7:0	RO	0_h	Extract byte 2 information for the packet on DS1 (First UDW in the Stream ID packet)
4865_h (Ch 0) 5465_h (Ch 1) 6065_h (Ch 2) $6C65_h$ (Ch 3)	EXTRACT_STREAM_ID_REG3	EXTRACT_STREAM_ID_BYTE3	7:0	RO	0_h	Extract byte 3 information for the packet on DS1 (First UDW in the Stream ID packet)
4866_h (Ch 0) 5466_h (Ch 1) 6066_h (Ch 2) $6C66_h$ (Ch 3)	EXTRACT_STREAM_ID_REG4	EXTRACT_STREAM_ID_BYTE4	7:0	RO	0_h	Extract byte 4 information for the packet on DS1 (First UDW in the Stream ID packet)
4867_h (Ch 0) 5467_h (Ch 1) 6067_h (Ch 2) $6C67_h$ (Ch 3)	EXTRACT_STREAM_ID_REG5	EXTRACT_STREAM_ID_BYTE5	7:0	RO	0_h	Extract byte 5 information for the packet on DS1 (First UDW in the Stream ID packet)
4868_h (Ch 0) 5468_h (Ch 1) 6068_h (Ch 2) $6C68_h$ (Ch 3)	EXTRACT_STREAM_ID_REG6	EXTRACT_STREAM_ID_BYTE6	7:0	RO	0_h	Extract byte 6 information for the packet on DS1 (First UDW in the Stream ID packet)

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$487D_h$ (Ch 0) $547D_h$ (Ch 1) $607D_h$ (Ch 2) $6C7D_h$ (Ch 3)	INS_ID_BYTE1_REG	INS_ID_BYTE1	7:0	RWC	0_h	Identification code byte 1
$487E_h$ (Ch 0) $547E_h$ (Ch 1) $607E_h$ (Ch 2) $6C7E_h$ (Ch 3)	INS_ID_BYTE2_REG	INS_ID_BYTE2	7:0	RWC	0_h	Identification code byte 2
$488D_h$ (Ch 0) $548D_h$ (Ch 1) $608D_h$ (Ch 2) $6C8D_h$ (Ch 3)	AUD_EXT_CONFIG_REG	MUTE_2_3	3:3	RW	0_h	Audio Mute for channels 2 & 3. When HIGH, the device will set the CH1_AOUT_2_3 serial output to 0.
		MUTE_0_1	2:2	RW	0_h	Audio Mute for channels 0 & 1. When HIGH, the device will set the CH1_AOUT_0_1 serial output to 0.
$488E_h$ (Ch 0) $548E_h$ (Ch 1) $608E_h$ (Ch 2) $6C8E_h$ (Ch 3)	AUDIO_DID_9_8_REG	AUDIO_DID_9_8	1:0	RW	0_h	Bits 8-9 of the audio packet DID to be extracted.
$488F_h$ (Ch 0) $548F_h$ (Ch 1) $608F_h$ (Ch 2) $6C8F_h$ (Ch 3)	AUDIO_DID_7_0_REG	AUDIO_DID_7_0	7:0	RW	0_h	Bits 0-7 of the audio packet DID to be extracted.
4892_h (Ch 0) 5492_h (Ch 1) 6092_h (Ch 2) $6C92_h$ (Ch 3)	AUDIO_DETECT_0_REG	AUDIO_GRP_DETECT	7:0	RO	0_h	Audio Group detection status. 10000000_b = Group 8 DID detected 01000000_b = Group 7 DID detected 00100000_b = Group 6 DID detected 00010000_b = Group 5 DID detected 00001000_b = Group 4 DID detected 00000100_b = Group 3 DID detected 00000010_b = Group 2 DID detected 00000001_b = Group 1 DID detected

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
4893_h (Ch 0) 5493_h (Ch 1) 6093_h (Ch 2) $6C93_h$ (Ch 3)	AUDIO_DETECT_1_REG	AUDIO_DETECT_1	0:0	RO	0_b	When HIGH, indicates that an ancillary data packet having a DID matching audio_did has been detected in the video.
$48C6_h$ (Ch 0) $54C6_h$ (Ch 1) $60C6_h$ (Ch 2) $6CC6_h$ (Ch 3)	ANC_PACKET_DID_9_8_REG	ANC_PACKET_DID_9_8	1:0	RW	0_h	10-bit DID that the device will seek and extract UDW's from. ANC_PACKET_DID is considered a static signal. Bits [9:8]
$48C7_h$ (Ch 0) $54C7_h$ (Ch 1) $60C7_h$ (Ch 2) $6CC7_h$ (Ch 3)	ANC_PACKET_DID_7_0_REG	ANC_PACKET_DID_7_0	7:0	RWC	0_h	10-bit DID that the device will seek and extract UDW's from. ANC_PACKET_DID is considered a static signal. Bits [7:0]
$48C8_h$ (Ch 0) $54C8_h$ (Ch 1) $60C8_h$ (Ch 2) $6CC8_h$ (Ch 3)	ANC_EXTRACT_STATUS_REG	ANC_PACKET_INCOMPLETE	2:2	RO	0_b	When HIGH, indicates that the packet the device has received contains more than 16 UDWs, which exceeds the maximum allowable amount.
		ANC_EXTRACT_UPDATE_TOGGLE	1:1	ROCW	0_b	Set HIGH when the device has finished extracting all the words from the desired packet type. Writing 1 to this bit clears the status.
		ANC_EXTRACT_IDLE	0:0	RO	0_b	1_b = Device is not currently extracting words from the desired DID packet. 0_b = Device is currently extracting words from the DID packet specified by ANS_PACKET_DID
$48C9_h$ (Ch 0) $54C9_h$ (Ch 1) $60C9_h$ (Ch 2) $6CC9_h$ (Ch 3)	ANC_PACKET_SDID_9_8_REG	ANC_PACKET_SDID_9_8	1:0	RO	0_h	Secondary Data Identification Word extracted from the ancillary data packet. Bits [9:8]
$48CA_h$ (Ch 0) $54CA_h$ (Ch 1) $60CA_h$ (Ch 2) $6CCA_h$ (Ch 3)	ANC_PACKET_SDID_7_0_REG	ANC_PACKET_SDID_7_0	7:0	RO	0_h	Secondary Data Identification Word extracted from the ancillary data packet. Bits [7:0]

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$48CB_h$ (Ch 0) $54CB_h$ (Ch 1) $60CB_h$ (Ch 2) $6CCB_h$ (Ch 3)	ANC_PACKET_DC_9_8_REG	ANC_PACKET_DC_9_8	1:0	RO	0_h	Data Word Count extracted from the ancillary data packet. Represents the number of User Data Words (UDW) in the ancillary data packet. Bits [9:8]
$48CC_h$ (Ch 0) $54CC_h$ (Ch 1) $60CC_h$ (Ch 2) $6CCC_h$ (Ch 3)	ANC_PACKET_DC_7_0_REG	ANC_PACKET_DC_7_0	7:0	RO	0_h	Data Word Count extracted from the ancillary data packet. Represents the number of User Data Words (UDW) in the ancillary data packet. Bits [7:0]
$48CD_h$ (Ch 0) $54CD_h$ (Ch 1) $60CD_h$ (Ch 2) $6CCD_h$ (Ch 3)	ANC_PACKET_UDW0_9_8_REG	ANC_PACKET_UDW0_9_8	1:0	RO	0_h	User Data Word 0 extracted from the ancillary data packet. Bits [9:8]
$48CE_h$ (Ch 0) $54CE_h$ (Ch 1) $60CE_h$ (Ch 2) $6CCE_h$ (Ch 3)	ANC_PACKET_UDW0_7_0_REG	ANC_PACKET_UDW0_7_0	7:0	RO	0_h	User Data Word 0 extracted from the ancillary data packet. Bits [7:0]
$48CF_h$ (Ch 0) $54CF_h$ (Ch 1) $60CF_h$ (Ch 2) $6CCF_h$ (Ch 3)	ANC_PACKET_UDW1_9_8_REG	ANC_PACKET_UDW1_9_8	1:0	RO	0_h	User Data Word 1 extracted from the ancillary data packet. Bits [9:8]
$48D0_h$ (Ch 0) $54D0_h$ (Ch 1) $60D0_h$ (Ch 2) $6CD0_h$ (Ch 3)	ANC_PACKET_UDW1_7_0_REG	ANC_PACKET_UDW1_7_0	7:0	RO	0_h	User Data Word 1 extracted from the ancillary data packet. Bits [7:0]
$48D1_h$ (Ch 0) $54D1_h$ (Ch 1) $60D1_h$ (Ch 2) $6CD1_h$ (Ch 3)	ANC_PACKET_UDW2_9_8_REG	ANC_PACKET_UDW2_9_8	1:0	RO	0_h	User Data Word 2 extracted from the ancillary data packet. Bits [9:8]
$48D2_h$ (Ch 0) $54D2_h$ (Ch 1) $60D2_h$ (Ch 2) $6CD2_h$ (Ch 3)	ANC_PACKET_UDW2_7_0_REG	ANC_PACKET_UDW2_7_0	7:0	RO	0_h	User Data Word 2 extracted from the ancillary data packet. Bits [7:0]

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$48D3_h$ (Ch 0) $54D3_h$ (Ch 1) $60D3_h$ (Ch 2) $6CD3_h$ (Ch 3)	ANC_PACKET_UDW3_9_8_REG	ANC_PACKET_UDW3_9_8	1:0	RO	0_h	User Data Word 3 extracted from the ancillary data packet. Bits [9:8]
$48D4_h$ (Ch 0) $54D4_h$ (Ch 1) $60D4_h$ (Ch 2) $6CD4_h$ (Ch 3)	ANC_PACKET_UDW3_7_0_REG	ANC_PACKET_UDW3_7_0	7:0	RO	0_h	User Data Word 3 extracted from the ancillary data packet. Bits [7:0]
$48D5_h$ (Ch 0) $54D5_h$ (Ch 1) $60D5_h$ (Ch 2) $6CD5_h$ (Ch 3)	ANC_PACKET_UDW4_9_8_REG	ANC_PACKET_UDW4_9_8	1:0	RO	0_h	User Data Word 4 extracted from the ancillary data packet. Bits [9:8]
$48D6_h$ (Ch 0) $54D6_h$ (Ch 1) $60D6_h$ (Ch 2) $6CD6_h$ (Ch 3)	ANC_PACKET_UDW4_7_0_REG	ANC_PACKET_UDW4_7_0	7:0	RO	0_h	User Data Word 4 extracted from the ancillary data packet. Bits [7:0]
$48D7_h$ (Ch 0) $54D7_h$ (Ch 1) $60D7_h$ (Ch 2) $6CD7_h$ (Ch 3)	ANC_PACKET_UDW5_9_8_REG	ANC_PACKET_UDW5_9_8	1:0	RO	0_h	User Data Word 5 extracted from the ancillary data packet. Bits [9:8]
$48D8_h$ (Ch 0) $54D8_h$ (Ch 1) $60D8_h$ (Ch 2) $6CD8_h$ (Ch 3)	ANC_PACKET_UDW5_7_0_REG	ANC_PACKET_UDW5_7_0	7:0	RO	0_h	User Data Word 5 extracted from the ancillary data packet. Bits [7:0]
$48D9_h$ (Ch 0) $54D9_h$ (Ch 1) $60D9_h$ (Ch 2) $6CD9_h$ (Ch 3)	ANC_PACKET_UDW6_9_8_REG	ANC_PACKET_UDW6_9_8	1:0	RO	0_h	User Data Word 6 extracted from the ancillary data packet. Bits [9:8]
$48DA_h$ (Ch 0) $54DA_h$ (Ch 1) $60DA_h$ (Ch 2) $6CDA_h$ (Ch 3)	ANC_PACKET_UDW6_7_0_REG	ANC_PACKET_UDW6_7_0	7:0	RO	0_h	User Data Word 6 extracted from the ancillary data packet. Bits [7:0]

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$48DB_h$ (Ch 0) $54DB_h$ (Ch 1) $60DB_h$ (Ch 2) $6CDB_h$ (Ch 3)	ANC_PACKET_UDW7_9_8_REG	ANC_PACKET_UDW7_9_8	1:0	RO	0_h	User Data Word 7 extracted from the ancillary data packet. Bits [9:8]
$48DC_h$ (Ch 0) $54DC_h$ (Ch 1) $60DC_h$ (Ch 2) $6CDC_h$ (Ch 3)	ANC_PACKET_UDW7_7_0_REG	ANC_PACKET_UDW7_7_0	7:0	RO	0_h	User Data Word 7 extracted from the ancillary data packet. Bits [7:0]
$48DD_h$ (Ch 0) $54DD_h$ (Ch 1) $60DD_h$ (Ch 2) $6CDD_h$ (Ch 3)	ANC_PACKET_UDW8_9_8_REG	ANC_PACKET_UDW8_9_8	1:0	RO	0_h	User Data Word 8 extracted from the ancillary data packet. Bits [9:8]
$48DE_h$ (Ch 0) $54DE_h$ (Ch 1) $60DE_h$ (Ch 2) $6CDE_h$ (Ch 3)	ANC_PACKET_UDW8_7_0_REG	ANC_PACKET_UDW8_7_0	7:0	RO	0_h	User Data Word 8 extracted from the ancillary data packet. Bits [7:0]
$48DF_h$ (Ch 0) $54DF_h$ (Ch 1) $60DF_h$ (Ch 2) $6CDF_h$ (Ch 3)	ANC_PACKET_UDW9_9_8_REG	ANC_PACKET_UDW9_9_8	1:0	RO	0_h	User Data Word 9 extracted from the ancillary data packet. Bits [9:8]
$48E0_h$ (Ch 0) $54E0_h$ (Ch 1) $60E0_h$ (Ch 2) $6CE0_h$ (Ch 3)	ANC_PACKET_UDW9_7_0_REG	ANC_PACKET_UDW9_7_0	7:0	RO	0_h	User Data Word 9 extracted from the ancillary data packet. Bits [7:0]
$48E1_h$ (Ch 0) $54E1_h$ (Ch 1) $60E1_h$ (Ch 2) $6CE1_h$ (Ch 3)	ANC_PACKET_UDW10_9_8_REG	ANC_PACKET_UDW10_9_8	1:0	RO	0_h	User Data Word 10 extracted from the ancillary data packet. Bits [9:8]
$48E2_h$ (Ch 0) $54E2_h$ (Ch 1) $60E2_h$ (Ch 2) $6CE2_h$ (Ch 3)	ANC_PACKET_UDW10_7_0_REG	ANC_PACKET_UDW10_7_0	7:0	RO	0_h	User Data Word 10 extracted from the ancillary data packet. Bits [7:0]

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$48E3_h$ (Ch 0) $54E3_h$ (Ch 1) $60E3_h$ (Ch 2) $6CE3_h$ (Ch 3)	ANC_PACKET_UDW11_9_8_REG	ANC_PACKET_UDW11_9_8	1:0	RO	0_h	User Data Word 11 extracted from the ancillary data packet. Bits [9:8]
$48E4_h$ (Ch 0) $54E4_h$ (Ch 1) $60E4_h$ (Ch 2) $6CE4_h$ (Ch 3)	ANC_PACKET_UDW11_7_0_REG	ANC_PACKET_UDW11_7_0	7:0	RO	0_h	User Data Word 11 extracted from the ancillary data packet. Bits [7:0]
$48E5_h$ (Ch 0) $54E5_h$ (Ch 1) $60E5_h$ (Ch 2) $6CE5_h$ (Ch 3)	ANC_PACKET_UDW12_9_8_REG	ANC_PACKET_UDW12_9_8	1:0	RO	0_h	User Data Word 12 extracted from the ancillary data packet. Bits [9:8]
$48E6_h$ (Ch 0) $54E6_h$ (Ch 1) $60E6_h$ (Ch 2) $6CE6_h$ (Ch 3)	ANC_PACKET_UDW12_7_0_REG	ANC_PACKET_UDW12_7_0	7:0	RO	0_h	User Data Word 12 extracted from the ancillary data packet. Bits [7:0]
$48E7_h$ (Ch 0) $54E7_h$ (Ch 1) $60E7_h$ (Ch 2) $6CE7_h$ (Ch 3)	ANC_PACKET_UDW13_9_8_REG	ANC_PACKET_UDW13_9_8	1:0	RO	0_h	User Data Word 13 extracted from the ancillary data packet. Bits [9:8]
$48E8_h$ (Ch 0) $54E8_h$ (Ch 1) $60E8_h$ (Ch 2) $6CE8_h$ (Ch 3)	ANC_PACKET_UDW13_7_0_REG	ANC_PACKET_UDW13_7_0	7:0	RO	0_h	User Data Word 13 extracted from the ancillary data packet. Bits [7:0]
$48E9_h$ (Ch 0) $54E9_h$ (Ch 1) $60E9_h$ (Ch 2) $6CE9_h$ (Ch 3)	ANC_PACKET_UDW14_9_8_REG	ANC_PACKET_UDW14_9_8	1:0	RO	0_h	User Data Word 14 extracted from the ancillary data packet. Bits [9:8]
$48EA_h$ (Ch 0) $54EA_h$ (Ch 1) $60EA_h$ (Ch 2) $6CEA_h$ (Ch 3)	ANC_PACKET_UDW14_7_0_REG	ANC_PACKET_UDW14_7_0	7:0	RO	0_h	User Data Word 14 extracted from the ancillary data packet. Bits [7:0]

Table 5-1: GV7704 Register Descriptions — Channel Controls (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$48EB_h$ (Ch 0) $54EB_h$ (Ch 1) $60EB_h$ (Ch 2) $6CEB_h$ (Ch 3)	ANC_PACKET_UDW15_9_8_REG	ANC_PACKET_UDW15_9_8	1:0	RO	0_h	User Data Word 15 extracted from the ancillary data packet. Bits [9:8]
$48EC_h$ (Ch 0) $54EC_h$ (Ch 1) $60EC_h$ (Ch 2) $6CEC_h$ (Ch 3)	ANC_PACKET_UDW15_7_0_REG	ANC_PACKET_UDW15_7_0	7:0	RO	0_h	User Data Word 15 extracted from the ancillary data packet. Bits [7:0]
$48ED_h$ (Ch 0) $54ED_h$ (Ch 1) $60ED_h$ (Ch 2) $6CED_h$ (Ch 3)	ANC_PACKET_CS_9_8_REG	ANC_PACKET_CS_9_8	1:0	RO	0_h	CS Word extracted from the ancillary data packet. Equal to the nine least significant bits of the sum of the nine least significant bits of the data identification (DID) word, the data block number (DBN)/ secondary data identification word (SDID), the data count (DC) word, and all user data words (UDW) in the packet. Bits [9:8]
$48EE_h$ (Ch 0) $54EE_h$ (Ch 1) $60EE_h$ (Ch 2) $6CEE_h$ (Ch 3)	ANC_PACKET_CS_7_0_REG	ANC_PACKET_CS_7_0	7:0	RO	0_h	CS Word extracted from the ancillary data packet. Bits [7:0]
$48EF_h$ (Ch 0) $54EF_h$ (Ch 1) $60EF_h$ (Ch 2) $6CEF_h$ (Ch 3)	OUTPUT_BLOCK_CFG_REG	BT656_ENABLE	0:0	RW	0_b	1_b = Device generates the BT656 10-bit YCbCr multiplexed video format 0_b = Device generates the default SMPTE 10-bit YCbCr multiplexed video format
$48F4_h$ (Ch 0) $54F4_h$ (Ch 1) $60F4_h$ (Ch 2) $6CF4_h$ (Ch 3)	TX_WORD_CLK_ENABLE_REG	TX_WORD_CLK_ENABLE	0:0	RW	0_b	Used in the procedure to enable SDO. See Section 4.3.2.1 for details
$492C_h$ (Ch 0) $552C_h$ (Ch 1) $612C_h$ (Ch 2) $6D2C_h$ (Ch 3)	PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL_REG	PARALLEL_VIDEO_OUT_DRV_STRENGTH_SEL	0:0	RW	0_b	Parallel video output (PCLK, HOUT, VOUT, FOUT, DOUT[9:0]) drive strength select. 1_b= high drive strength 0_b = low drive strength

6. Application Information

6.1 Typical Application Circuit

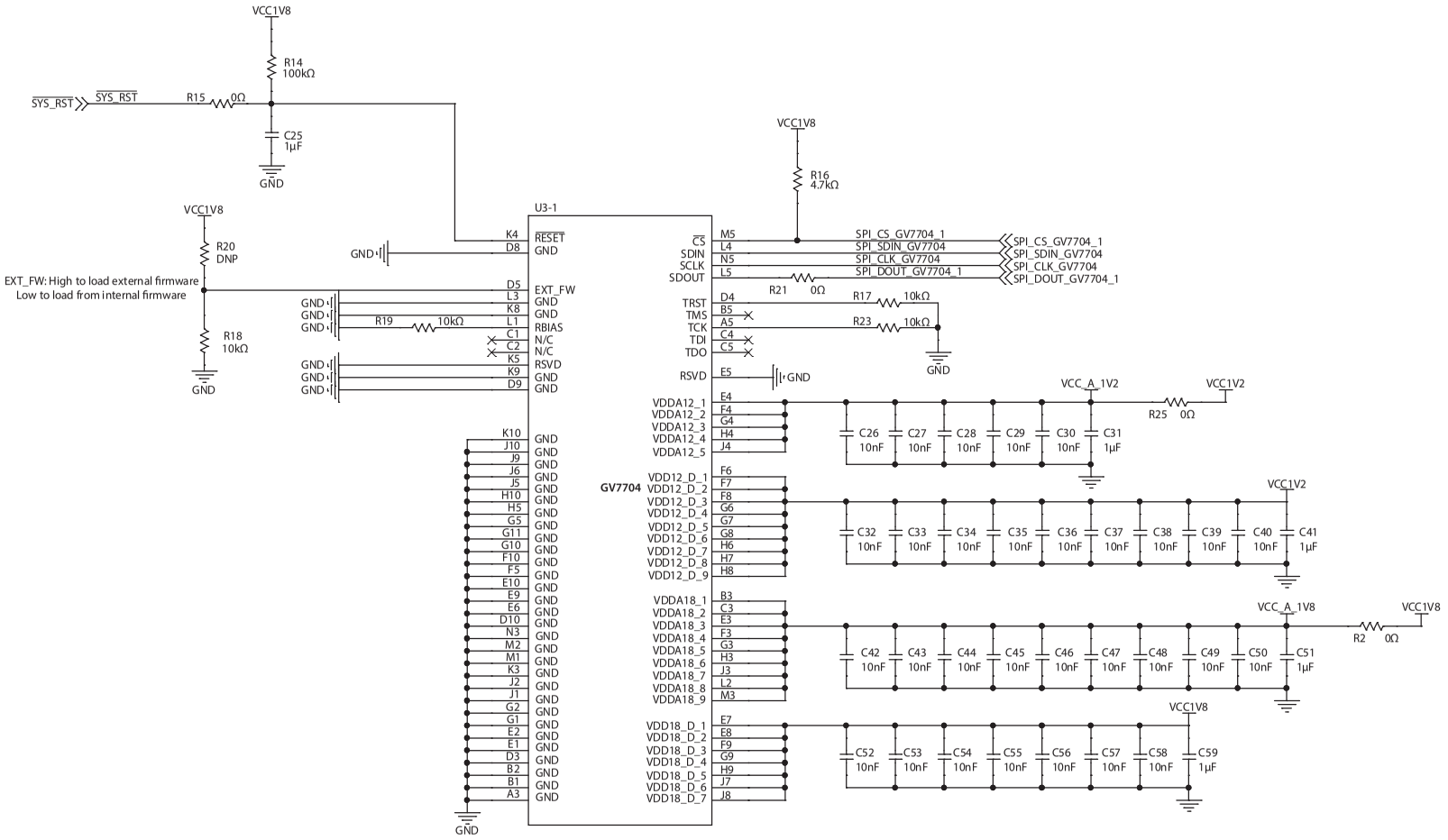


Figure 6-1: Typical Application Circuit (Part 1)

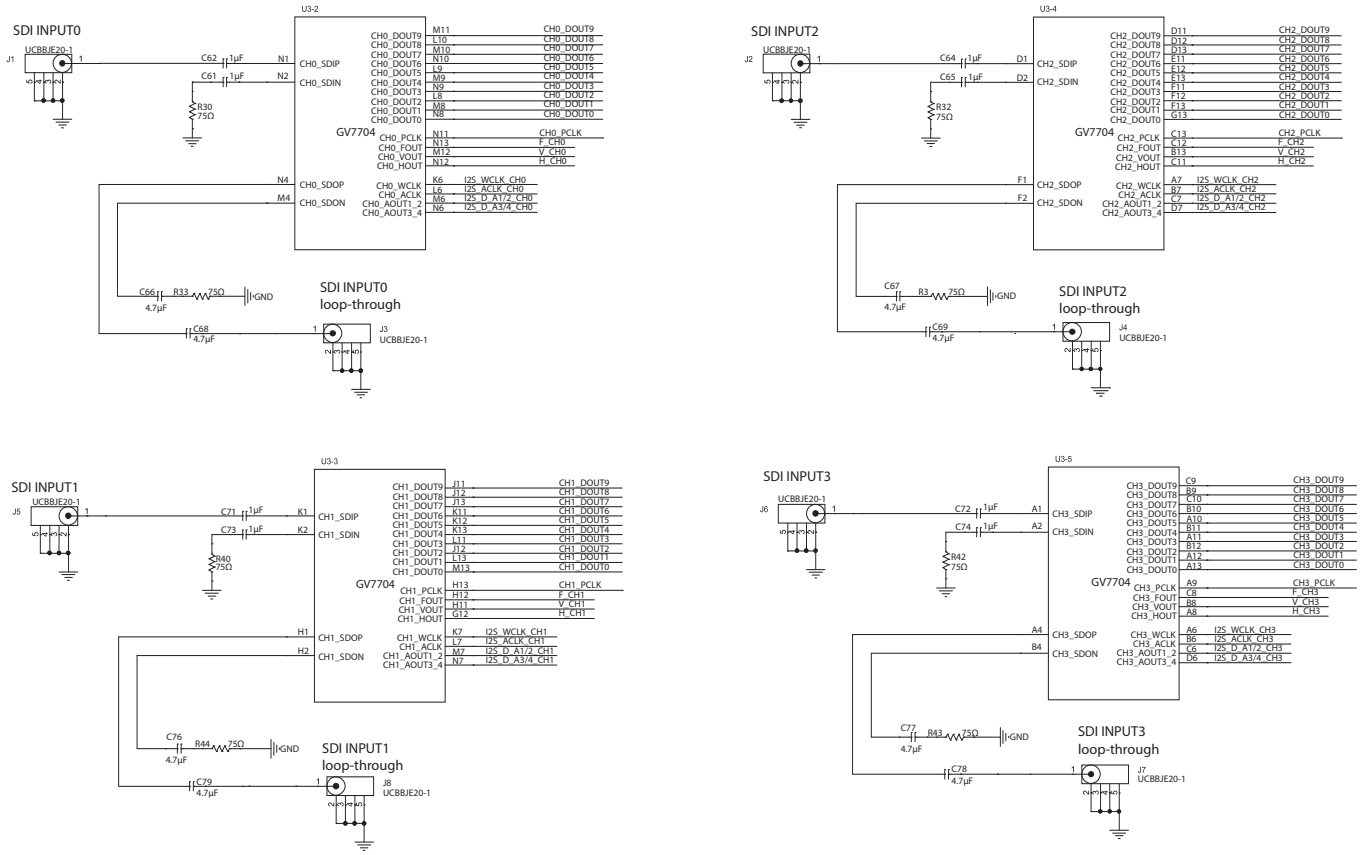


Figure 6-2: Typical Application Circuit (Part 2)

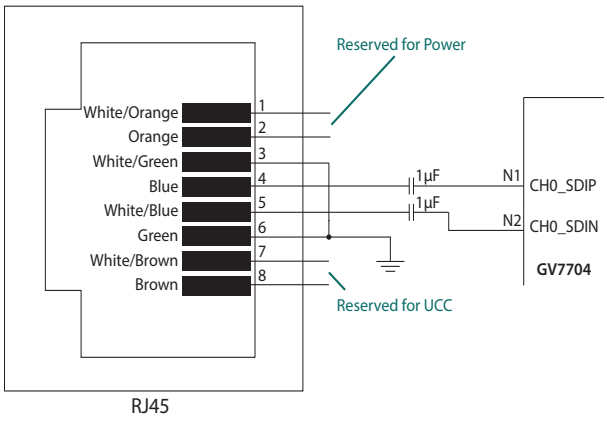
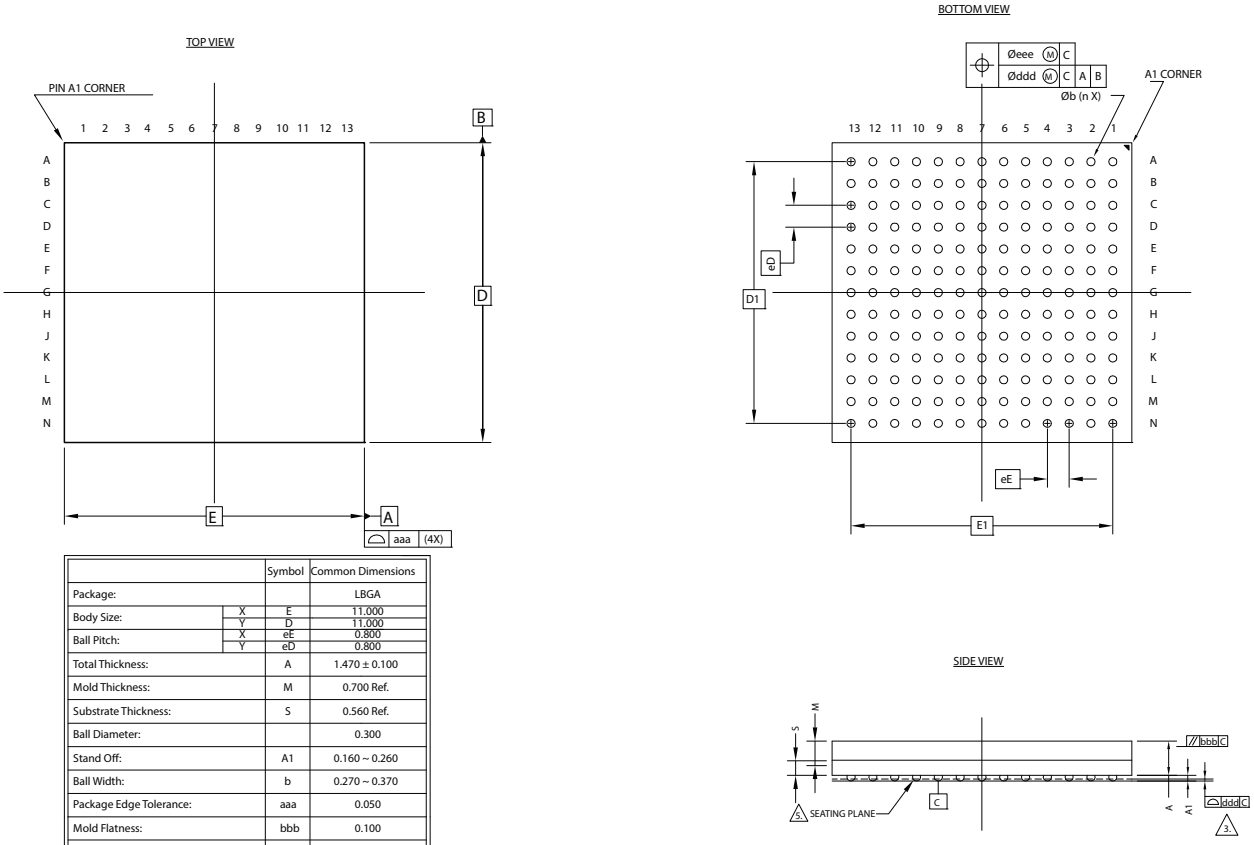


Figure 6-3: Alternative CATx Input Circuit

7. Packaging Information

7.1 Package Dimensions



		Symbol	Common Dimensions
Package:			LBGA
Body Size:	X	E	11.000
	Y	D	11.000
Ball Pitch:	X	eE	0.800
	Y	eD	0.800
Total Thickness:		A	1.470 ± 0.100
Mold Thickness:		M	0.700 Ref.
Substrate Thickness:		S	0.560 Ref.
Ball Diameter:			0.300
Stand Off:		A1	0.160 ~ 0.260
Ball Width:		b	0.270 ~ 0.370
Package Edge Tolerance:		aaa	0.050
Mold Flatness:		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package):		eee	0.150
Ball Offset (Ball):		fff	0.050
Ball Count:		n	169
Edge Ball Center to Center:	X	E1	9.600
	Y	D1	9.600

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 7-1: GV7704 Package Dimensions

7.2 Recommended PCB Footprint

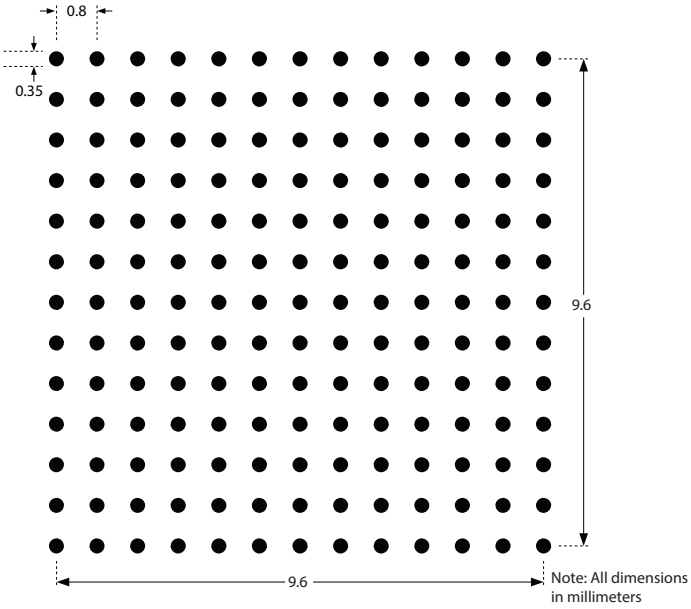


Figure 7-2: GV7704 PCB Footprint

7.3 Marking Diagram

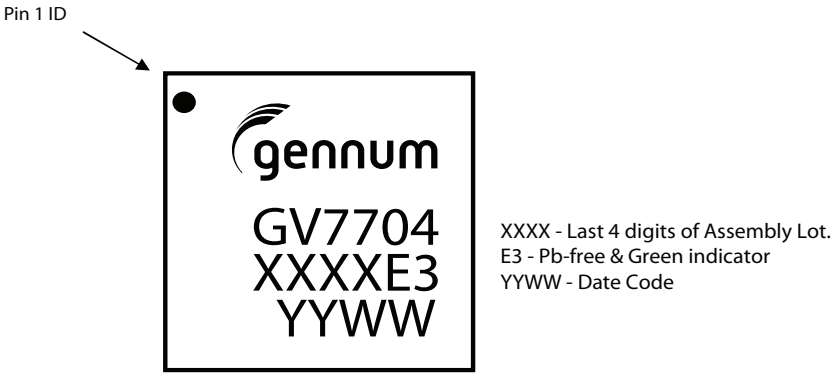


Figure 7-3: GV7704 Marking Diagram

7.4 Solder Reflow Profile

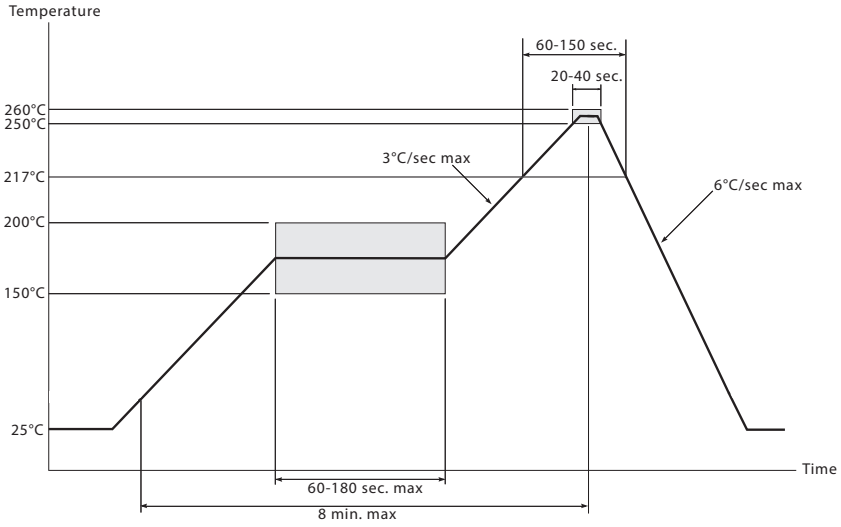


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.5 Packaging Data

Table 7-1: GV7704 Packaging Data

Parameter	Value
Package Type/Dimensions/Pad Pitch	169 WB-BGA 11mm x 11mm, 0.8mm pitch
Moisture Sensitivity Level (MSL)	3
Junction to Case Thermal Resistance, θ_{j-c}	12.1°C/W
Junction to Ambient Thermal Resistance (zero airflow), θ_{j-a}	35.4°C/W
Junction-to-Top of Package Characterization, θ_{j-t}	0.14°C/W
Junction to Board Thermal Resistance, θ_{j-b}	25.7°C/W
Pb-free and RoHS Compliant	Yes

7.6 Ordering Information

Table 7-2: GV7704 Ordering Information

Part	Package
GV7704-IBE3	169-pin LBGA (176 pc/Tray)

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com