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WiSmart™
EC32L1x, EC32L2x, EC32L4x
Datasheet
ULPE Wi-Fi modules

econais
Powers the Internet of Things

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1 Introduction

WiSmart™ is a versatile, self-contained ultra-low power embedded Wi-Fi modules family for adding Wi-Fi functionality to any existing or new electronic device, sensor, meter or appliance.

The EC32Lxx modules are surface mounted

WiSmart™ is small in size, high performance design, with models based on the STM32F1x, STM32F2x and STM32F4x families of low power, high performance 32-bit MCUs, combined with the smallest and lowest power consumption Wi-Fi chip in the market.

There are three series of WiSmart™ modules differentiating between them on the MCU assembled in the modules.

Baseline models:

- EC32L11 using STM32F103RD Cortex M3 MCU
- EC32L12 using STM32F103RE Cortex M3 MCU
- EC32L13 using STM32F103RF Cortex M3 MCU
- EC32L14 using STM32F103RG Cortex M3 MCU

Advanced models:

- EC32L22 using STM32F205RE Cortex M3 MCU
- EC32L23 using STM32F205RF Cortex M3 MCU and
- EC32L24 using STM32F205RG Cortex M3 MCU

High Performance model:

- EC32L44 using STM32F405RG Cortex M4 MCU

All the models are pin-to-pin compatible, exporting the same HW interfaces. The performance of the exported HW interfaces differs between the models.

Please refer to Chapter 8.1 for details on each the available MCU and their HW interface characteristics for the EC32Lxx modules.

The EC32L13 Baseline model is the most commonly used, covering most of the IoT and M2M applications.

WiSmart™ modules run a powerful software stack provided as library which includes:

- TCP-IP stack supporting UDP/TCP sockets, both RAW and BSD format
- The kernel of ChibiOS RTOS (GNU licensed)
- Wi-Fi driver
- Wi-Fi management engine
- WPA/WPA2 supplicant
- SSL/HTTPS
- RTC based Power Management Engine
- Many free Source Code applications demonstrating the way to add custom application code on top of the provided library.

The default WiSmart™ library provides out-of-the-box supports Wi-Fi Ad-Hoc, Wi-Fi client, Wi-Fi AP modes f operation and WPS with Push-Button and PIN options.

Customer can make use of the well-defined API exported by the module in order to achieve short

time to market and very short learning curve.

There is plenty of FLASH memory left free for any customer application to be developed and run in the module MCU. The RAM/FLASH footprint of the library varies depending to included features.

Depending on the application it is possible to provide for entry level models a library with minimal functions.

The customer applications (i.e. for reading data from a HW interface and sending them to network) will need only a couple of kilobytes space as almost everything is in the library and the custom code will need just to make calls to the ECONAIS library functions or to STM library functions.

WiSmart™ platform and family of products is the ideal development platform for wireless application like but not limited to:

- Thermostats
- Wi-Fi enabled sensors (i.e. CO_2 sensors)
- Smart Meters (Electrical Smart Grid applications), Gas Meters, Water Flow meters
- Remote Control units, Garage door open system
- Security/Surveillance (Motion Detector, Fire alarms, Area monitoring)
- Air-condition units and white appliances
- Lighting control
- Building automation
- Automotive applications
- Wi-Fi audio solutions

1.1 Features

The following table describes in details the available features.

Feature	Info/Comments
Open (no encryption)	YES
WEP 64/128 bits	YES
WPA/WPA2 PSK (TKIP/AES)	YES
WPA/WPA2 Enterprise	YES (TLS, TTLS, PEAP)
WPS 2.0	YES (Push Button and Pin Methods)
802.11 b/g/n (2.4 GHz)	YES
Access Point (AP) mode	YES (up to 3 clients by default, up to 5 clients on demand)
Client (STA) mode	YES
Ad-Hoc	YES
RF band	2.4 GHz
Supported 802.11 channels	1-14
Wake On Lan	NO
Site Survey functionality available to customer code	YES
Configurable parameters for Site Survey available to customer	YES
Advanced Soft and Hard Cut Roaming with configurable alert zone limits.	YES (Less than 20ms AP handover time)
Configurable Background Scan	YES
HTTPS/SSL support	YES
DHCP client	YES
DHCP Server (Available only in AP mode)	YES
DNS Client	YES
FTP Client	ON DEMAND for specific projects
FTP Server	ON DEMAND for specific projects
HTTP Client	YES
HTTP Server	YES By default used for WiSmart Configuration
SD card support with FAT FS	ON DEMAND for specific projects
HTTP Audio streaming	YES
RTP Audio Streaming	YES
DLNA (Compatible with DLNA 1.5)	YES Audio renderer - DMR and Media server - DMS

The EC32Lxx modules are available in two antenna configurations:

1) On module Chip antenna
2) With a connector for external antenna (chapter 15)

Using the on module chip antenna the modules has range up to 400m in open space, line of sight without any enclosure or cover of the WiSmart™, using MAX RF TX power. Indoors the range varies and depends on the structure the material and the surfaces of the building. Typical indoor

range with the chip antenna is between 25m and 50m.

When used external antenna, its central frequency should be 2.450 to 2.500 GHz, the bandwidth should be 100MHz, the VSWR should be 1.92 to 2 max and the impedance should be 50 Ohm

2 Recommended Operation & Storage Conditions

Table 1 shows the recommended temperature range of temperature for storage and operation of the WiSmart™ modules.

Rating	Min	Max	Unit
Storage Temperature	-50	+125	°C
Operating Temperature	-30	+85	°C

Table 1: Recommended operation & storage conditions

NOTE:

- If WiSmart™ EC32Lxx will be operated **only** at -28°C to -30°C range the recommended voltage supply is 3.6V in order to maintain the maximum range.
  If in this temperature range (-28°C to -30°C) the supply voltage is 3.3V, the range of WiSmart™ is expected to be degraded by a couple of meters.
  WiSmart™ functionality and network performance is not affected by the voltage or the temperature.
- If WiSmart™ EC32Lxx will be operated at different temperatures in the range of -30°C to +85 °C the recommended voltage supply is 3.3V.

If the device is stored in conditions outside recommended Storage Temperature range it might be damaged.

If the device is operated in temperature ranges exceeding the Operating Temperature rage, it might stop performing as designed or stop working. RF output power is expected to degrade up to -2dB as the device temperature closes the limits of the Operating Temperature range.

The normal device operation is expected to be resumed as soon as the device returns within the recommended Operating Temperature range.

3 Power Supply

WiSmart™ typical power supply is 3.3V. For very low temperatures the voltage must be increased. For operation at -30°C the supply voltage should be 3.6V.

Power should be supplied to WiSmart™ pins 3, 50 and 51. Please refer to pin assignment table on page 16.

Maximum current (peak) for 3.3V power supply using internal clock at 64MHz and having all peripherals enabled iis 282.5mA

Maximum current (peak) for 3.3V power supply, using external clock at 72MHz and all peripherals enabled is or 289.5mA.

Minimum, maximum and typical values for the supply voltages are shown in Table 2.

Rating	Min	Typ	Max	Unit
Supply Voltage VCC	2.75	3.3	3.6	V

Table 2: WiSmart power supply voltage

IMPORTANT NOTE: At -30°C the supply voltage should be 3.6V.

3.1 Ground Pins

The WiSmart™ is an RF device and requires as such a good RF grounding.

It is very important to connect all ground pins to GND. Please refer to pin assignment table on page 16.

3.2 Power-up sequence

To power-up the module apply a voltage within the recommended range to all VCC pads and have connected all GND pads.

The module need maximum 500ms before is ready to accept any command or exchange data through the peripherals. This time includes all the software and hardware initialization procedures.

4 Wi-Fi RF Specifications

Conditions: VBAT = 3.6 V. Operating temperature Tamb = 25°C.

4.1 Wi-Fi receiver RF sensitivity

Item	Data Rate	Modulation	EC32Lxx	Unit
Receiver minimum input level sensitivity for 802.11 b/g	1 Mbps	DPSK	-94	dBm
	2 Mbps	QDPSK	-91	dBm
	5.5 Mbps	CCK/DPSK	-89	dBm
	11 Mbps	CCK/QDPSK	-87	dBm
	6 Mbps	ODFM/BPSK	-89	dBm
	9 Mbps	ODFM/BPSK	-88	dBm
	12 Mbps	ODFM/BPSK	-87	dBm
	18 Mbps	ODFM/BPSK	-86	dBm
	24 Mbps	OFDM/16-QAM	-82	dBm
	36 Mbps	OFDM/16-QAM	-79	dBm
	48 Mbps	OFDM/64-QAM	-74	dBm
	54 Mbps	OFDM/64-QAM	-72	dBm
Receiver minimum input level sensitivity for 802.11 n	7.2 Mbps	OFDM/QPSK	-88	dBm
	14.4 Mbps	OFDM/QPSK	-85	dBm
	21.7 Mbps	OFDM/QPSK	-83	dBm
	28.9 Mbps	OFDM/16-QAM	-80	dBm
	43.4 Mbps	OFDM/16-QAM	-77	dBm
	57.8 Mbps	OFDM/64-QAM	-73	dBm
	65 Mbps	OFDM/64-QAM	-71	dBm
	72.2 Mbps	OFDM/64-QAM	-69	dBm

Table 3: receiver RF sensitivity

4.2 Wi-Fi transmitter RF specifications

Item	Conditions	EC32Lxx		Unit
		Typ	Max	
Transmit Output Power Levels	802.11b	17	18	dBm
	802.11g	13	14.5	dBm
	802.11n	12	13.5	dBm

Table 4: Transmitter RF output power

4.3 Operating Channels

WiSmart™ Wi-Fi can operate in the 2.4GHz band in channels and frequencies as shown in Table 5.

Item	Min	Max	Unit
Center Frequency	2412	2484	MHz
Channel	1	14	Channel Numbers

Table 5: Channels and frequencies

4.4 Supported Wi-Fi operating modes and features

WiSmart™ modules support the Wi-Fi modes of operation and Wi-Fi features as shown in Table 6.

Wi-Fi feature	Supported mode/feature	Description
Modes of operation	Client (STA), AP, Ad-Hoc,	**Wi-Fi client (STA mode):** WiSmart™ joins and connects to an existing network. In this Wi-Fi network there is a managing device (i.e. an AP or a Wi-Fi router). The AP or Wi-Fi Route is controlling the access of the devices to the Wi-Fi network and the flow of data is through the AP or Wi-Fi router. There is full Wi-Fi power save support for this mode and the power consumption is dramatically decreased. **AP mode:** In this mode the WiSmart™ becomes the AP and manages the Wi-Fi network. Other devices can connect directly to WiSmart as they would with any other Wi-Fi AP or router. There is full Wi-Fi power save support in this mode. The WiSmart acting as AP need to transmit beacon frames (Wi-Fi management packets) in order for another device to detect it and attempt to connect to it. This increases slightly the WiSmart™ power consumption in this mode comparing to Wi-Fi client mode. WiSmart™ controls the data flow in this mode. **Ad-Hoc:** WiSmart™ connects directly with other Wi-Fi devices in a peer-to-peer Wi-Fi network without any Wi-Fi network management from any of the participating devices. This is legacy direct device connection. In Ad-Hoc mode there is no Wi-Fi power save feature available for Wi-Fi devices thus the power consumption is increased.
Security configuration	Open, WEP, WPA/TKIP, WPA/AES, WPA2/TKIP, WPA2/AES, WPS	WEP support WPA/WPA2 PSK WPA/WPA2 Enterprise (TLS/TTLS/PEAP) WPS (PIN, Push button)
Roaming	Fast roaming	Fast roaming enables WiSmart™ to switch APs in less than 20ms

Table 6: Wi-Fi Operating modes and features

5 Wi-Fi Standards Compliance

5.1 IEEE/IETF

Standard	Revision	Description
802.11	802.11 R2003	WLAN MAC& PHY
802.11b	802.11 R2003	High rate DSSS (5,5/11Mbit/s)
802.11d	802.11 R2003	Operation in different regulatory domains
802.11e	D9,0 Aug. 2004	QoS enhancements
802.11g	-2003	Extended rate PHY (ERP-PBCC, DSS-OFDM)
802.11i	-2004	Security enhancements
802.11k	Draft 11.0, 2008	Wireless network management
802.11r	Draft 9.0, 2008	Fast BSS transition
802.11h	1997 edition	Bridge tunneling
RFC1023	Inherent	Frame encapsulation
802.15.2		Bluetooth coexistence

Table 7: IEEE/IETF standards compliance

5.2 Wi-Fi

Specification	Description	Revision
Wi-Fi 802.11b with WPA system interoperability test plan for IEEE 802.11b devices	802.11b devices with WPA	2.1
Wi-Fi 802.11g with WPA system interoperability test plan	802.11g devices with WPA	2.0

Table 8: Wi-Fi standards compliance

5.3 Wi-Fi Regulatory compliance

Country	Approval authority	Regulatory	Frequency Band (GHz)
USA	FCC	FCC	2.4-2.4835
Europe / Canada	National	ETSI	2.4-2.4835
Japan	MPHPT	ARIB	2.4-2.497

Table 9: Wi-Fi Regulatory compliance

6 Wi-Fi Shutdown

The Wi-Fi module shutdown pin is controlled by pin 4 of WiSmart™ module. This pin should be connected to the voltage regulator (if any) supplying pins 50 & 51 of the module. The SHUTDOWN pin is active low, so it should be set high during normal operation. Pulling the SHUTDOWN pin low sets Wi-Fi chip in Shutdown mode. This turns OFF most parts of the circuit and minimizes the current consumption. All I/O interface pins are set to predefined states (high, low or high-z) when in Shutdown mode.

IT IS STRONGLY RECOMMENDED
TO LEAVE THE SHUTDOWN FUNCTION TO BE CONTROLLED BY libwismart
AND USE ONLY THE PROVIDED libwismart API
TO TURN ON/OFF THE Wi-Fi

7 WiSmart™ EC32Lxx pad Assignments

EC32Lxx is a surface mounted module. It has 55 pads to be soldered on the carrying motherboard. The assignment of those pads, the default and alternate functions is described in Table 10.

Pad	Pad Name	Type	Main function (after reset)	Default/Alternate function(s)
1	VSSA	S	GND	
2	VSSA	S	GND	
3	VDDA	S	Power Input 3.3V	
4(2)	PB5(2)	I/O	PB5	I2C1_SMBA / SPI3_MOSI / I2S3_SD (see Note (2))
5	PB8	I/O	PB8	TIM4_CH3 / SDIO_D4
6	PB9	I/O	PB9	TIM4_CH4 / SDIO_D5
7	BOOT0	I	BOOT0	
8	SDA	I/O	PB7	I2C1_SDA / FSMC_NADV / TIM4_CH2
9	SCL	I/O	PB6	I2C1_SCL / TIM4_CH1
10	VBAT	S	VBAT	
11	TAMPER	I/O	PC13	TAMPER_RTC
12	OSC32_OUT	I/O	PC15	OSC32_OUT
13	OSC32_IN	I/O	PC14	OSC32_IN
14	OSC_IN	I/O	OSC_IN	FSMC_D2
15	PD1	I/O	OSC_OUT	FSMC_D3
16	RST	I/O	NRST	NRST
17	PC2	I/O	PC2	ADC123_IN12
18	PA1	I/O	PA1	USART2_RTS / ADC123_IN1 / TIM5_CH2 / TIM2_CH2
19	VSSA	S	GND	
20	PA8	I	PA8	USART1_CK / M1_CH1 / MCO
21	PA4	I/O	PA4	SPI1_NSS / USART2_CK / DAC_OUT1 / ADC12_IN4
22	WKUP	I/O	PA0	WKUP / USART2_CTS / ADC123_IN0 / TIM2_CH1_ETR / TIM5_CH1 / TIM8_ETR
23	USART2_TX	I/O	PA2	USART2_TX / TIM5_CH3 / ADC123_IN2 / TIM2_CH3
24	USART2_RX	I/O	PA3	USART2_RX / TIM5_CH4 / ADC123_IN3 / TIM2_CH4
25	SPI1_SCK	I/O	PA5	SPI1_SCK / DAC_OU2/ ADC12_IN5
26	SPI1_MISO	I/O	PA6	SPI1_MISO / TIM8_BKIN / ADC12_IN6 / TIM3_CH1
27	SPI1_MOSI	I/O	PA7	SPI1_MOSI / TIM8_CH1N / ADC12_IN7 / TIM3_CH2
28	BOOT1	I/O	PB2 / BOOT1	
29	PC6	I/O	PC6	I2S2_MCK / TIM8_CH1/SDIO_D6
30	JTRST	I/O	NJTRST	SPI3_MISO
31	JTDO	I	JTDO	SPI3_SCK / I2S3_CK

32	JTDI	I/O	JTDI	SPI3_NSS / I2S3_WS
33[1]	JTCK [1]	I/O	JTCK / SWCLK (see Note [1])	
34	JTMS	I/O	JTMS / SWDIO	
35	SPI2_WS	I/O	PB12	SPI2_NSS / I2S_WS /I 2C2_SMBA / USART3_CK / TIM1_BKIN
36	SPI2_SCK	I/O	PB13	SPI2_SCK / I2S2_CK / USART3_CTS / TIM1_CH1N
37	SPI2_MISO	I/O	PB14	SPI2_MISO / TIM1_CH2N / USART3_RTS
38	SPI2_MOSI	I/O	PB15	SPI2_MOSI / I2S2_SD / TIM1_CH3N
39[1]	SD_D0[1]	I/O	PC8	TIM8_CH3 / SDIO_D0 (see Note [1])
40[1]	SD_D1[1]	I/O	PC9	TIM8_CH4 / SDIO_D1 (see Note [1])
41	TXD	I/O	PA9	USART1_TX / TIM1_CH2
42	RXD	I/O	PA10	USART1_RX / TIM1_CH3
43	USBDM	I/O	PA11	USART1_CTS / USBDM / CAN_RX / TIM1_CH4
44	USBDP	I/O	PA12	USART1_RTS / USBDP / CAN_TX / TIM1_ETR
45[1]	SD_D2[1]	I/O	PC11	UART4_RX / SDIO_D3 (see Note [1])
46[1]	SD_D3[1]	I/O	PC10	UART4_TX / SDIO_D2 (see Note [1])
47[1]	SD_CLK[1]	I/O	PC12	UART5_TX / SDIO_CK (see Note [1])
48[1]	SD_CMD[1]	I/O	PD2	TIM3_ETR / UART5_RX / SDIO_CMD (see Note [1])
49	VDD	O	1.2V Output	
50	VBAT	S	Power Input 3.3V	
51	VDDIO	S	Power Input 3.3V	
52	VSSA	S	GND	
53	PB10	I/O	PB10	I2C2_SCL / USART3_TX
54	PB11	I/O	PB11	I2C2_SDA / USART3_RX
55	PC7	I/O	PC7	I2S3_MCK / TIM8_CH2 / SDIO_D7

Table 10: EC32Lxx pad assignment

Notes:

(1): **These pins are used by libwismart for the communication between MCU and Wi-Fi and should not be used or connected in any way.**

(2): **This pin is used by libwismart for enabling / disabling Wi-Fi via external regulator. The pin should not be used on the WiSmart™ SDK/Eval board. In customer board another GPIO can be used for controlling the power supply of the Wi-Fi chip.**

8 Available Interfaces

The WiSmart™ EC32Lxx exports a number of interfaces that facilitate the communication of the module with various sensors, devices and peripherals.

8.1 Available interfaces and resources per EC32Lxx model

	Baseline Series			
Part Number	**EC32L11**	**EC32L12**	**EC32L13**	**EC32L14**
Operation Temperature	-30 to +85 °C			
Voltage range	3.0 – 3.6V			
Module Type	Surface mounted module			
Physical Dimensions	34.29 x 21.59 x 3.879mm			
MCU	**STM32F103RD** ARM Cortex-M3 Max clock: 72MHz Processing power: 90 DMIPS 1.25 DMIPS/MHz (Dhrystone 2.1)	**STM32F103RE** ARM Cortex-M3 Max clock: 72MHz Processing power: 90 DMIPS 1.25 DMIPS/MHz (Dhrystone 2.1)	**STM32F103RF** ARM Cortex-M3 Max clock: 72MHz Processing power: 90 DMIPS 1.25 DMIPS/MHz (Dhrystone 2.1)	**STM32F103RG** ARM Cortex-M3 Max clock: 72MHz Processing power: 90 DMIPS 1.25 DMIPS/MHz (Dhrystone 2.1)
FLASH	384K	512K	768K	1024K
RAM	64K		96K	
FLASH available for customer application	100K	100K	150K	400K
RAM available for customer application	25K	25K	30K	30K
Available I/O interfaces **NOTE:** The pins are multiplexed and used for more than one functions each. Always consult MCU datasheet and module datasheet	**1x 4.5 Mbps USART (USART1)** with RTS/CTS support **2x 2.25 Mbps USARTs (USART2, USART3)** with RTS/CTS support **2x I2C channels** • multi-master and slave modes • standard and fast modes • 7/10-bit addressing mode • 7-bit dual addressing mode as slave **2x I2S channels** (multiplexed with SPI2 and SPI3) • 16/32 bit resolution • Audio sampling frequencies from 8 kHz to 48 kHz • Can be output to the external DAC/CODEC at 256 times the sampling frequency **3x SPIs Master/Slave** (up to 18 Mbits/s) **2x 12-bit buffered channels DAC** • two DAC converters: one for each output channel • 8-bit or 12-bit monotonic output • left or right data alignment in 12-bit mode • synchronized update capability • external triggers for conversion **3x 12-bit channels ADC** • each ADC shares up to 16 external channels • Simultaneous sample and hold • Interleaved sample and hold • Single shunt **1x Temperature sensor** • conversion range is between 2V < VDDA < 3.6V **1x USB 1.1 device interface** • USB device peripheral • compatible with the USB full-speed 12 Mbit/s **1x CAN 2.0A & B (active)** • up to 1 Mbit/s • standard frames with 11-bit identifiers • extended frames with 29-bit identifiers • 3x transmit mailboxes, 2x receive FIFOs with 3 stages • 14 scalable filter banks **1x JTAG** **25x GPIOs** • Most of the GPIO pins are shared with digital or analog alternate functions			

Table 11: interfaces and resources for EC32L1x models

	Advanced Series		
Part Number	**EC32L22**	**EC32L23**	**EC32L24**
Operation Temperature	-30 to +85 °C		
Voltage range	3.0 – 3.6V		
Module Type	Surface mounted module		
Physical Dimensions	34.29 x 21.59 x 3.879mm		
MCU	**STM32F205RE** ARM Cortex-M3 Max clock: 120MHz Processing power: 150 DMIPS 1.25 DMIPS/MHz (Dhrystone 2.1)	**STM32F205RF** ARM Cortex-M3 Max clock: 120MHz Processing power: 150 DMIPS 1.25 DMIPS/MHz (Dhrystone 2.1)	**STM32F205RG** ARM Cortex-M3 Max clock: 120MHz Processing power: 150 DMIPS 1.25 DMIPS/MHz (Dhrystone 2.1)
FLASH	512K	768K	1024K
RAM	128K		
FLASH available for customer application	100K	150K	400K
RAM available for customer application	62K		
Available I/O interfaces **NOTE:** The pins are multiplexed and used for more than one functions each. Always consult MCU datasheet and module datasheet	**1x 7.5 Mbps USART (USART1)** with RTS/CTS support **1x 7.5 Mbps UART (USART6)** noRTS/CTS support **2x 3.25 Mbps USARTs (USART2, USART3)** with RTS/CTS support **1x 3.25 Mbps UART (UART4)** no RTS/CTS support **2x I2C channels** • multi-master and slave modes • standard and fast modes • 7/10-bit addressing mode • 7-bit dual addressing mode as slave **2x I2S channels** (multiplexed with SPI2 and SPI3) • 16/32 bit resolution • Audio sampling frequencies from 8 kHz to 192 kHz • Can be output to the external DAC/CODEC at 256 times the sampling frequency **3x SPIs Master/Slave** (up to 42 Mbits/s) **3x 12-bit channels ADC** • each ADC shares up to 16 external channels • Simultaneous sample and hold • Interleaved sample and hold **2x 12-bit buffered channels DAC** • two DAC converters: one for each output channel • 8-bit or 12-bit monotonic output • left or right data alignment in 12-bit mode • synchronized update capability • external triggers for conversion **1x Temperature sensor** • conversion range is between 1.8V < VDDA < 3.6V • internally connected to the ADC1_IN16 input channel **1x USB 1.1 device interface** • USB device peripheral • compatible with the USB full-speed 12 Mbit/s **2x CAN 2.0A & B (active)** • up to 1 Mbit/s • standard frames with 11-bit identifiers • extended frames with 29-bit identifiers • 3x transmit mailboxes, 2x receive FIFOs with 3 stages • 28 scalable filter banks • 256 bytes of SRAM allocated to each CAN **1x JTAG** **25x GPIOs** • Most of the GPIO pins are shared with digital or analog alternate functions • maximum I/O toggling up to 60 MHz **1x Random number generator (RNG)** • RNG that delivers 32-bit random numbers		
Special Features	1) MPU 2) DSP with FPU 3) True random number generator (RNG) 4) ART Accelerator™ (Adaptive real-time accelerator) allowing 0-wait state execution from Flash memory 5) Dedicated PLL for audio I2S application. It allows to achieve error-free I2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.		

Table 12: interfaces and resources for EC32L2x models

	High Performance Series
Part Number	**EC32L44**
Operation Temperature	-30 to +85 °C
Voltage range	3.0 – 3.6V
Module Type	Surface mounted module
Physical Dimensions	34.29 x 21.59 x 3.879mm
MCU	**STM32F405RG** ARM Cortex-M4 Max clock: 168MHz Processing power: 210 DMIPS 1.25 DMIPS/MHz (Dhrystone 2.1)
FLASH	1024K
RAM	192K
FLASH available for customer application	400K
RAM available for customer application	126K
Available I/O interfaces **NOTE:** The pins are multiplexed and used for more than one functions each. Always consult MCU datasheet and module datasheet	**1x 10.5 Mbps USART (USART1)** with RTS/CTS support **1x 10.5 Mbps UART (USART6) no** RTS/CTS support **2x 5.25 Mbps USARTs (USART2, USART3)** with RTS/CTS support **1x 5.25 Mbps UART (UART4) no** RTS/CTS support **2x I2C channels** • multi-master and slave modes • standard and fast modes • 7/10-bit addressing mode • 7-bit dual addressing mode as slave **2x I2S channels** (multiplexed with SPI2 and SPI3) • 16/32 bit resolution • Audio sampling frequencies from 8 kHz to 192 kHz • Can be output to the external DAC/CODEC at 256 times the sampling frequency **3x SPIs Master/Slave** (up to 42 Mbits/s) **3x 12-bit channels ADC** • each ADC shares up to 16 external channels • Simultaneous sample and hold • Interleaved sample and hold **2x 12-bit buffered channels DAC** • two DAC converters: one for each output channel • 8-bit or 12-bit monotonic output • left or right data alignment in 12-bit mode • synchronized update capability • external triggers for conversion **1x Temperature sensor** • conversion range is between 1.8V < VDDA < 3.6V • internally connected to the ADC1_IN16 input channel **1x USB 1.1 device interface** • USB device peripheral • compatible with the USB full-speed 12 Mbit/s **2x CAN 2.0A & B (active)** • up to 1 Mbit/s • standard frames with 11-bit identifiers • extended frames with 29-bit identifiers • 3x transmit mailboxes, 2x receive FIFOs with 3 stages • 28 scalable filter banks • 256 bytes of SRAM allocated to each CAN **1x JTAG** **25x GPIOs** • Most of the GPIO pins are shared with digital or analog alternate functions • maximum I/O toggling up to 84 MHz **1x Random number generator (RNG)** • RNG that delivers 32-bit random numbers
Special Features	1) MPU 2) DSP with FPU 3) True random number generator (RNG) 4) ART Accelerator™ (Adaptive real-time accelerator) allowing 0-wait state execution from Flash memory 5) Dedicated PLL for audio I2S application. It allows to achieve error-free I2S sampling clock accuracy without compromising on the CPU performance, while using USB peripherals.

Table 13: interfaces and resources for EC32L44 models

IMPORTANT NOTE: **HW interfaces** of the MCU, multiplexed with the SDIO signals (which are used for the communication between MCU and Wi-Fi chip) **must not be used**.

8.2 Universal synchronous/asynchronous receiver transmitters (USARTs)

The available universal synchronous/asynchronous receiver transmitters provide asynchronous communication. They support IrDA SIR ENDEC, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

Some of the USARTs also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All can be served by the DMA controller.

Please refer to MCU Datasheet for details on HW interfaces.

8.3 I^2C Bus

There are two available I²C bus interfaces for the EC32Lxx able to operate in multi-master and slave modes.

I^2C supports standard and fast modes, 7/10-bit addressing mode and 7-bit dual addressing mode (as slave).

A hardware CRC generation/verification is embedded.

I^2C can be served by DMA and supports SMBus 2.0/PMBus.

8.4 Serial Peripheral Interface (SPI)

There are three SPIs able to communicate in slave and master modes in full-duplex and simplex communication modes.

The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits.

The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

8.5 Inter-integrated sound (I^2S)

There are two standard I^2S interface (multiplexed with SPI interfaces), that can be operated in master or slave mode.

These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

8.6 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter

banks.

8.7 Universal Serial Bus (USB)

The EC32Lxx family embed a USB device peripheral compatible with the USB full-speed 12 Mbit/s.

The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support.

The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

8.8 GPIOs (General Purpose Inputs/Outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

8.9 ADC (Analog to Digital Converter)

Three 12-bit analog-to-digital converters are embedded into WiSmart™ EC32Lxx, and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timers (TIM1 and TIM8) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

8.10 DAC (Digital to Analog Converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output

- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference VREF+

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

8.11 Temperature Sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2V < VDDA < 3.6V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

8.12 JTAG

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

9 Other Features

9.1 Nested vectored interrupt controller (NVIC)

The EC32Lxx family embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

9.2 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. All the GPIOs could be connected to the 16 external interrupt lines.

9.3 Clocks and startup

System clock selection is done during startup sequence however the internal RC oscillator is selected as default CPU clock on reset. An external clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains.

Please check the MCU datasheet for the maximum frequency of the AHB, the high speed APB domains, the maximum allowed frequency of the low speed APB domain and for details on the clock tree.

9.4 Boot Modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By

default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.

- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

The state of the B0 pin determines the boot memory to be used.

9.5 Power supply schemes

- VDDIO = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- VDD, VDDA = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). VDDA and VSSA must be connected to VDD and VSS, respectively.
- VBAT = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.

9.6 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when VDD is below a specified threshold, VPOR/PDR, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the VDD/VDDA power supply and compares it to the VPVD threshold. An interrupt can be generated when VDD/VDDA drops below the VPVD threshold and/or when VDD/VDDA is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

9.7 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

9.8 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger

on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced-control timers TIMx, DAC, I^2S, SDIO and ADC.

9.9 RTC

The RTC and the backup registers are supplied through a switch that takes power either on VDD supply when present or through the VBAT pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

IMPORTANT NOTE: *The RTC cannot be used by customer application. Customer application should use the timers API provided by ECONAIS library*

9.10 Timers and watchdogs

The EC32Lxx family includes up to two advanced-control timers, up to four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer. The following table compares the features of the advanced-control, general-purpose and basic timers.

9.10.1 High-density timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture / Compare channels	Complementary outputs
TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM6,	16-bit	Up	Any integer	Yes	0	No

TIM7			between 1 and 65536			

Table 14: Timer feature comparison

9.10.2 Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

9.10.3 General-purpose timers (TIMx)

There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the EC32Lxx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

9.10.3.1 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

9.10.3.2 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device

when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

9.10.3.3 Window watchdog

The window watchdog is based on a 7-bit down-counter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

9.10.3.4 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto-reload capability
- Maskable system interrupts generation when the counter reaches 0.
- Programmable clock source

10 Schematics

NOTE: The schematics are also provided in separate high resolution files (EC32Lxx_Schematics.pdf)

10.1 EC32Lxx schematics

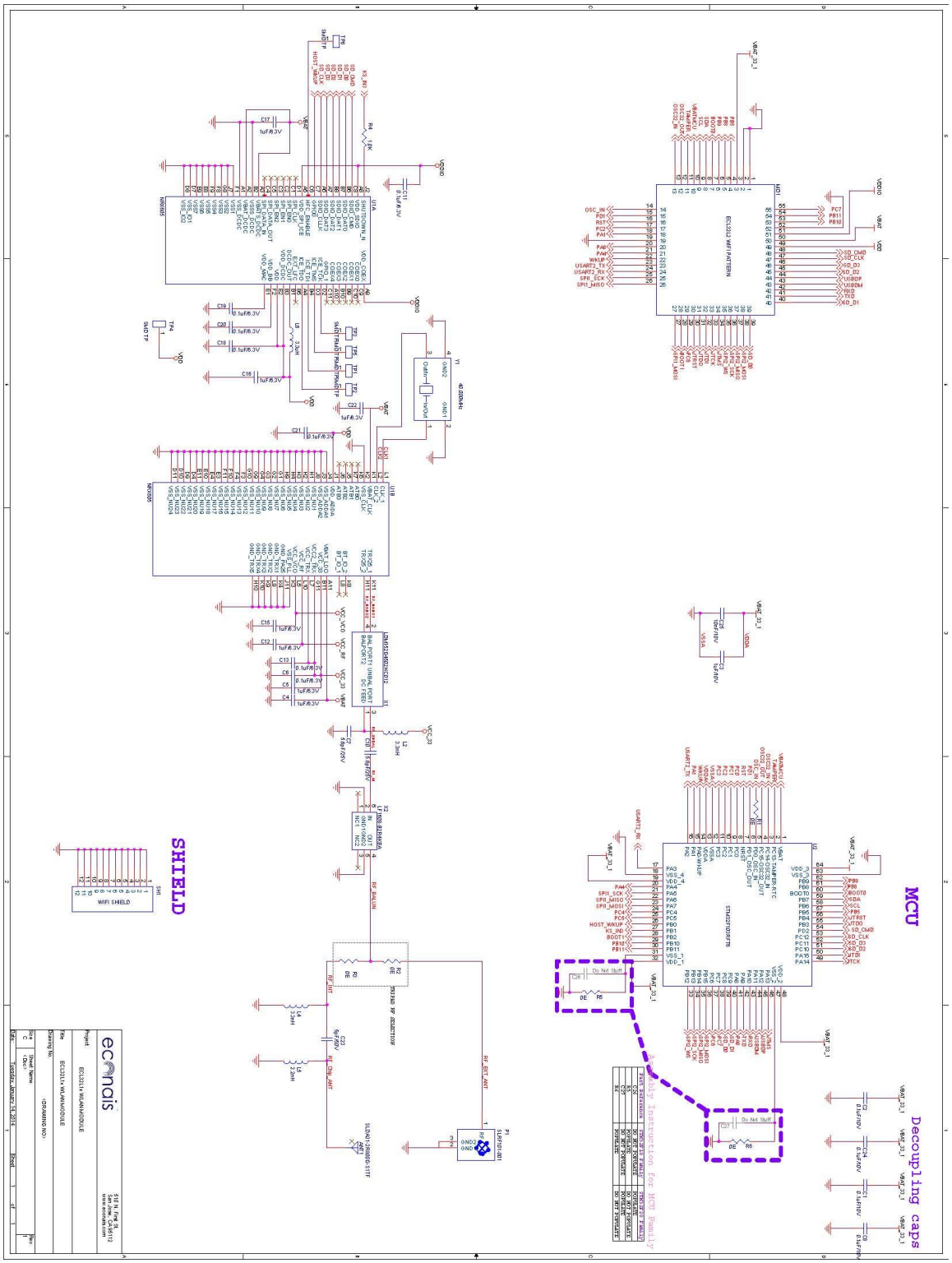


Figure 1 EC32L1x schematics

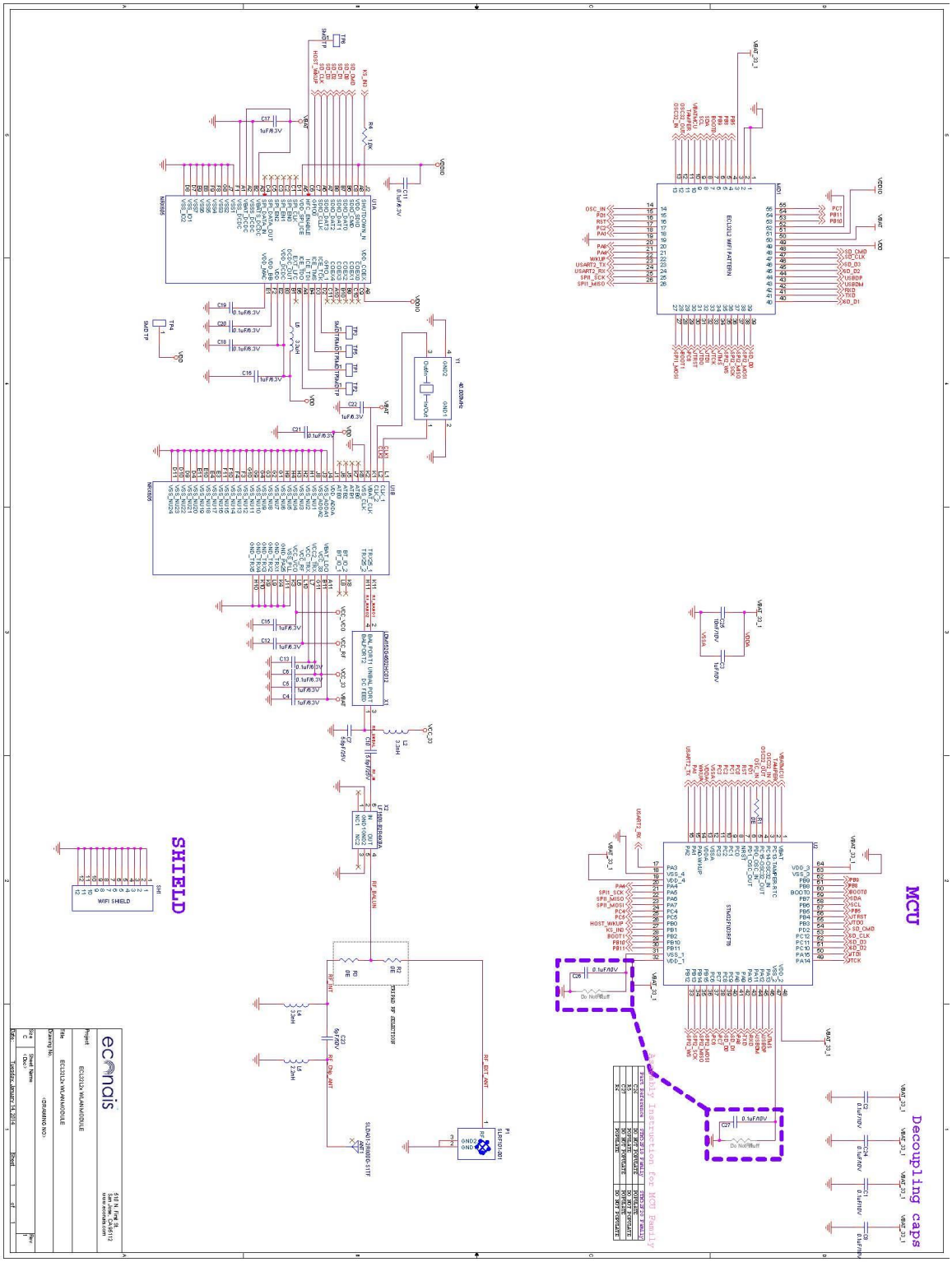


Figure 2: EC32L2x Schematics

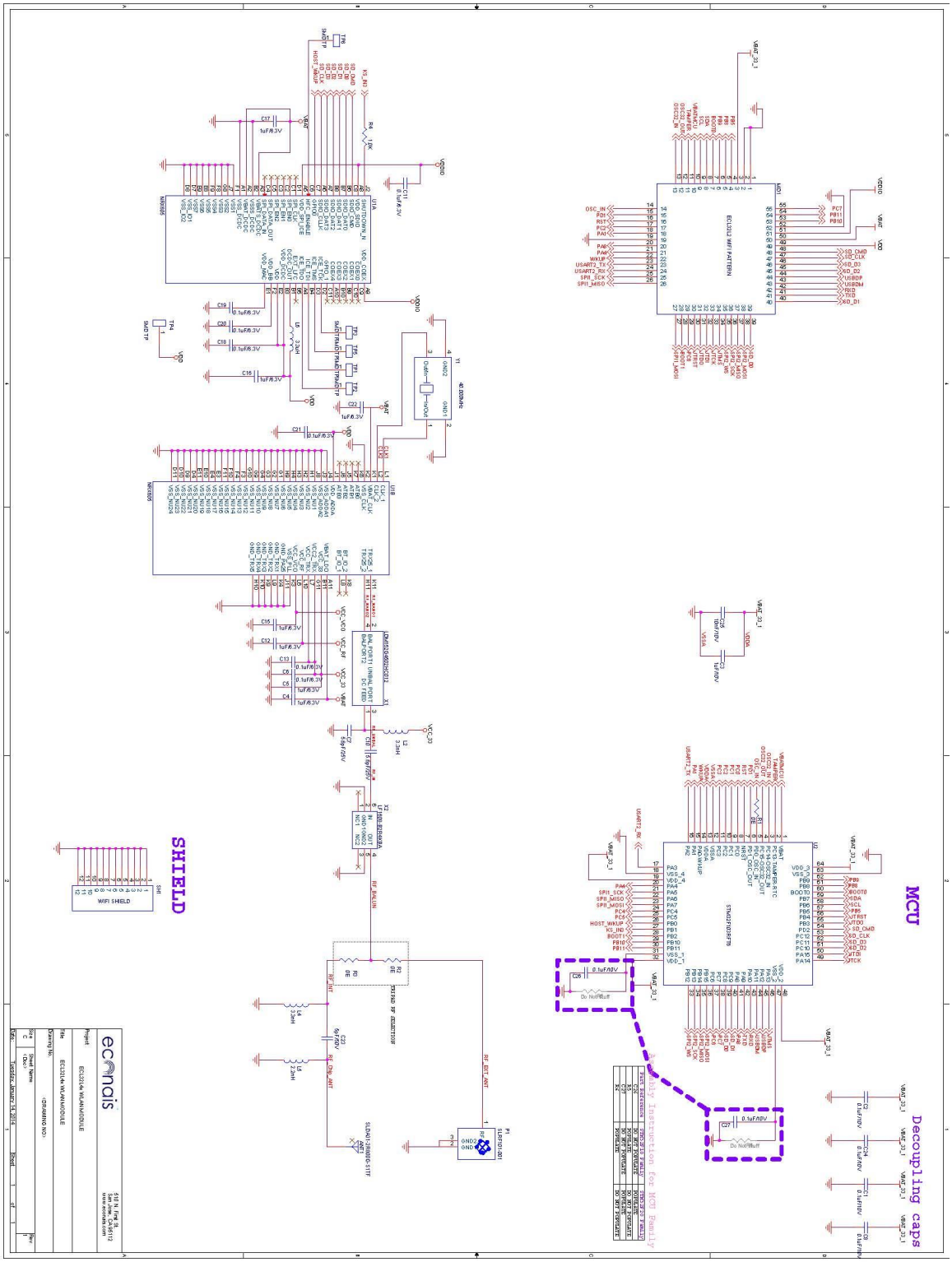


Figure 3: EC32L44 schematics

11 Mechanical Dimensions

The EC32Lxx WiSmart™ is a surface mountable module of size LxWxH = 34.29mm x 21.59mm x 3.89mm (including the shield). The tolerance of the length/width is ±0.2mm. The module Printed Circuit Board is 1.5mm thick with castellated mounting points around it. The EC32Lxx physical dimensions information is shown in details in Figure 4: EC32Lxx Mechanical dimensions.

NOTE: *All dimensions are in inches (and in millimeters in square brackets [MM])*

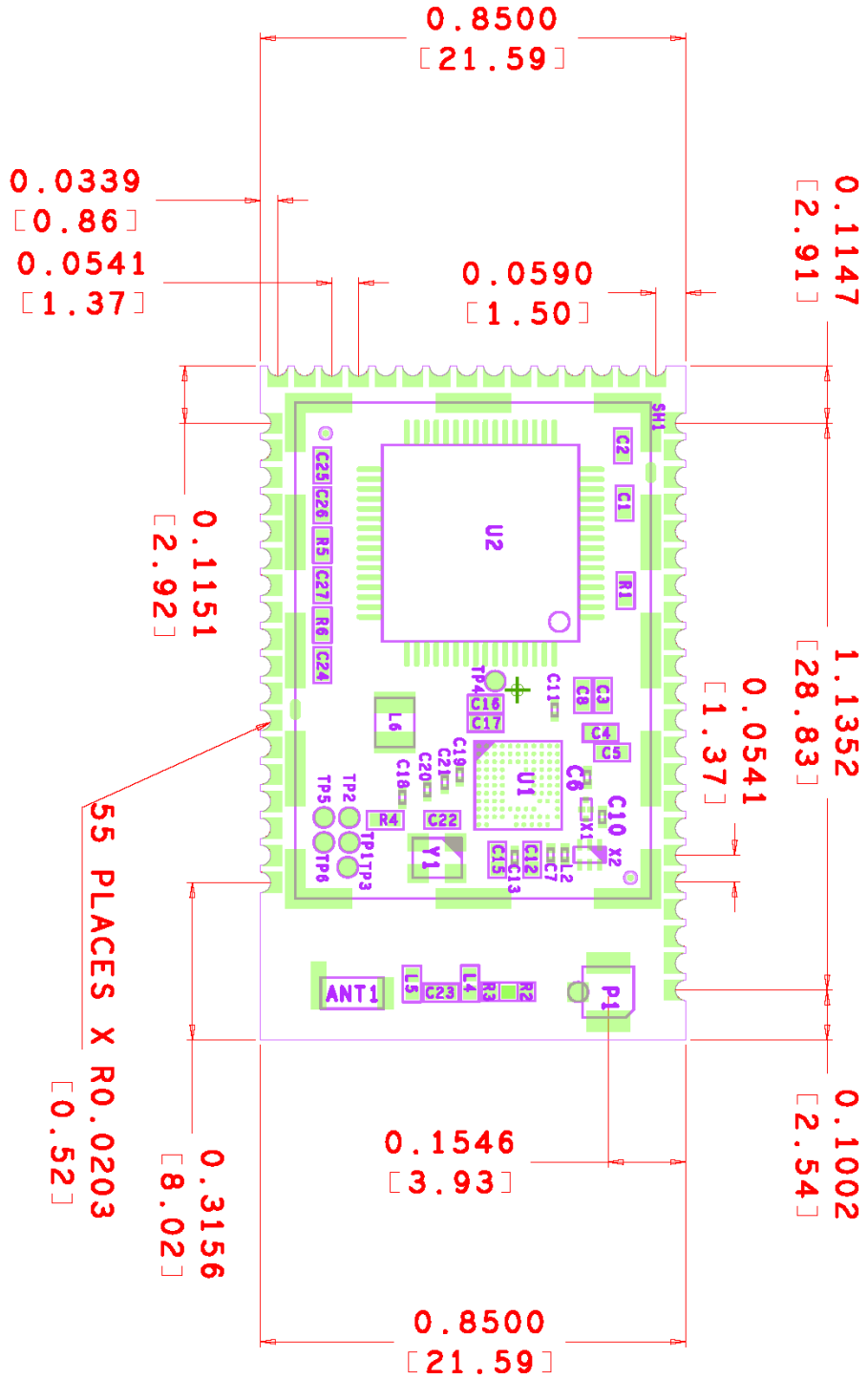


Figure 4: EC32Lxx Mechanical dimensions

12 Pad Diagram

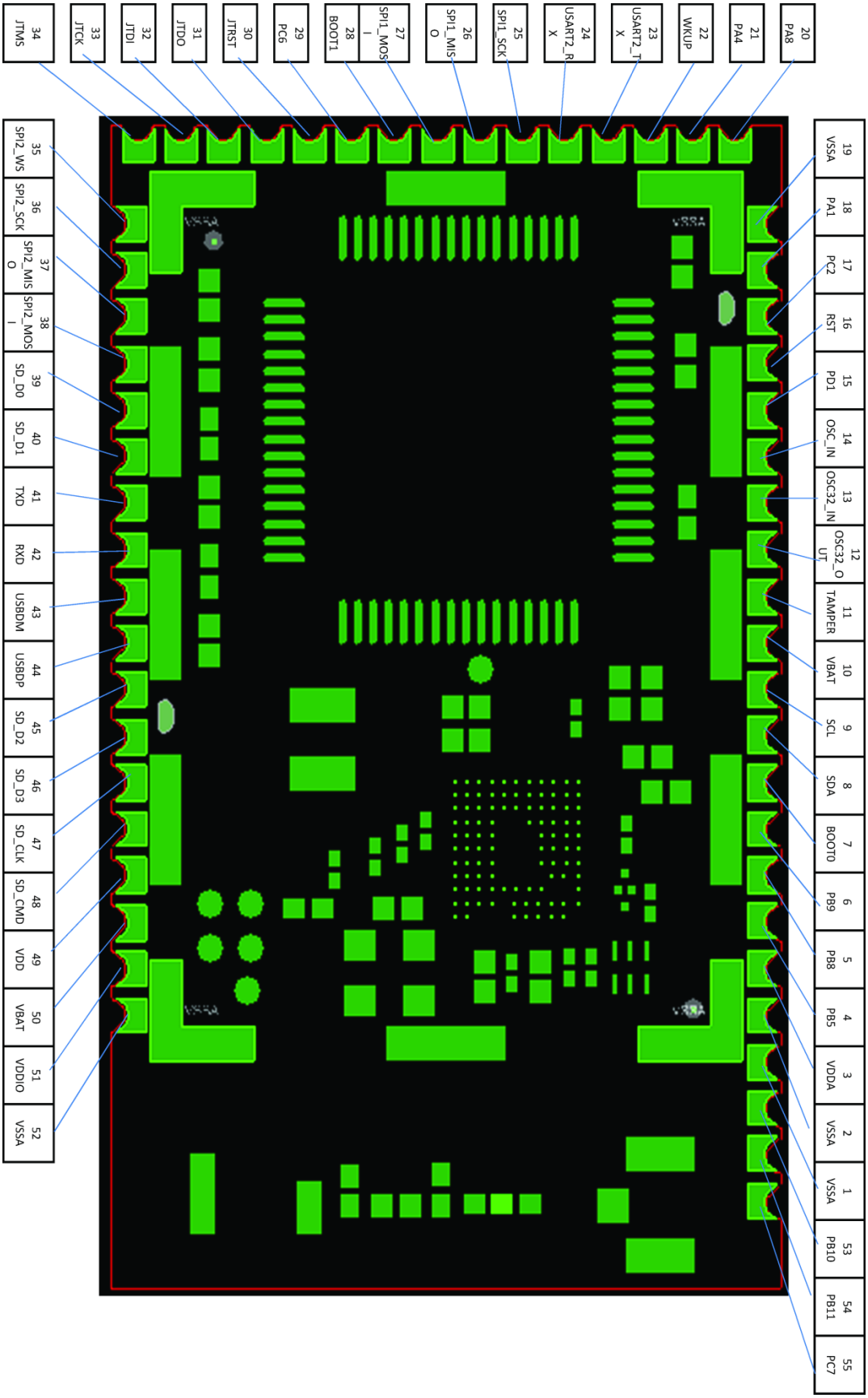


Figure 5: PADs diagram

13 Footprint recommendation

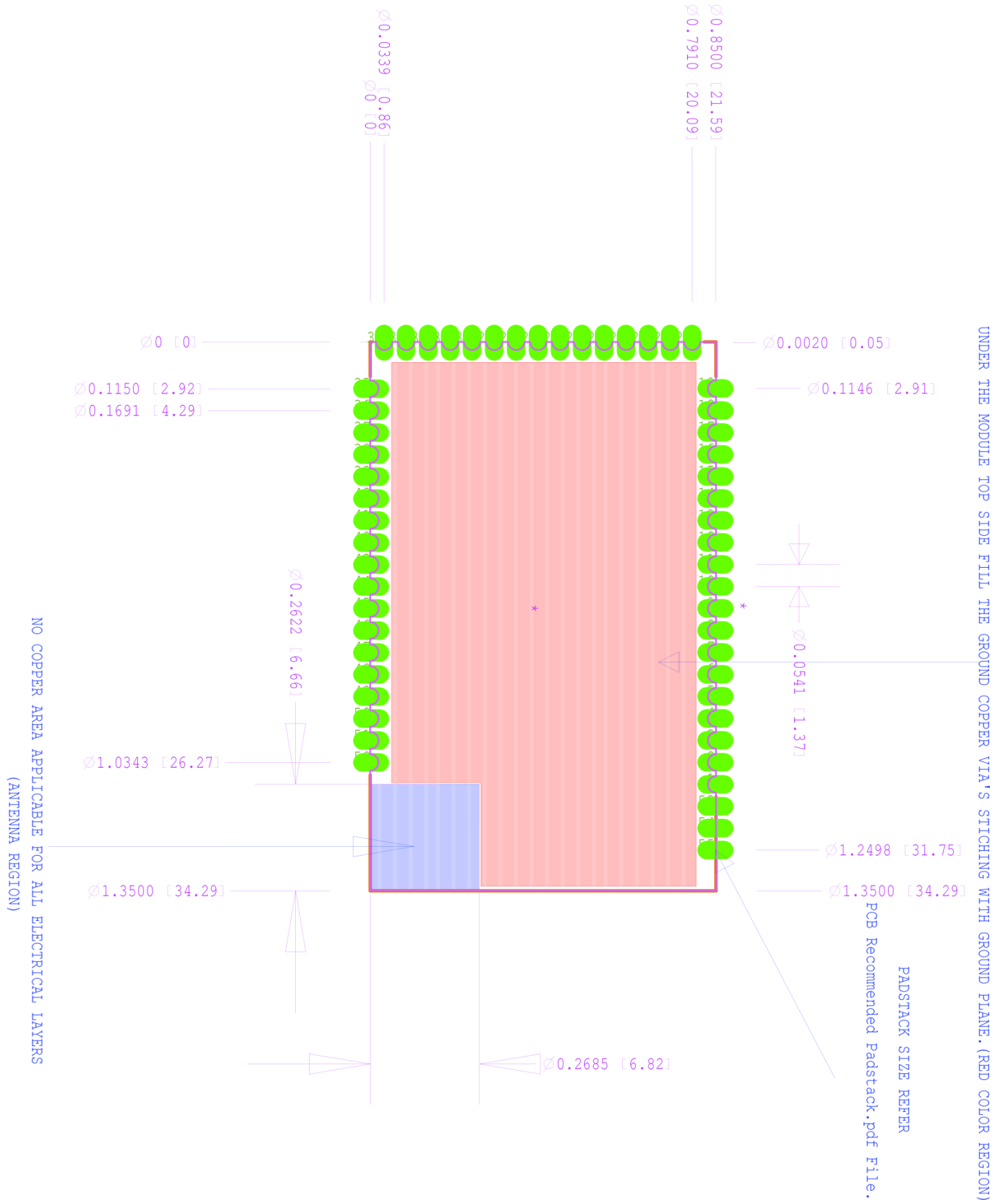


Figure 6: EC32Lxx Footprint recommendation

14 Motherboard Pads recommendation

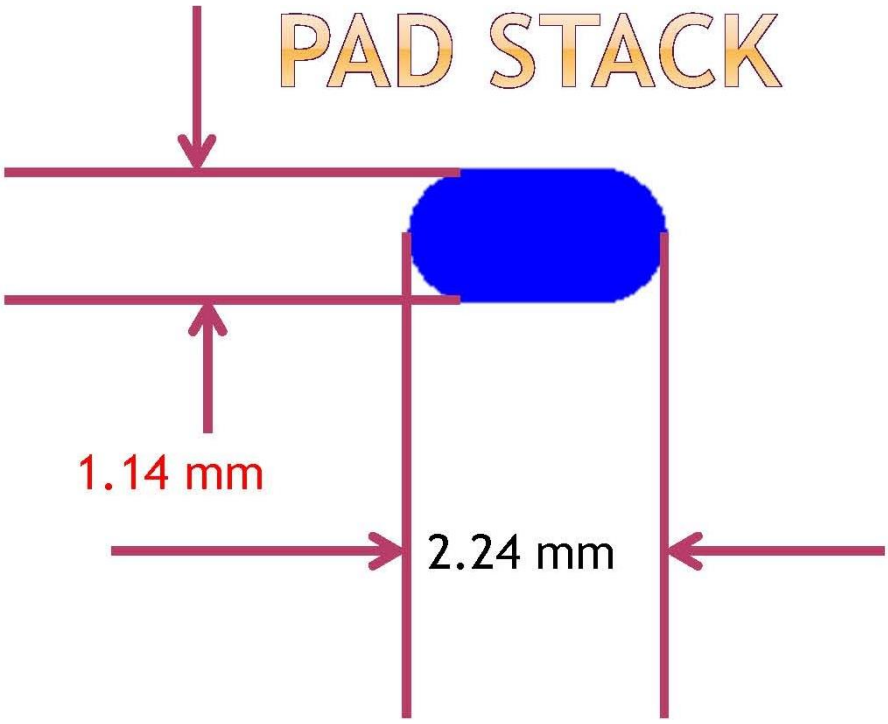
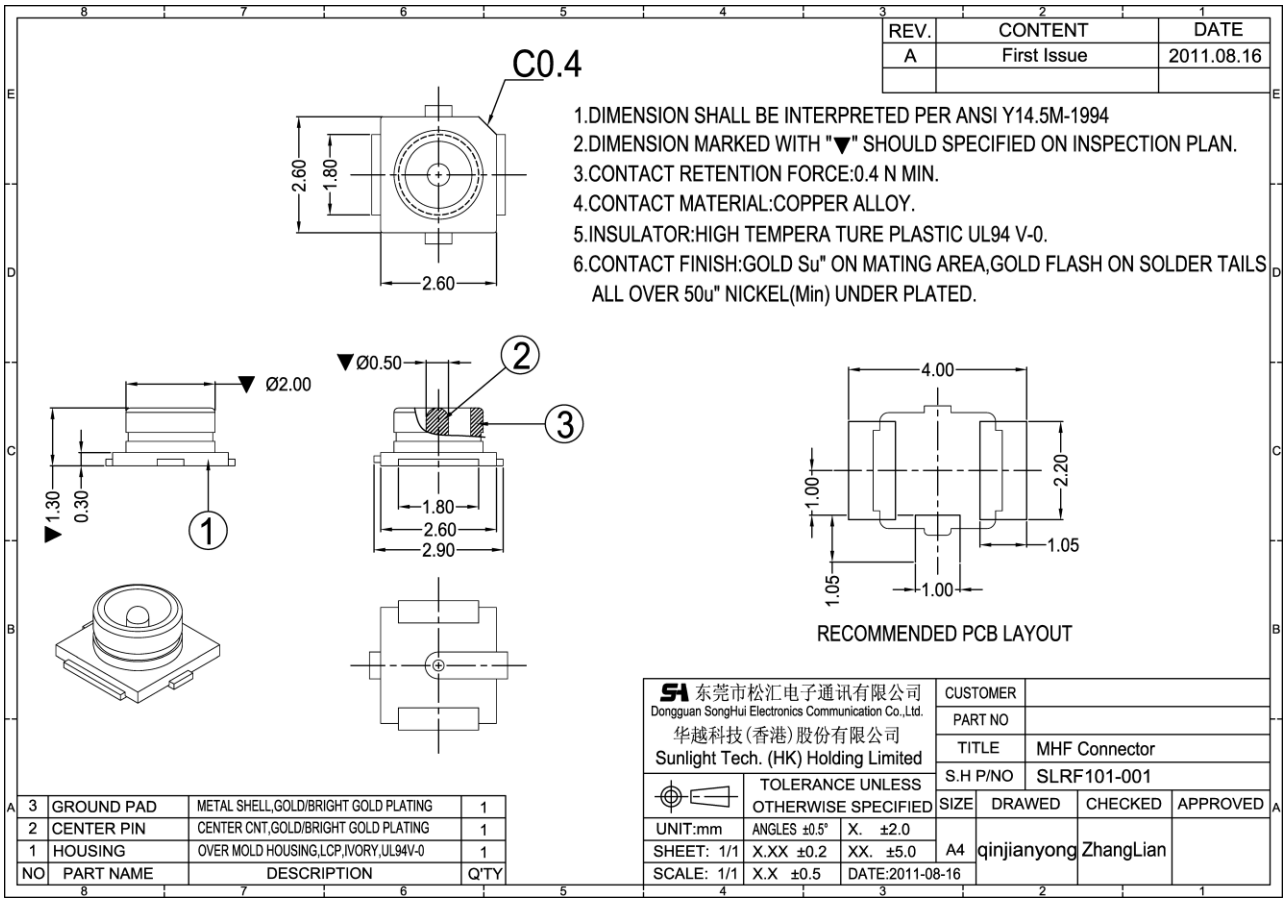


Figure 7: Motherboard PAD stack information

15 External Antenna connector information



The external antenna MHF connector manufacturer is Sunlight Tech in Hong Kong. The MHF connector part number is SLRF 101-001.

16 Connection Diagram – Reference Design Schematic

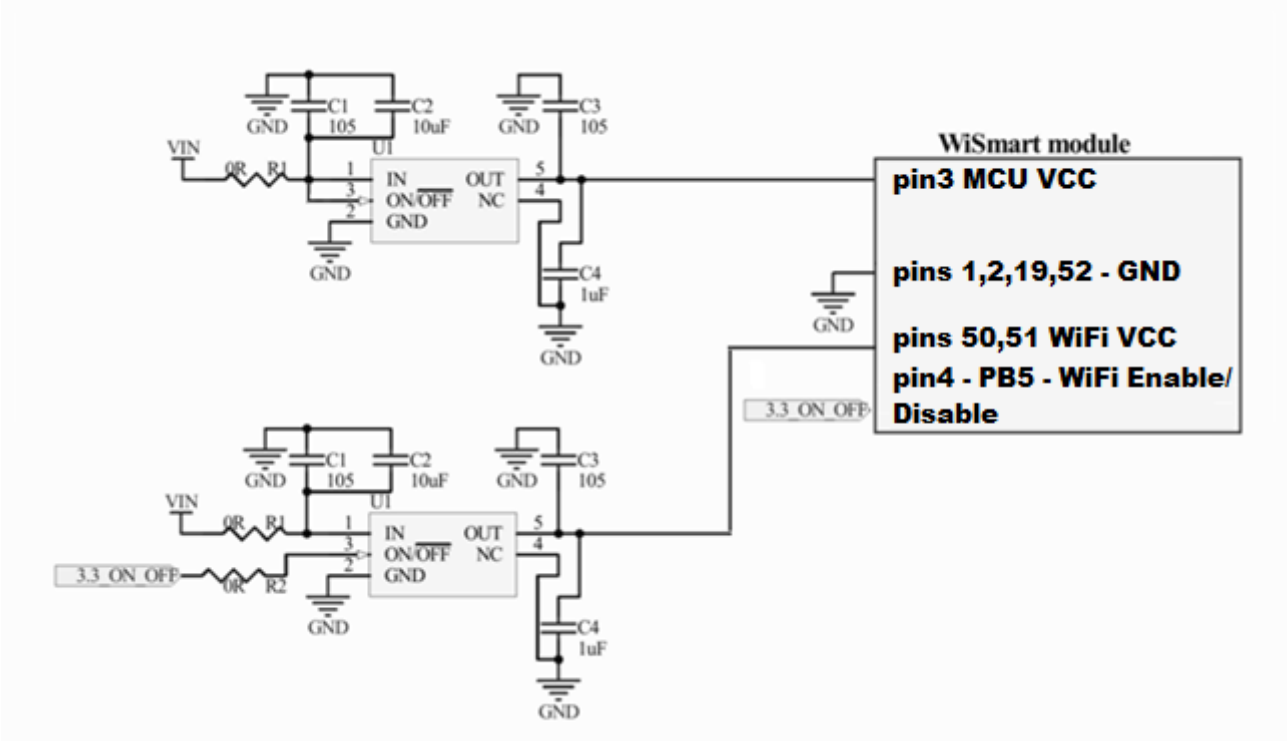


Figure 8: WiSmart power supply

The two ICs in Figure 8 are ultra-low dropdown voltage regulators, with output fixed voltage to 3.3V.

Pin 4 of the EC32Lxx WiSmart™ module is dedicated to Enable/Disable Wi-Fi **and should not be used by the customer application after reset**.

The regulators should both be capable of handling at least 289.5 mA of power.

17 Power save modes, wake-up times and power consumption

All members of WiSmart™ family of modules have implemented advanced algorithms of power save and power management for both MCU and Wi-Fi.

The Wi-Fi power save is controlled exclusively by the libwismart library and the customer can only turn ON/OF the total Wi-Fi subsystem.

The WiSmart power modes, the wake-up time from each of them and their descriptions are as shown in Table 15.

WiSmart power mode	Wake-up time	Description
NO POWER SAVE		**No power save** MCU runs always at full speed. No power save mechanism is used. In this mode the device has very fast reactions and fast threads switching achieving the highest possible performance. CPU and all Peripherals are always on. Wi-Fi connectivity is sustained.
NORMAL POWER SAVE	2 uS	**Normal level of power save** The CPU starts and stops automatically when needed according to the algorithm implemented in the libwismart library. All the peripherals are always ON and the only component that is going to sleep mode is the CPU. The device will wake-up from internal or external events/IRQs or the RTC trigger or on incoming Wi-Fi traffic. Wi-Fi connectivity is sustained.
HIGH POWER SAVE	20 uS	**High level of power save** The CPU starts and stops automatically when needed according to the algorithm implemented in the libwismart library. Peripherals are disabled and DMA is stopped The device will wake-up only from external IRQs or the RTC trigger or on incoming Wi-Fi traffic. Wi-Fi connectivity is sustained. **In this mode RTC cannot used by customer application as Calendar**
OFF		**Device not running** MCU is stopped and no code is executed. Wi-Fi is powered-off. The device will wake-up and resume operation only from an external IRQs or the RTC module. After wake-up the system is in reset state. This means that the full boot sequence will run including Wi-Fi initialization. After resuming operation the device will restore Wi-Fi and TCP socket connections automatically Wi-Fi connectivity is not sustained. **In this mode RTC cannot used by customer application**

Table 15: MCU power save levels

Wake-up time is the time from the wake event to the moment of the execution of the first command at the MCU.

IMPORTANT NOTE: ***From the application should be used the provided libwismart API to select the desired level of device power state and not try to control MCU directly.***

17.1 Expected EC32L1x baseline models power consumption

Test conditions and assumptions:

- The measurements are performed having the EC32L13 module mounted on the WiSmart SDK board.
- Real world environment of an average office with Wi-Fi networks in the area.
- The power consumption includes the complete module (MCU+Wi-Fi chip)
- Max Wi-Fi TX output power is used (+17dBm).
- Use of encryption or not does not affect power consumption
- TCP traffic is used which is the case in most of real world applications → An overhead of 10% or even more in lower rates compared to UDP:
    - In the RX TCP traffic there are also TX packets for acknowledgements
    - In the TX TCP traffic there are also RX packets for acknowledgements
- The power consumption is related to throughput.
- "iperf" is used in the WiSmart™ and on a PC to generate traffic and measure power consumption of complete system (not Wi-Fi only)

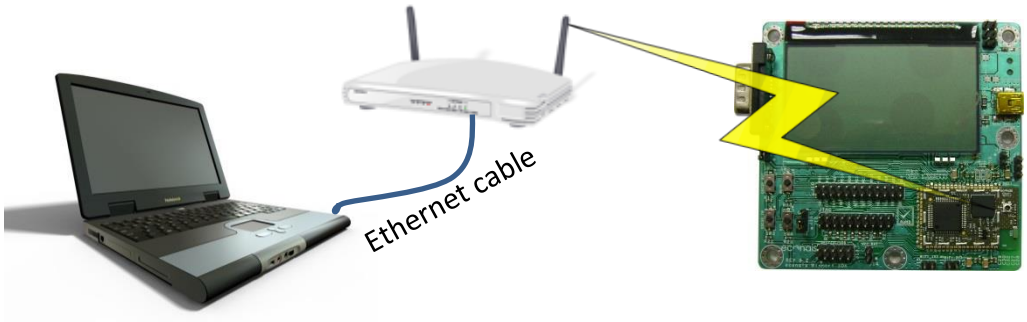


Figure 9: Power measurement setup

Table 14 shows the power consumption of the WiSmart™ with the iperf added to the Serial to Wi-Fi code in the environment described above.

All the values in table 14 are in mA.

The TCP network traffic expresses the amount of data transmitted or received within the period of one second.

The highest possible Wi-Fi link speed is automatically selected by the Wi-Fi chip for every transmission.

TCP network traffic	Power in mA @ 3.3V	
	RX	TX
Idle (Connected to Wi-Fi, no network traffic)	2,3	
1 kbps	6,4	6,5
2 kbps	6,4	6,8
3 kbps	6,4	6,8
4kbps	6,4	6,9
5 kbps	6,4	7,0
10 kbps	6,4	7,2
100 kbps	7,2	11,7
500 kbps	8,6	20,2
1 Mbps	12,6	35,2
2 Mbps	21,8	61,1
3 Mbps	42,3	90,4
4 Mbps	52,1	104,2
5 Mbps	61,3	110,3
6 Mbps	71,1	120,9
9 Mbps	89,6	134,4
MAX (PS) RX:15,9 Mbps TX: 9,7 Mbps	124,7	149,3
MAX (no PS) RX: 17,6 Mbps TX: 9,7 Mbps	134,8	149,6

Table 16: Power consumption vs TCP network traffic load, values are in mA

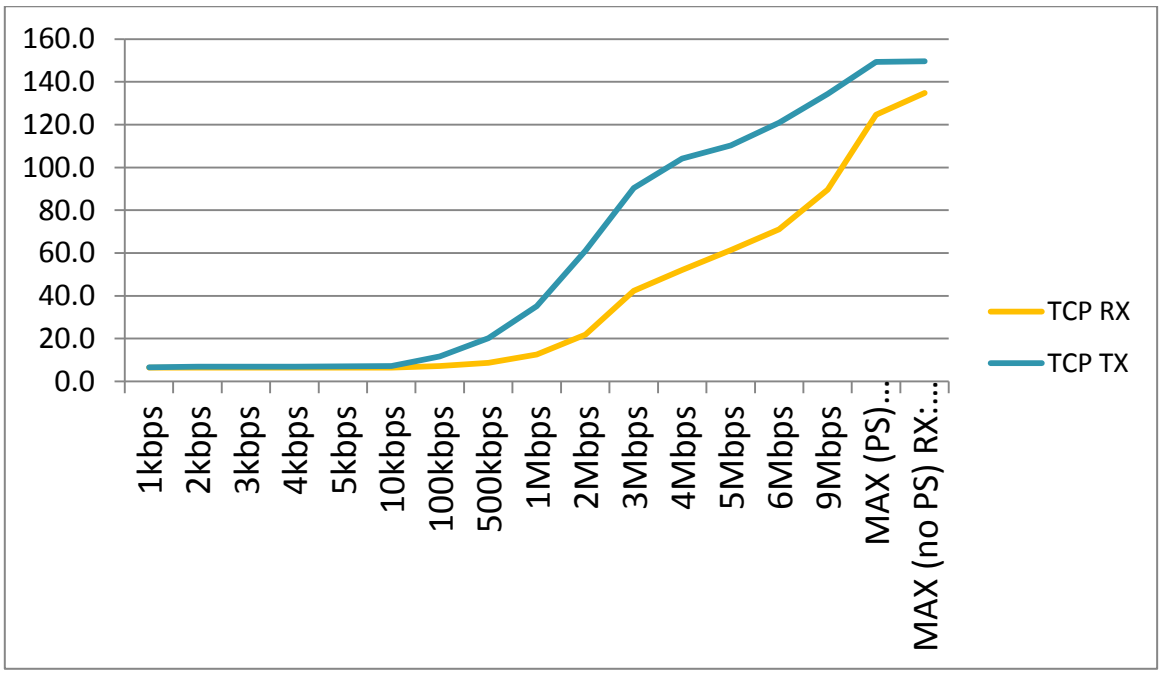


Figure 10: Power consumption vs TCP network traffic load diagram

18 Certifications

FCC ID: S67WSDE-670GN

IC ID: 11069A-WSDE670GN

CE ID: L350347L199

The EC32Lxx is compliant to the following standards:

- IEC 60950-1: 2005 (2nd Edition) Am 1:2009
- EN 60905-1:2006+A11:2009+A1:2010+A12:2011
- EN 300 328 V1.8.1 (2012-06)
- EN 301 489-1 V1.9.2 (2011.09)
- EN 301 489-17 V2.2.1 (2012-09)
- EN 62311:2008
- FCC Part 15, Subpart B, Class B
- 47 CFR FCC Part 15.247
- Canada Standard ICES-003 Issue 5
- ANSI C63.4:2003
- RSS-210 Issue 8 December 2010

19 References

- STM32F103xC, STM32F103xD, STM32F103xE Microcontroller Datasheet (Doc ID: 14611 Rev 8)
- STM32F103xF, STM32F103xG Microcontroller Datasheet (Doc ID 16554 Rev 3)
- RM0008, Reference manual for STM32F101xx, STM32F102xx, STM32F103xx, STM32F105xx and STM32F107xx advanced ARM-based 32-bit MCUs (Doc ID 13902 Rev 14)

20 Revision History

Rev	Date	Comments
1	20 Sep 2012	First issue (Preliminary version)
2	9 Apr 2013	Added information (Preliminary version)
3	15 Apr 2013	More detailed footprint information added
4	12 May 2013	Motherboard pad recommendation info added
5	14 May 2013	Typos correction
6	16 May 2013	Added information for operation voltage at -30^{o}C Added external antenna connector information
7	15 July 2013	Corrected pad #43 & #44 information Updated information on Power Consumption Added power-up sequence information
8	15 Jan 2014	Updates, typos
9	4 Mar 2014	Corrected names in pad assignment table
10	31-March-2014	Added characteristics tables per module
11	13-May-2014	Operational Temperature range clarification

Table 17: Revision history

21 ERRATA

1. There is a known issue with some AP/Routers with specific chipsets in 802.11n mode with which the WiSmart™ has lower performance by about 10%. For these cases is recommended to operate the WiSmart™ in 802.11b/g mode for maximum performance.
2. The VBAT pin of the MCU (pin 10 of the module) is by mistake connected internally to the Wi-Fi VBAT pin (pin 50 of the module). This would prevent the VBAT of the MCU to be supplied when the Wi-Fi part is powered off.

22 Contact Information

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