PIC18F6520/8520

PIC18F6520/8520 Rev. A1 Silicon/Data Sheet Errata

The PIC18F6520/8520 Rev. A1 parts you have received conform functionally to the Device Data Sheet (DS39609**B**), except for the anomalies described below.

All the issues listed here will be addressed in future revisions of the PIC18F6520/8520 silicon.

The following silicon errata apply only to PIC18F6520/8520 devices with these Device/ Revision IDs:

Part Number	Device ID	Revision ID
PIC18F6520	00 1011 001	00001
PIC18F8520	00 1011 000	00001

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: I/O Ports (Parallel Slave Port)

While operating in Parallel Slave Port mode, the OBF bit (PSPCON<6>) is supposed to be set when a byte is written to either PORTD or LATD. It has been noted that OBF may not be correctly set when a byte is written to LATD. If the byte is written to PORTD, then the OBF bit is set correctly.

Work around

To ensure the OBF bit is set correctly, write to PORTD rather than LATD.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Core (`DAW` Instruction)

The `DAW` instruction may improperly clear the Carry bit (STATUS<0>) when executed.

Work around

Test the Carry bit state before executing the `DAW` instruction. If the Carry bit is set, increment the next higher byte to be added using an instruction such as `INCFSZ` (this instruction does not affect any Status flags and will not overflow a BCD nibble). After the `DAW` instruction has been executed, process the Carry bit normally (see Example 1).

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 1: PROCESSING THE CARRY BIT DURING BCD ADDITIONS

```
MOVLW   0x80        ; .80 (BCD)
ADDLW   0x80        ; .80 (BCD)

BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB
DAW
BTFSC   STATUS, C   ; test C
INCFSZ  byte2       ; inc next higher LSB

This is repeated for each DAW instruction
```

3. Module: External Memory Bus

When performing writes on the external memory interface, a short glitch is present on the $\overline{LB}$ and $\overline{UB}$ lines. The length of the glitch is proportional to FOSC and also may vary with process, voltage and temperature. The glitch occurs well before the $\overline{WRH}$ line is asserted and no adverse affect on the operation of the external memory interface has been observed.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: USART

Writing to the USART TXREGx, faster than the baud rate in Synchronous mode, will overwrite the previous value instead of double-buffering as in Asynchronous mode.

Work around

Load the first character into TXREGx and then wait for a TXx interrupt, or check the TXxIF bit before writing each additional character to TXREGx.

Date Codes that pertain to this issue:

All engineering and production devices.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39609**B**), the following clarifications and corrections should be noted.

1. Module: Table 23-1: Configuration Bits and Device IDs

In **Section 23.0 "Special Features of the CPU"**, Table 23-1 has been updated. Information in Note 3 has been changed and all changes are noted with **bold** text.

TABLE 23-1: CONFIGURATION BITS AND DEVICE IDS

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	—	—	$\overline{\text{OSCSEN}}$	—	—	FOSC2	FOSC1	FOSC0	--1- -111
300002h	CONFIG2L	—	—	—	—	BORV1	BORV0	BODEN	$\overline{\text{PWRTEN}}$	---- 1111
300003h	CONFIG2H	—	—	—	—	WDTPS2	WDTPS1	WDTPS0	WDTEN	---- 1111
300004h(1)	CONFIG3L	WAIT	—	—	—	—	—	PM1	PM0	1--- --11
300005h	CONFIG3H	—	—	—	—	—	—	**r**(3)	CCP2MX	---- --**x**1
300006h	CONFIG4L	$\overline{\text{DEBUG}}$	—	—	—	—	LVP	—	STVREN	1--- -1-1
300008h	CONFIG5L	CP7(2)	CP6(2)	CP5(2)	CP4(2)	CP3	CP2	CP1	CP0	1111 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	WRT7(2)	WRT6(2)	WRT5(2)	WRT4(2)	WRT3	WRT2	WRT1	WRT0	1111 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	EBTR7(2)	EBTR6(2)	EBTR5(2)	EBTR4(2)	EBTR3	EBTR2	EBTR1	EBTR0	1111 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	**(Note 4)**
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 0110

Legend: x = unknown, u = unchanged, — = unimplemented, q = value depends on condition, **r = reserved**. Shaded cells are unimplemented, read as '0'.

Note 1: Unimplemented in PIC18F6X20 devices**, read as '0'.**
2: Unimplemented in PIC18FX520 and PIC18FX620 devices**, read as '0'.**
3: **Unimplemented in PIC18FX620 and PIC18FX720 devices, read as '0'.**
4: See Register 23-13 for DEVID1 values.

2. Module: DC Characteristics

In **Section 26.2 "DC Characteristics: Power-Down and Supply Current"**, the specifications and conditions for parameters D025 and D026 have been changed (changes are shown in **bold** text).

26.2 DC Characteristics: Power-Down and Supply Current PIC18F6520/8520 (Industrial, Extended) PIC18LF6520/8520 (Industrial)

PIC18LFXX20 (Industrial)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18FXX20 (Industrial, Extended)		**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
D025 (ΔIOSCB)	**Timer1 Oscillator** PIC18F8520/8620	6.5	40	µA	+25°C	VDD = 4.2V	32 kHz on Timer1
		6.5	50	µA	-40°C to +85°C		
		6.5	65	µA	-40°C to +125°C		
	PIC18LF6520/8520	**2.1**	**4.0**	**µA**	**-40°C**	**VDD = 2.0V**	**32 kHz on Timer1**
		1.8	**4.0**	**µA**	**+25°C**		
		2.1	**8.0**	**µA**	**+85°C**		
		2.2	**10**	**µA**	**-40°C**	**VDD = 3.0V**	**32 kHz on Timer1**
		2.6	**10**	**µA**	**+25°C**		
		2.9	**15**	**µA**	**+85°C**		
D026 (ΔIAD)	**A/D Converter**	<1	2	µA	**-40°C to +85°C**	VDD = 2.0V	A/D on, not converting. Device is in Sleep.
		<1	2	µA	**-40°C to +85°C**	VDD = 3.0V	
		<1	2	µA	**-40°C to +85°C**	VDD = 5.0V	
		<1	**8**	**µA**	**-40°C to +125°C**	**VDD = 5.0V**	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;

MCLR = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

3. Module: Table 26-4: Memory Programming Requirements

In **Section 26.0 "Electrical Characteristics"**, Table 26-4: Memory Programming Requirements, parameter D124 has been added and parameters D123A and D134A have been removed. Typical values for D123 and D134 have changed. Changes to the table are shown in **bold** text.

TABLE 26-4: MEMORY PROGRAMMING REQUIREMENTS

DC Characteristics			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Data EEPROM Memory					
D123	TRETD	Characteristic Retention	40	**100**	—	Year	-40°C to +85°C **(Note 3)**
D124	**TREF**	**Number of Total Erase/Write Cycles before Refresh**	**1M** **10K**	**10M** **1M**	**—** **—**	**E/W** **E/W**	**-40°C to +85°C (Note 4)** **-40°C to +125°C (Note 4)**
D132B	VPEW	**VDD for Self-Timed Write or Row Erase**	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D134	TRETD	Characteristic Retention	40	**100**	—	Year	-40°C to +85°C **(Note 3)**

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications are for programming the on-chip program memory through the use of table write instructions.

2: The pin may be kept in this range at times other than programming, but it is not recommended.

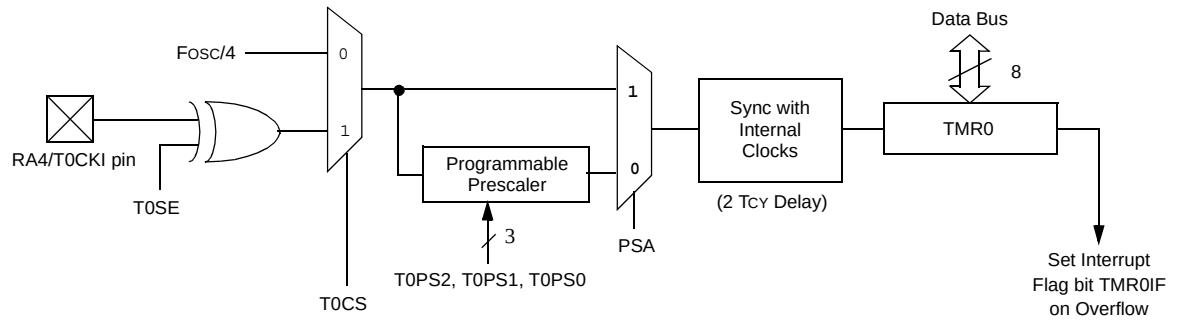
3: Retention time is valid, provided no other specifications are violated.

4: **Refer to Section 7.8 "Using the Data EEPROM" for a more detailed discussion on data EEPROM endurance.**

4. Module: Timer0 Block Diagrams

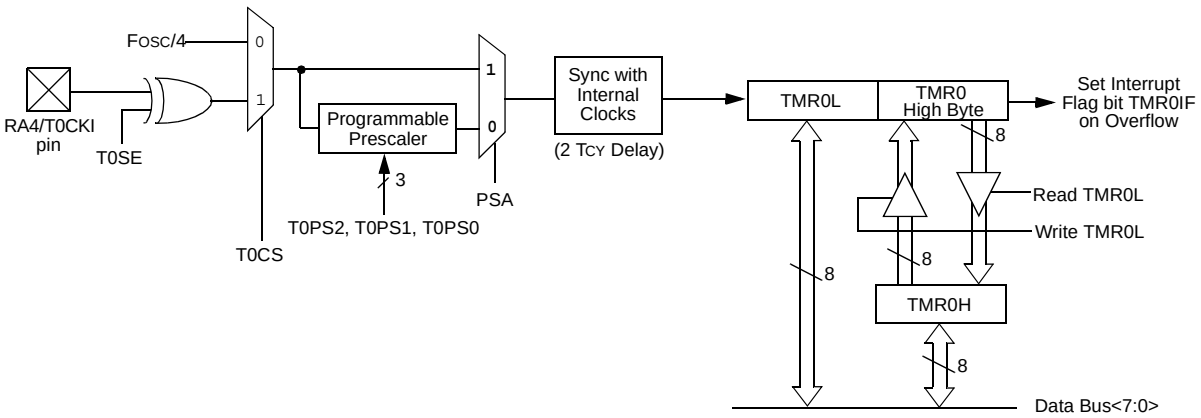
In Figure 11-1 and Figure 11-2 of the Device Data Sheet, the Timer0 Prescaler Assignment (PSA) bits are incorrectly stated. To remedy this, the bit values have been swapped as shown in the figures below.

FIGURE 11-1: TIMER0 BLOCK DIAGRAM IN 8-BIT MODE



Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

FIGURE 11-2: TIMER0 BLOCK DIAGRAM IN 16-BIT MODE



Note: Upon Reset, Timer0 is enabled in 8-bit mode with clock input from T0CKI max. prescale.

5. Module: DC Characteristics (VDD Specifications)

The PIC18LFX520 VDD (parameter D001) specifications listed in **Section 26.1 "DC Characteristics: Supply Voltage"** of the Device Data Sheet have been changed.

The following table shows the current test limits (modified values are shown in **bold**).

26.1 DC Characteristics: Supply Voltage PIC18F6520/8520 (Industrial, Extended) PIC18LF6520/8520 (Industrial)

PIC18LF6520/8520/6620/8620/6720/8720 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F6520/8520 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**					
		PIC18LFX520	**2.0**	**—**	**3.3**	**V**	**Timer1 oscillator enabled**
		PIC18LFX520	**2.0**	**—**	**5.5**	**V**	**Timer1 oscillator disabled**
		PIC18FX520	**4.2**	**—**	**5.5**	**V**	

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

6. Module: DC Characteristics

The following parameters in **Section 26.3 "DC Characteristics"** have been updated as follows:

- D032A has been changed and renamed D033
- D033 has been changed and renamed D033A
- D033B has been added
- D042A has been changed and renamed D043
- D043 has been changed and renamed D043A
- D043B has been added.

Changes are shown in **bold** text in the following table.

26.3 DC Characteristics: PIC18F6520/8520 (Industrial, Extended) PIC18LF6520/8520 (Industrial)

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
D033		**OSC1 (HS mode)**	**VSS**	**0.3 VDD**	**V**	
D033A		**OSC1 (in RC and EC mode)(1)**	**VSS**	**0.2 VDD**	**V**	
D033B		**OSC1 (in XT and LP modes and T1OSI)**	**VSS**	**0.3**	**V**	
	VIH	**Input High Voltage**				
D043		**OSC1 (HS mode)**	**0.7 VDD**	**VDD**	**V**	
D043A		**OSC1 (RC mode)(1)**	**0.9 VDD**	**VDD**	**V**	
D043B		**OSC1 (in XT and LP modes and T1OSI)**	**1.6**	**VDD**	**V**	

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PICmicro® device be driven with an external clock while in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

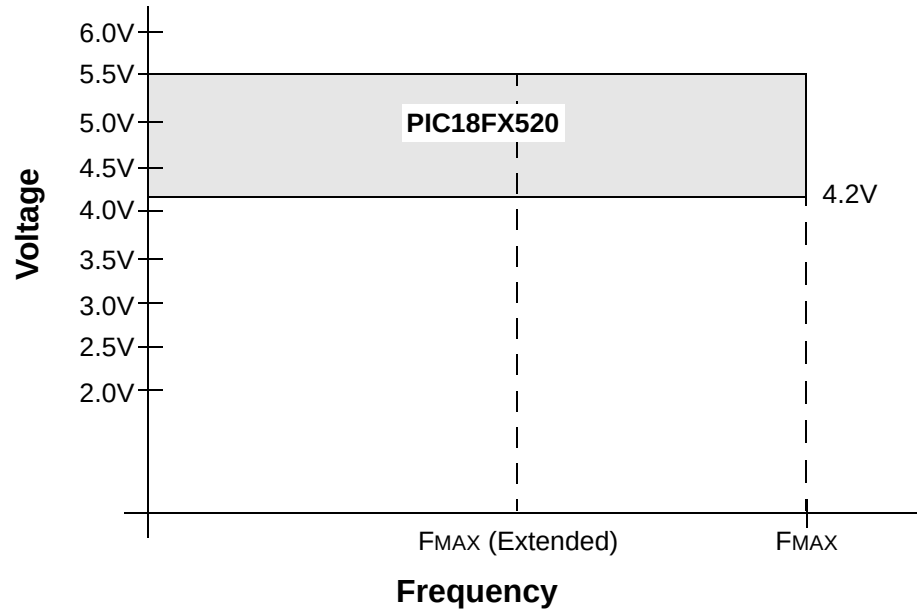
3: Negative current is defined as current sourced by the pin.

4: Parameter is characterized but not tested.

7. Module: Voltage-Frequency Graph

In **Section 26.0 "Electrical Characteristics"**, Figure 26-1 has been updated to clarify the voltage frequency for Industrial and Extended devices.

FIGURE 26-1: PIC18F6520/8520 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL, EXTENDED)



FMAX = 40 MHz for PIC18F6520/8520 in Microcontroller mode.
FMAX = 25 MHz for PIC18F6520/8520 in modes other than Microcontroller mode.
FMAX (Extended) = 25 MHz.

8. Module: External Clock Timing Requirements

External clock timing requirements for PIC18FX520 devices (Table 26-6, page 322) have been revised as follows (changes are shown in **bold** text):

TABLE 26-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	FOSC	External CLKI Period	DC	40	MHz	EC, ECIO, PIC18FX520 (Industrial
			DC	25	MHz	EC, ECIO, PIC18FX520 using external memory interface (Industrial)
			DC	**25**	**MHz**	**EC, ECIO, PIC18FX520 (Extended)**
		Oscillator Frequency	DC	4	MHz	RC oscillator
			0.1	4	MHz	XT oscillator
			4	25	MHz	HS oscillator (Industrial)
			4	**16**	**MHz**	**HS oscillator (Extended)**
			4	10	MHz	HS+PLL, PIC18FX520 (Industrial)
			4	6.25	MHz	HS+PLL, PIC18FX520 using external memory interface (Industrial)
			4	**6.25**	**MHz**	**HS+PLL, PIC18FX520 (Extended)**
			5	33	kHz	LP Oscillator mode
1	TOSC	External CLKI Period	25	—	ns	EC, ECIO, PIC18FX520 (Industrial)
			40	—	ns	EC, ECIO, PIC18FX520 using external memory interface (Industrial)
			40	**—**	**ns**	**EC, ECIO, PIC18FX520 (Extended)**
		Oscillator Period	250	—	ns	RC oscillator
			250	10,000	ns	XT oscillator
			40	250	ns	HS oscillator (Industrial)
			62.5	**250**	**ns**	**HS oscillator (Extended)**
			100	250	ns	HS+PLL, PIC18FX520 (Industrial)
			160	250	ns	HS+PLL, PIC18FX520 using external memory interface (Industrial)
			160	**250**	**ns**	**HS+PLL, PIC18FX520 (Extended)**
			30	200	µs	LP Oscillator mode

9. Module: CCP

In **Section 23.3.1 "Wake-up From Sleep"**, the list of peripheral interrupts which can wake the device from Sleep has been updated. From the list of 11 events, item 4 has been clarified and item 5 has been removed. The list now reads as follows:

1. PSP read or write.
2. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
3. TMR3 interrupt. Timer3 must be operating as an asynchronous counter.
4. CCP Capture mode interrupt (capture will not occur)
5. MSSP (Start/Stop) bit detect interrupt.
6. MSSP transmit or receive in Slave mode (SPI/I^2C).
7. USART RX or TX (Synchronous Slave mode).
8. A/D conversion (when A/D clock source is RC).
9. EEPROM write operation complete.
10. LVD interrupt.

10. Module: Voltage Reference Specifications

In Table 26-2: Voltage Reference Specifications (page 317), parameter D311, V_{RAA}, should be replaced with the following (specifications and conditions modified):

TABLE 26-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 3.0V < V_{DD} < 5.5V, -40°C < T_A < +125°C (unless otherwise stated).							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D311	V_{RAA}	Absolute Accuracy	—	—	**1/2**	LSb	

11. Module: OSCCON Register

In the OSCCON register (Register 2-1, page 25), the Reset value for the SCS bit (OSCCON<0>) was incorrectly stated as R/W-1 and has been changed to R/W-0

12. Module: Instruction Set (BTG)

In Table 24-1: PIC18FXXXX Instruction Set (page 262), the BTG instruction has been changed (change shown in **bold** text).

TABLE 24-1: PIC18FXXXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word		Status Affected	Notes
			MSb	LSb		
BYTE-ORIENTED FILE REGISTER OPERATIONS						
BTG f, **b**, a	Bit Toggle f	1	0111 bbba	ffff ffff	None	1, 2

13. Module: A/D Converter Characteristics

In Table 26-25: A/D Converter Characteristics (page 340), specification A40 has been added:

TABLE 26-25: A/D CONVERTER CHARACTERISTICS: PIC18FXX20 (INDUSTRIAL, EXTENDED) PIC18LFXX20 (INDUSTRIAL)

Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
A01	NR	Resolution		—	—	10	bit	
A03	EIL	Integral Linearity Error		—	—	<±1	LSb	VREF = VDD = 5.0V
A04	EDL	Differential Linearity Error		—	—	<±1	LSb	VREF = VDD = 5.0V
A05	EG	Gain Error		—	—	<±1	LSb	VREF = VDD = 5.0V
A06	EOFF	Offset Error		—	—	<±1.5	LSb	VREF = VDD = 5.0V
A10	—	Monotonicity		guaranteed(2)			—	VSS ≤ VAIN ≤ VREF
A20 A20A	VREF	Reference Voltage (VREFH – VREFL)		1.8V 3V	— —	— —	V V	VDD < 3.0V VDD ≥ 3.0V
A21	VREFH	Reference Voltage High		AVSS	—	AVDD + 0.3V	V	
A22	VREFL	Reference Voltage Low		AVSS – 0.3V(5)	—	VREFH	V	
A25	VAIN	Analog Input Voltage		AVSS – 0.3V(5)	—	AVDD + 0.3V(5)	V	VDD ≥ 2.5V **(Note 3)**
A30	ZAIN	Recommended Impedance of Analog Voltage Source		—	—	2.5	kΩ	**(Note 4)**
A40	**IAD**	**A/D Current for VDD**	**PIC18FXXXX**	**—**	**180**	**—**	**μA**	**Average current during conversion**
			PIC18LFXX20	**—**	**90**	**—**	**μA**	
A50	IREF	VREF Input Current **(Note 1)**		— —	— —	5 150	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: VSS ≤ VAIN ≤ VREF

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: For VDD < 2.5V, VAIN should be limited to <.5 VDD.

4: Maximum allowed impedance for analog voltage source is 10 kΩ. This requires higher acquisition times.

5: IVDD – AVDDI must be <3.0V and IAVSS – VSSI must be <0.3V.

REVISION HISTORY

Rev A Document (5/2003)

First revision of this document. Silicon issues 1 (I/O Ports), 2 (Core) and 3 (MSSP). Data Sheet Clarification issues 1 (A/D), 2 (Data EEPROM), 3 (Memory), 4 (Timer0), 5 (Pin Diagrams), 6 (MSSP), 7 (A/D Converter Characteristics), 8 (Electrical Characteristics), 9 (Low-Power Timer1), 10 (Table 23-1: Configuration Bits and Device IDs), 11 (Register 23-5: CONFIG3H: Configuration Register 3 High), 12 (DC Characteristics) and 13 (Table 26-4: Memory Programming Requirements).

Rev B Document (3/2004)

Added silicon issues 4 (External Memory Bus) and 5 (USART). Previous Data Sheet Clarification issues 1-9 and 11 were removed; previous issues 10, 12 and 13 remain and are now numbered 1-3.

Rev C Document (8/2004)

Revised silicon issue 3 (MSSP – SPI, Slave Mode). Revised Data Sheet Clarification issue 2 (DC Characteristics) and added issue 4 (Timer0 Block Diagrams), 5 (DC Characteristics – V_{DD} Specifications) and 6 (DC Characteristics).

Rev D Document 1/2005)

Removed silicon issue 3 (MSSP – SPI, Slave Mode). Updated silicon issues 1 (I/O Ports – Parallel Slave Port), 2 (Core – DAW Instruction), 3 (External Memory Bus) and 4 (USART). Revised Data Sheet Clarification issues 1 (Table 23-1: Configuration Bits and Device IDs), 2 (DC Characteristics: Power-Down and Supply Current), 3 (Table 26-4: Memory Programming Requirements), 4 (Timer0 Block Diagrams) and 5 (DC Characteristics – V_{DD} Specifications. Added Data Sheet Clarification issues 7 (Voltage-Frequency Graph), 8 (External Clock Timing Requirements), 9 (CCP), 10 (Voltage Reference Specifications), 11 (OSCCON Register), 12 (Instruction Set – BTG) and 13 (A/D Converter Characteristics).

NOTES:

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