PIC16C781/782

PIC16C781/782 Rev. B1 Silicon/Data Sheet Errata

The PIC16C781/782 parts you have received conform functionally to the Device Data Sheet (DS41171**A**), except for the anomalies described below.

Note:	The silicon revision of a specific component is identified by its manufacture date code: YYWW, YY is the year of manufacture and WW is the specific work week. All material with a date code of 0228 or earlier is revision B1 silicon, and subject to the Errata contained in this document. Any components with a latter date code will be silicon revision B3 or latter and will be covered in a separate Errata. For additional information concerning date codes, refer to the packaging information section of the PIC16C781/782 data sheet (DS41171A).

1. Module: Programmable Switch Mode Controller (PSMC)

In the Pulse Width Mode (PWM) when a comparator threshold crossing event occurs after the minimum duty cycle time (Min DC) and coincident with a PSMC clock edge, the pulse output of the PSMC will immediately and correctly go to the inactive state. One PSMC clock period later, the output may incorrectly become active and remain active until the pulse terminates at the completion of the maximum duty cycle time (Max DC).

Work around

If possible, use the Pulse Skipping Mode (PSM). If your application requires PWM, then please contact your local Microchip representative.

2. Module: Voltage Comparator

When the voltage comparator inputs are subjected to fast rise time pulses, some units exhibit a momentary invalid state on their output. The probability of generating an invalid output state is dependant upon four factors:

1. Pulse slew rate
2. Supply Voltage (V_{DD})
3. Ambient Temperature
4. Reference Voltage (V_{COMMON_MODE})

Figures 1 through 5 show the input slew rate limits for normal operation of the voltage comparators in Fast mode, for a variety of Common mode voltages, supply voltages and ambient temperatures.

If the PSMC is used in conjunction with the voltage comparators, an invalid voltage comparator output state can cause the premature termination of PSMC output pulses.

Work around

The pulse rise time of inputs to the voltage comparators should be less than the limits shown in Figures 1 through 5 for the specific conditions of operation (supply voltage, temperature, Common mode voltage). The values shown are for pulses with a constant rise time. For pulses with compound rise times (pulses with non-linear or changing slopes), the limits may be different.

Note:	The area below the line for any given temperature is the safe operating area.

FIGURE 1: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT VDD = 5.5V

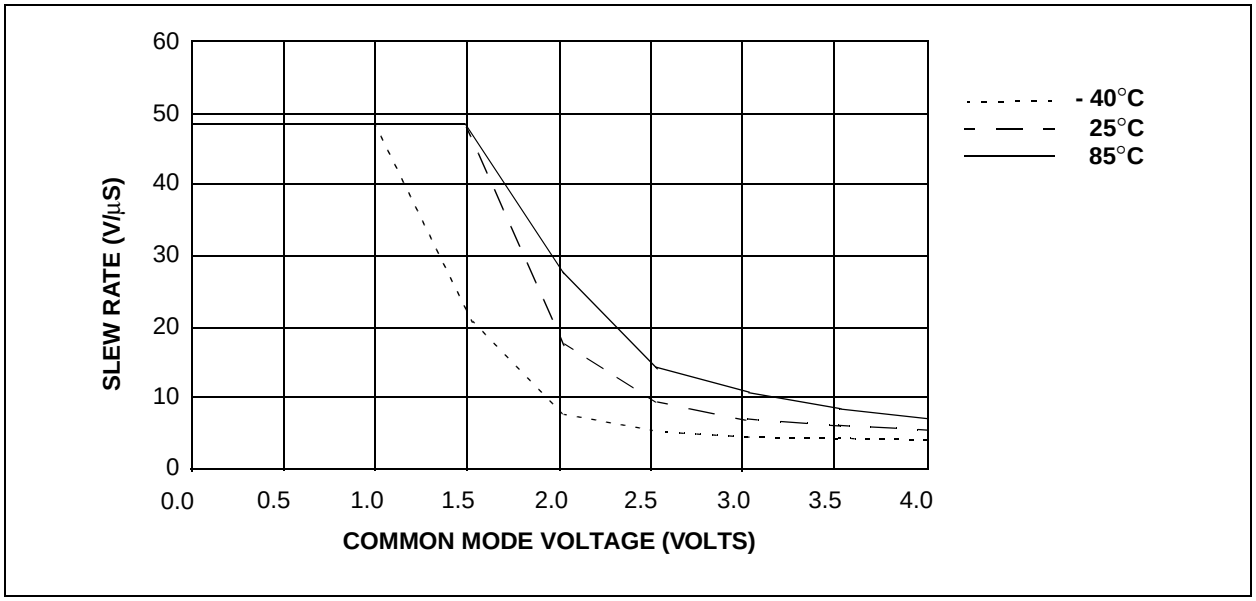


FIGURE 2: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT VDD = 5.5V

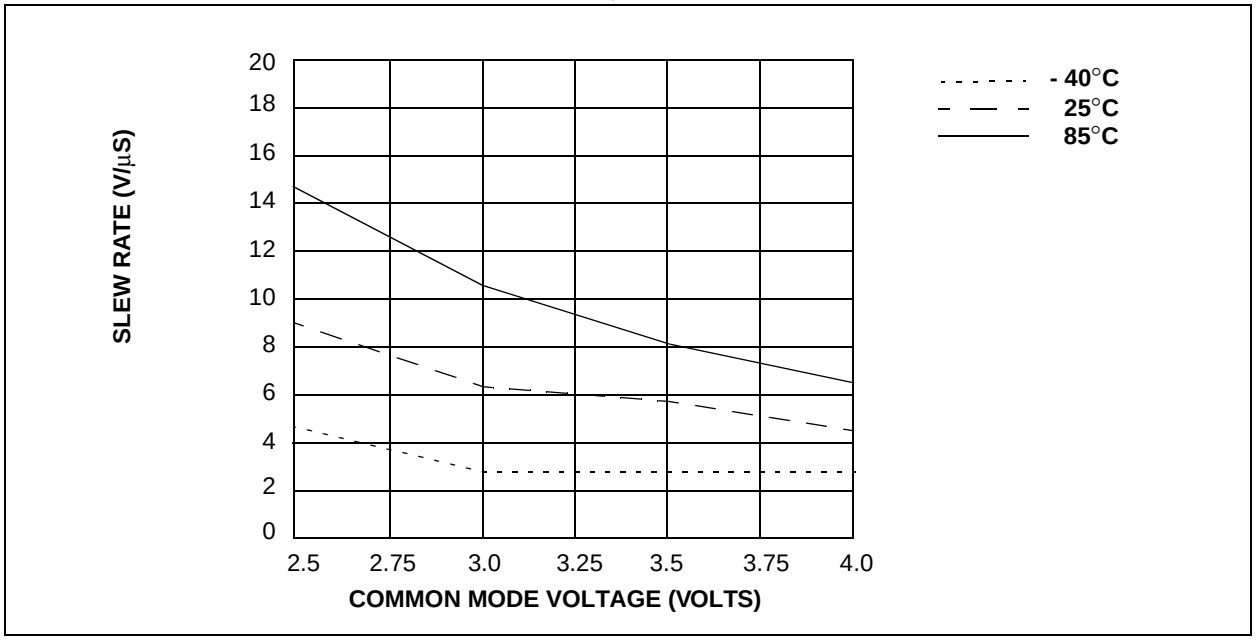


FIGURE 3: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT VDD = 4.0V

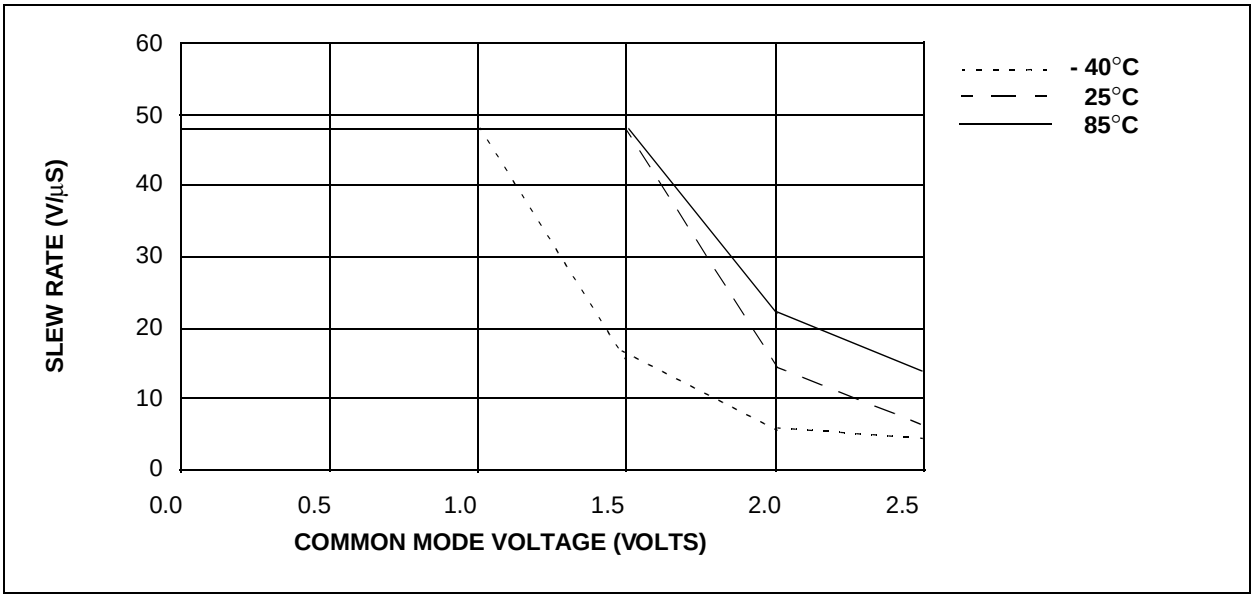


FIGURE 4: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT VDD = 3.5V

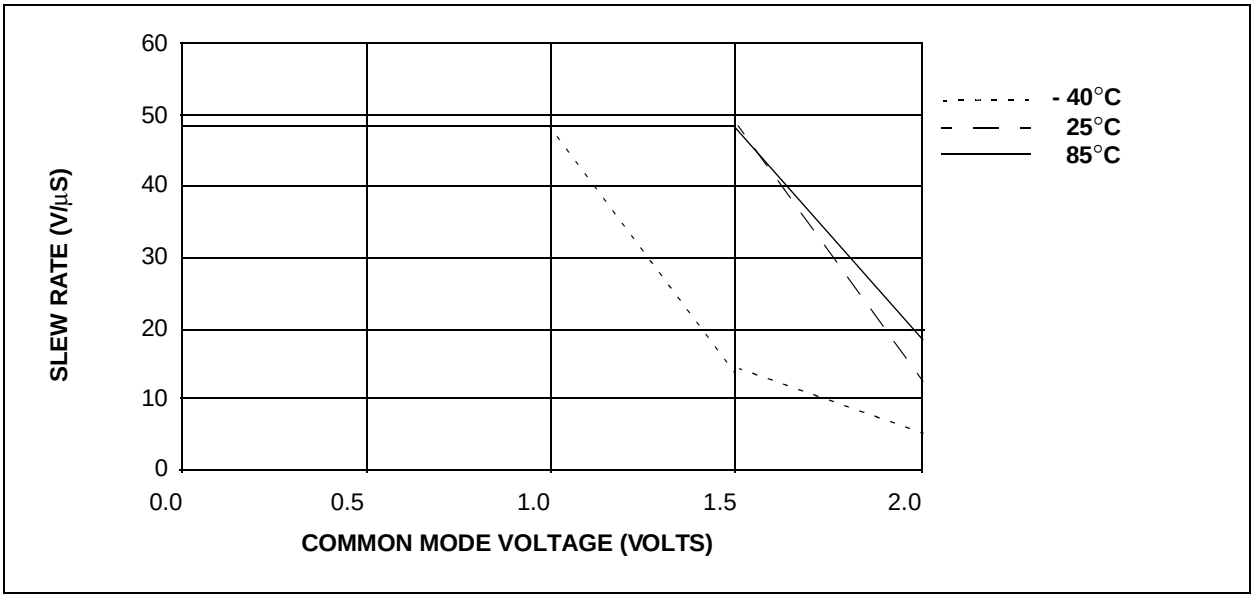
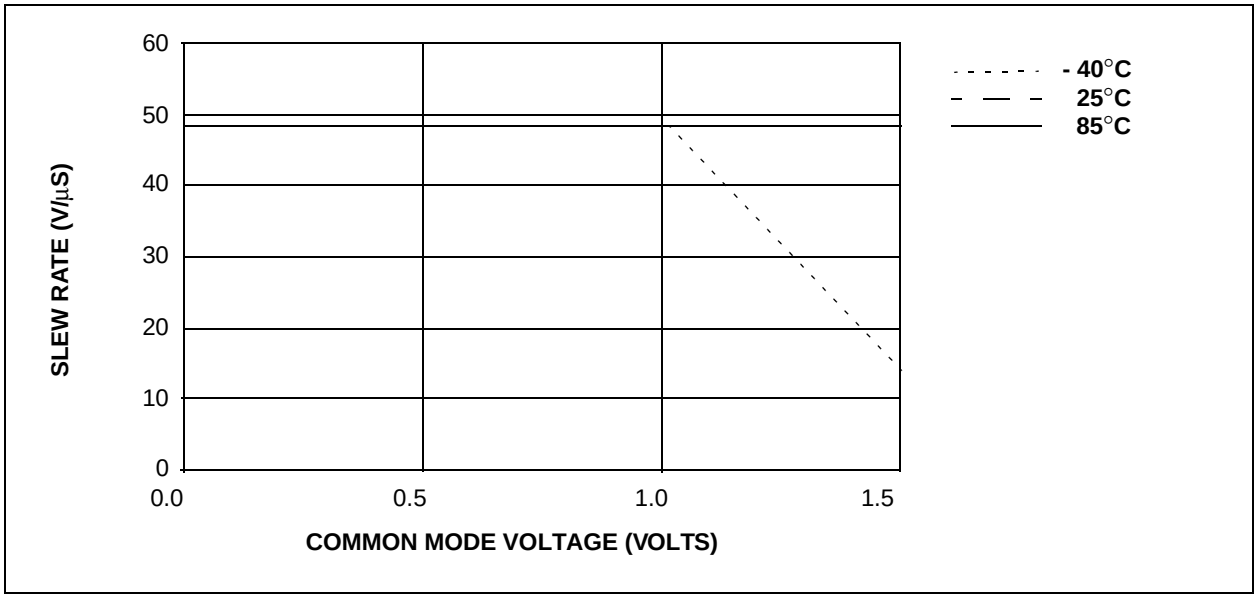


FIGURE 5: VOLTAGE COMPARATOR INPUT, MAXIMUM SLEW RATE AT V_{DD} = 3.0V



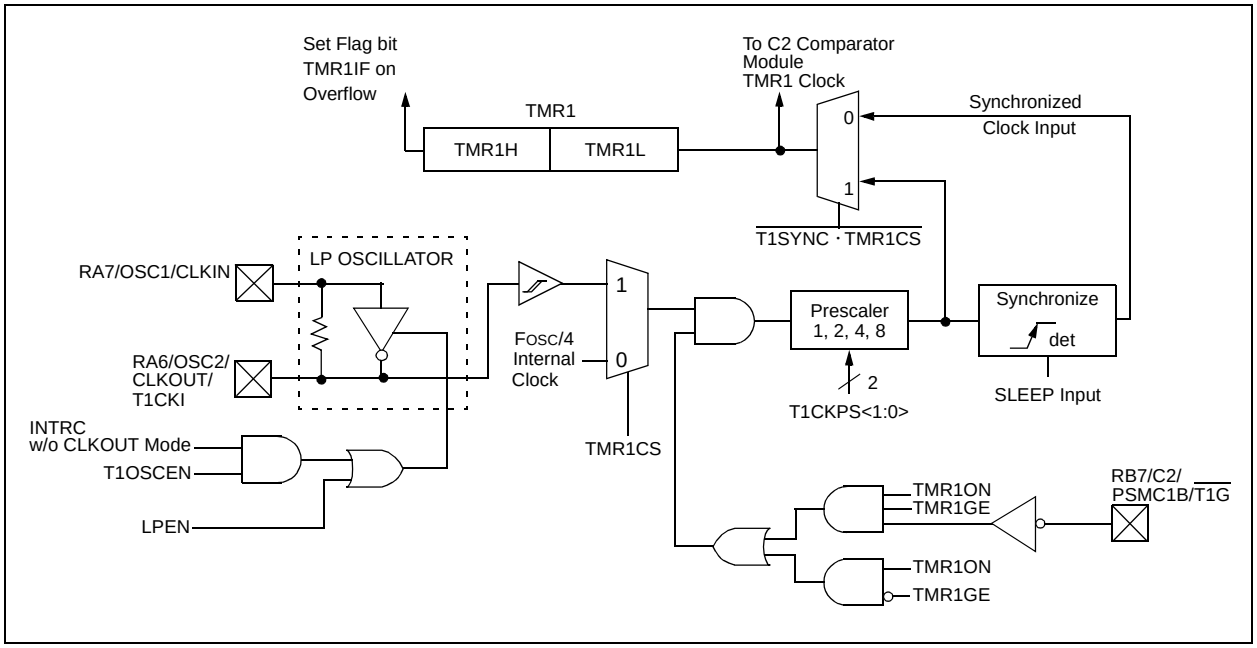
3. Module: Timer1

Exception to Figure 6-2 on page 58 of the data sheet.

The Timer1 gate function controls the flow of clock pulses to the Timer1 prescaler, not the Timer1 counter, as specified in Figure 6-2. Figure 6-2 below shows the Timer1 gate circuitry as it exists now.

Note: To implement synchronized sampling for a Delta Sigma converter, use the software implementation as described in Application Note AN700.

FIGURE 6-2: TIMER1 ON THE PIC16C781/782 BLOCK DIAGRAM



Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41171**A**), the following clarifications and corrections should be noted.

1. Module: I/O Ports

Exception to Figure 3-6 on page 32.

When the RA5 pin is configured as the external MCLR input (CONFIG<MCLRE> = 1), the port bit will read as set (RA<5> = 1), not cleared, as specified in Figure 3-6.

2. Module: Digital-to-Analog Converter

Correction to Example 10-1 on page 81.

The following line of code:

"`BSF ANSEL,1 ;set RB1 as analog`"

Should be:

"`BSF ANSEL,5 ;set RB1 as analog`"

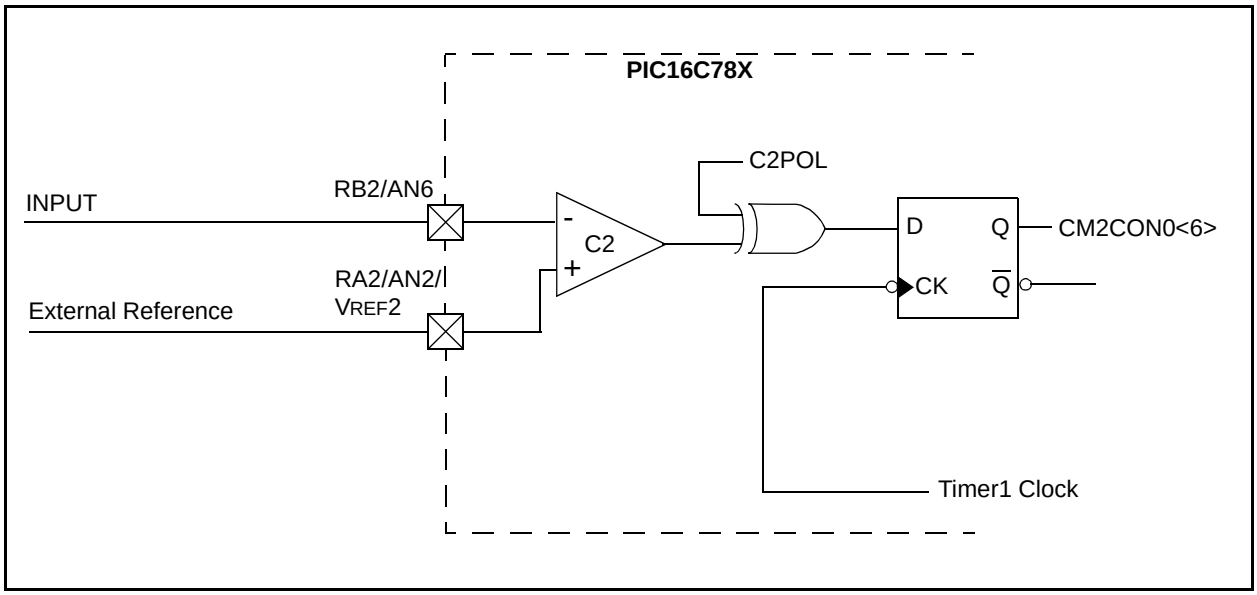
Note: DAC output function overrides ANSEL and TRISB register control of the port pin.

3. Module: Comparator Module

Correction to Figure 12-3 on page 95.

The synchronizing clock signal is supplied by the Timer1 clock, not the RA6 pin as shown in Figure 12-3.

FIGURE 12-3: COMPARATOR C2 CONFIGURATION WITH OUTPUT SYNCHRONIZED TO TIMER1 CLOCK



REVISION HISTORY

Rev A Document (1/02)

Original errata document, which includes clarifications/corrections to Data Sheet Items 1, 2, 3 and 4.

Rev B Document (6/02)

Added Item 1 to page 1.

Rev C Document (7/01)

Added Figures 1 through 5. Added Item 2, Voltage Comparator to page 1.

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

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