

# ESD7471, SZESD7471

## Ultra-Low Capacitance ESD Protection

### Micro-Packaged Diodes for ESD Protection

The ESD7471 is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, high breakdown voltage, high linearity, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. It has industry leading capacitance linearity over voltage making it ideal for RF applications. This capacitance linearity combined with the extremely small package and low insertion loss makes this part well suited for use in antenna line applications for wireless handsets and terminals.

#### Features

- Industry Leading Capacitance Linearity Over Voltage
- Ultra-Low Capacitance: 0.35 pF Max
- Stand-off Voltage: 5.3 V
- Low Leakage: < 1 nA
- Low Dynamic Resistance: < 1  $\Omega$
- IEC61000-4-2 Level 4 ESD Protection
- 1000 ESD IEC61000-4-2 Strikes  $\pm 8$  kV Contact / Air Discharged
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications
- USB 2.0, USB 3.0

#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
IEC 61000-4-2 Contact (ESD) (Note 1)	ESD	$\pm 20$	KV
IEC 61000-4-2 Air (ESD) (Note 1)	ESD	$\pm 20$	kV
IEC 61000-4-5 (ESD) (Note 2)	ESD	2.2	A
Total Power Dissipation (Note 3) @ $T_A = 25^\circ\text{C}$	$P_D$	300	mW
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	400	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature - Maximum (10 Second Duration)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. At least 10 discharges at  $T_A = 25^\circ\text{C}$ , per IEC61000-4-2 waveform.
2. Non-repetitive current pulse at  $T_A = 25^\circ\text{C}$ , per IEC61000-4-5 waveform.
3. Mounted with recommended minimum pad size, DC board FR-4



ON Semiconductor®

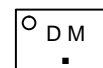
[www.onsemi.com](http://www.onsemi.com)



#### MARKING DIAGRAM



XDFN2  
CASE 711AM



- D = Specific Device Code
- M = Date Code
- = Pb-Free Package

#### ORDERING INFORMATION

Device	Package	Shipping†
ESD7471N2T5G	XDFN2 (Pb-Free)	8000 / Tape & Reel
SZESD7471N2T5G	XDFN2 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

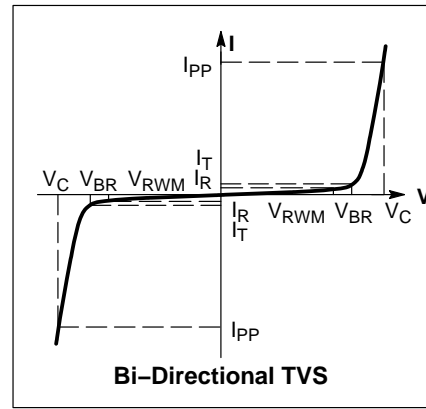
# ESD7471, SZESD7471

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current

\*See Application Note AND8308/D for detailed explanations of datasheet parameters.



## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$				5.3	V
Breakdown Voltage	$V_{BR}$	$I_T = 1\text{ mA}$ (Note 4)	7.0			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5.3\text{ V}$		< 1	50	nA
Clamping Voltage	$V_C$	$I_{PP} = 1\text{ A}$ (Note 5)		13	15	V
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ $V_R = 0\text{ V}$ , $f = 1\text{ GHz}$		0.24 0.24	0.35 0.35	pF
Dynamic Resistance	$R_{DYN}$	TLP Pulse		0.8		$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
- Non-repetitive current pulse at  $25^\circ\text{C}$ , per IEC61000-4-5 waveform.

## TYPICAL CHARACTERISTICS

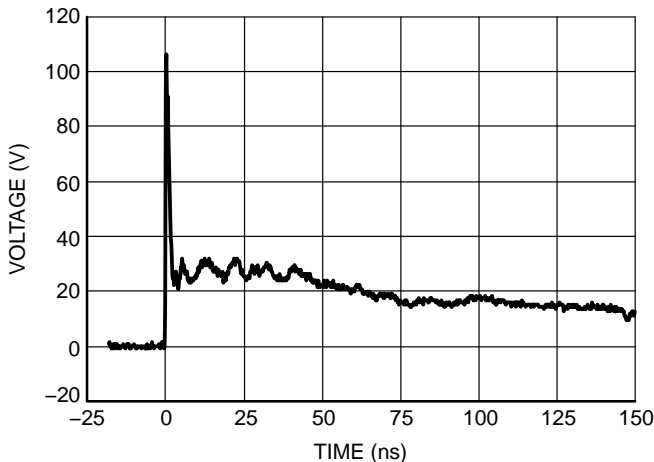


Figure 1. Typical IEC61000-4-2 + 8 kV Contact ESD Clamping Voltage

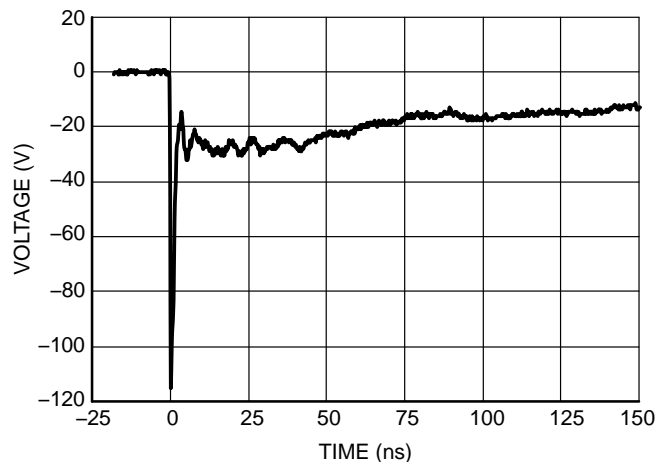


Figure 2. Typical IEC61000-4-2 - 8 kV Contact ESD Clamping Voltage

# ESD7471, SZESD7471

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 3. IEC61000-4-2 Spec

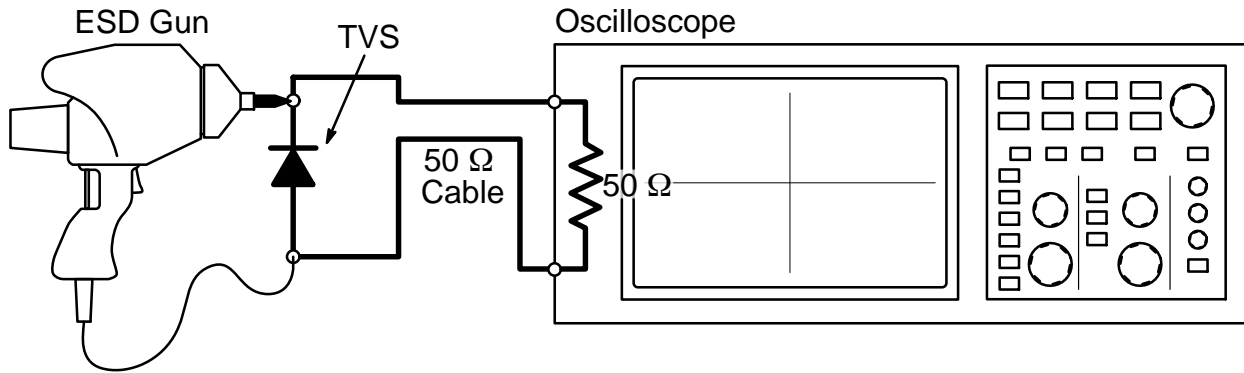


Figure 4. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

# ESD7471, SZESD7471

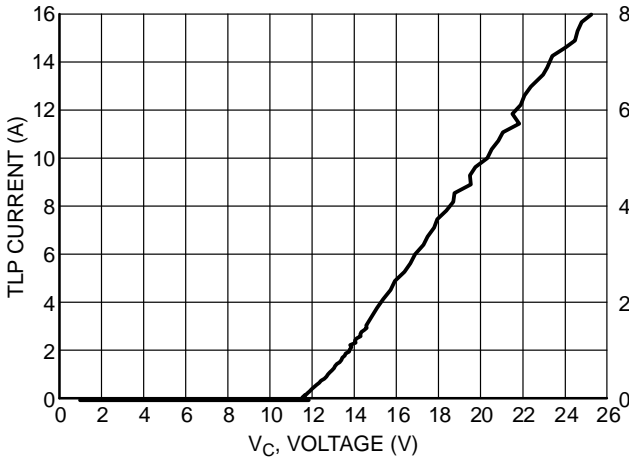


Figure 5. Typical Positive TLP IV Curve

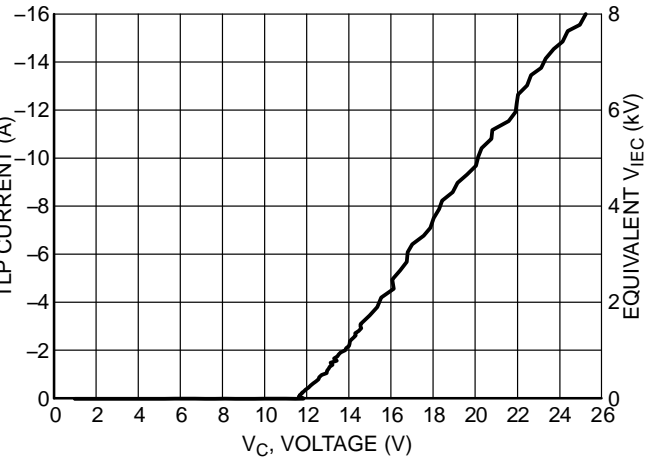


Figure 6. Typical Negative TLP IV Curve

NOTE: TLP parameter:  $Z_0 = 50 \Omega$ ,  $t_p = 100 \text{ ns}$ ,  $t_r = 300 \text{ ps}$ , averaging window:  $t_1 = 30 \text{ ns}$  to  $t_2 = 60 \text{ ns}$ .

## Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

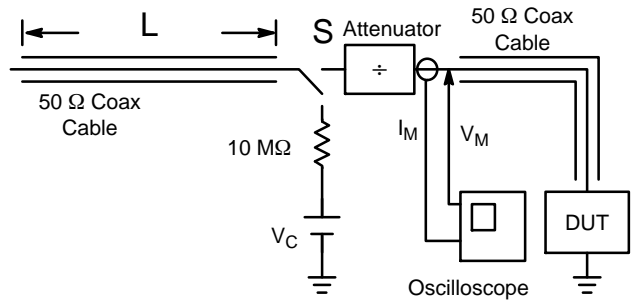


Figure 7. Simplified Schematic of a Typical TLP System

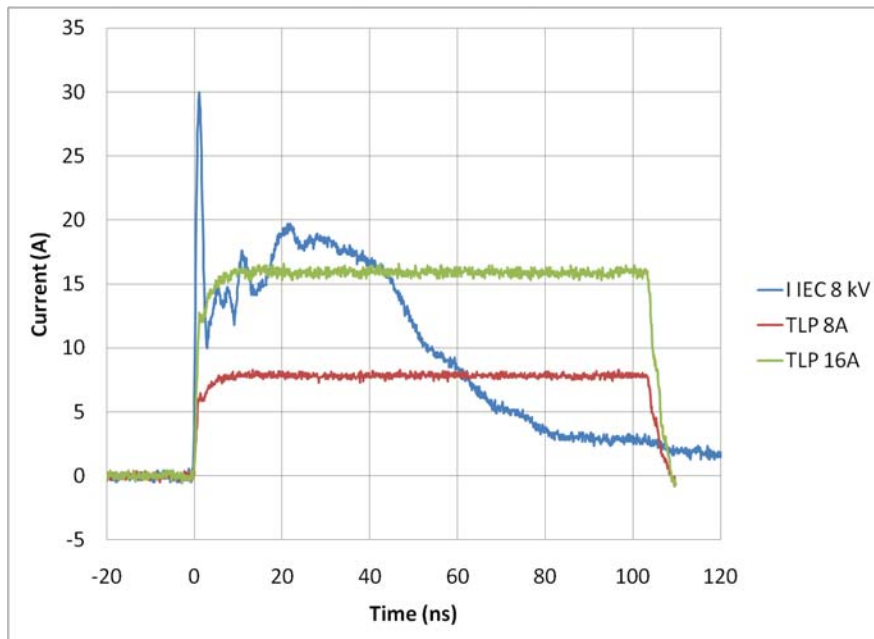


Figure 8. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

# ESD7471, SZESD7471

## TYPICAL CHARACTERISTICS

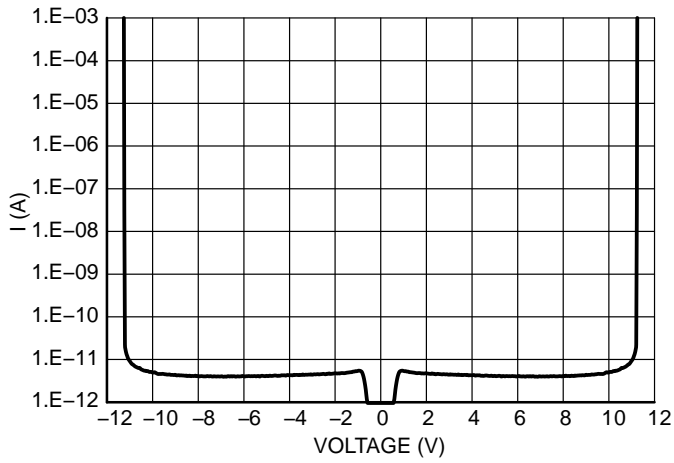


Figure 9. IV Characteristics

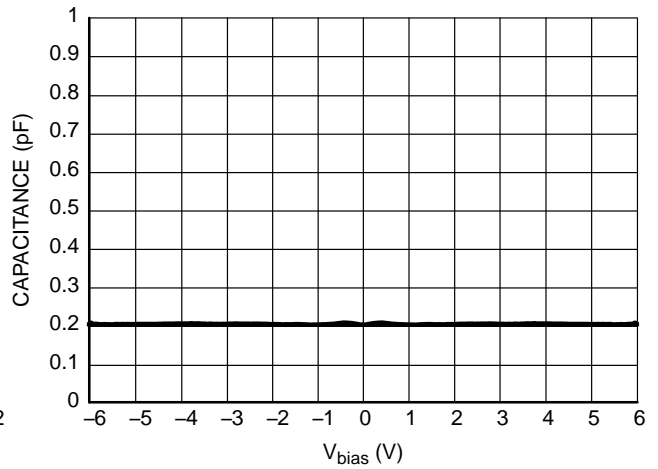


Figure 10. CV Characteristics

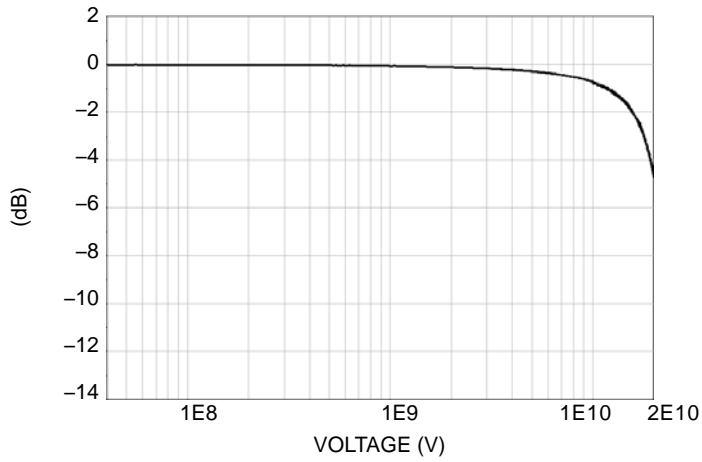


Figure 11. RF Insertion Loss

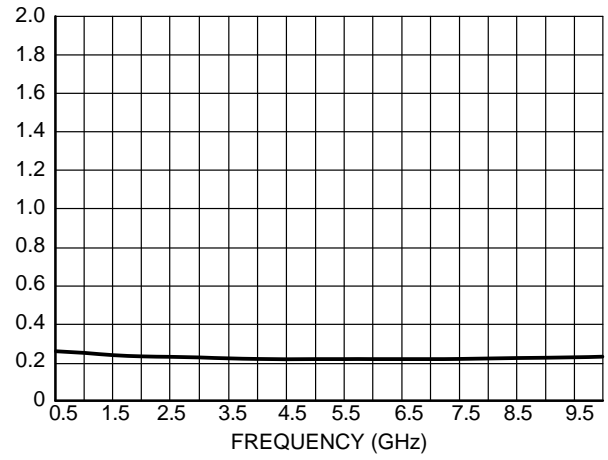
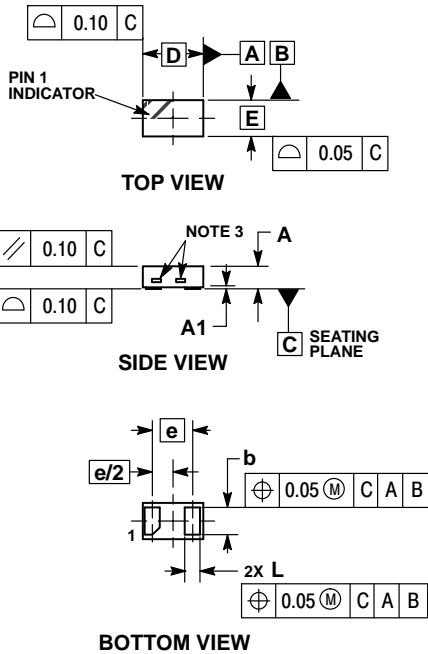


Figure 12. Capacitance over Frequency

# ESD7471, SZESD7471

## PACKAGE DIMENSIONS

### XDFN2 1.0x0.6, 0.65P (SOD-882) CASE 711AM ISSUE O

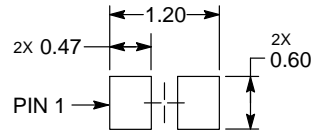


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

MILLIMETERS		
DIM	MIN	MAX
A	0.34	0.44
A1	—	0.05
b	0.43	0.53
D	1.00	BSC
E	0.60	BSC
e	0.65	BSC
L	0.20	0.30

### RECOMMENDED SOLDER FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative