550kHz Synchronous Switching Regulator Controller Plus Linear Regulator Controller

FEATURES

- **Dual Regulated Outputs: One Switching Regulator and One Linear Regulator**
- **Excellent DC Accuracy: ±1.5% for Switcher and ±2% for Linear Regulator**
- External N-Channel MOSFET Architecture
- No External Current Sense Resistor Required
- Burst Mode® Operation at Light Load (LTC1704)
- Continuous Switching at Light Load (LTC1704B)
- Linear Regulator with Programmable Current Limit
- Linear Regulator with Programmable Start-Up Delay
- Low Shutdown Current: <150µA
- High Efficiency Over Wide Load Current Range
- PGOOD Flag Monitors Both Outputs
- Small 16-Pin Narrow SSOP Package

APPLICATIONS

- Multiple Logic Supply Generator
- Distributed Power Applications
- High Efficiency Power Conversion

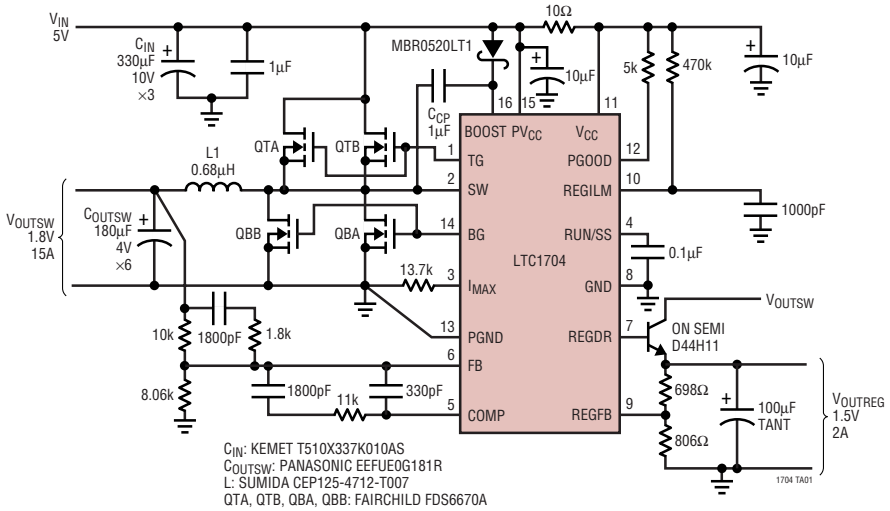
DESCRIPTION

The LTC®1704/LTC1704B include a high power synchronous switching regulator controller plus a linear regulator controller. The switching regulator controller is designed to drive a pair of N-channel MOSFETs in a voltage mode, synchronous buck configuration to provide the main supply. The constant frequency, true PWM architecture switches at 550kHz, minimizing external component size, cost and optimizing load transient performance. The LTC1704 features automatic transition to power saving Burst Mode operation at light loads. The LTC1704B does not shift into Burst Mode operation at light loads, eliminating low frequency output ripple at the expense of light load efficiency. The linear regulator controller is designed to drive an external NPN power transistor to provide up to 2A of current to an auxiliary load.

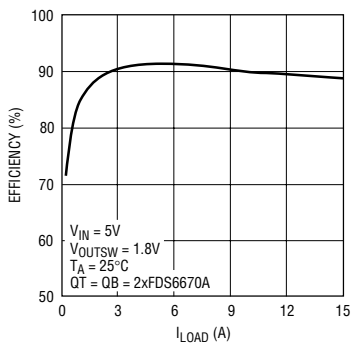
The LTC1704/LTC1704B deliver better than ±1.5% DC accuracy at the switcher outputs and ±2% at the linear regulator outputs. High performance feedback loops allow the circuit to keep total output regulation within ±5% under all transient conditions. An open-drain PGOOD output indicates when both outputs are within ±10% of their regulated values.

TYPICAL APPLICATION

5V to 1.8V/15A and 1.5V/2A Application



Switcher Efficiency



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage

V_{CC}, PV_{CC} 6V

BOOST 12V

BOOST – SW 6V

Input Voltage

SW ..... –1V to 6V

FB, REGFB, REGILM,

RUN/SS, I_{MAX} ..... –0.3V to (V_{CC} + 0.3V)

Peak Output Current <10µs

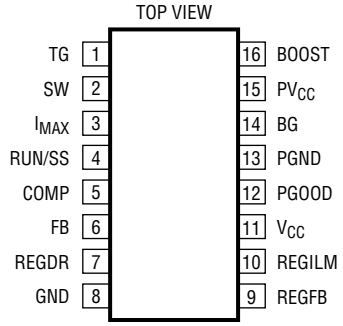
TG, BG (Note 7) 5A

Operating Temperature Range (Note 2) .. –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1704EGN LTC1704BEGN
GN PART MARKING
1704 1704B

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = PV_{CC} = BOOST = 5V, unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Supply Voltage		●	3.15	5	5.5	V
PV_{CC}	PV_{CC} Supply Voltage	(Note 4)	●	3.15	5	5.5	V
BV_{CC}	BOOST Pin Voltage	V_{BOOST} – V_{SW} (Note 4)	●	3.15	5	5.5	V
I_{VCC}	V_{CC} Supply Current	Test Circuit $V_{RUN/SS}$ = 0V, V_{REGILM} = 0V	● ●		4.5 75	8 150	mA µA
I_{PVCC}	PV_{CC} Supply Current	Test Circuit, No Load at Drivers $V_{RUN/SS}$ = 0V (Notes 5, 6)	● ●		3	6 50	mA µA
I_{BOOST}	BOOST Pin Current	Test Circuit $V_{RUN/SS}$ = 0V (Notes 5, 6)	● ●		2	6 50	mA µA
V_{SHDN}	RUN/SS Shutdown Threshold	$V_{RUN/SS}$ ↑	●	0.2	0.5		V
I_{SS}	RUN/SS Source Current	$V_{RUN/SS}$ = 0V			–3		µA
Switcher Control Loop							
V_{FB}	Feedback Voltage		●	0.788	0.800	0.812	V
I_{FB}	Feedback Input Current		●			±1	µA
dV_{FB}	Feedback Voltage Line Regulation	V_{CC} = 3.3V to 5.5V	●		±0.01	±0.1	%/V
	Output Voltage Load Regulation	(Note 7)	●	–0.2	–0.1		%
A_{FB}	Feedback Amplifier DC Gain		●	74	85		dB
GBW	Feedback Amplifier Gain Bandwidth Product	f = 100kHz (Note 7)			20		MHz
I_{COMP}	Feedback Amplifier Output Sink/Source Current		●	±3	±10		mA
V_{PGOOD}	Negative Power Good Threshold		●	–15	–10	–6	%
	Positive Power Good Threshold		●	6	10	15	%
I_{IMAX}	I_{MAX} Source Current	V_{IMAX} = 0V	●	–11.5	–10	–8.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = PV_{CC} = BOOST = 5V, unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switcher Switching Characteristics							
f_{OSC}	Oscillator Frequency	Test Circuit	●	460	550	650	kHz
DC_{MAX}	Maximum Duty Cycle		●	87	90	93	%
t_{NOV}	Driver Nonoverlap	Test Circuit (Note 8)	●	10	25	120	ns
t_r, t_f	Driver Rise/Fall Time	Test Circuit (Note 8)	●		15	100	ns
Linear Regulator Controller							
V_{REGFB}	Feedback Voltage	Test Circuit, R_{REGILM} = 680k	 ●	0.784 0.780	0.800 0.800	0.816 0.820	V V
I_{REGFB}	REGFB Input Current		●			±1	µA
dV_{REGFB}	Feedback Voltage Line Regulation	Test Circuit, V_{CC} = 4.5V to 5.5V	●		±0.05	±0.2	%/V
	Feedback Voltage Load Regulation	Test Circuit, I_{REGDR} = 0mA to 30mA	●	–0.2	–0.05		%
I_{REGDR}	Driver Output Current	Test Circuit R_{REGILM} = 680k, V_{REGFB} = 0.76V, V_{REGDR} = 3.3V R_{REGILM} = 680k, V_{REGFB} = 0V, V_{REGDR} = 1V	●	30	 20 6		mA mA mA
$V_{DROPOUT}$	Driver Dropout Voltage	Test Circuit, I_{REGDR} = 30mA, V_{REGDR} = 3.3V, dV_{REGFB} = –1% (Note 9)	●		0.65	1.1	V
V_{REGILM}	REGILM Threshold	Test Circuit, R_{REGILM} = 680k			0.8		V
$I_{REGILMINT}$	REGILM Internal Pull-Up Current	V_{REGILM} = 0V			–1.9		µA
V_{PGOOD}	Negative REGFB Power Good Threshold		●	–15	–10	–6	%
	Positive REGFB Power Good Threshold		●	6	10	15	%
PGOOD							
I_{PGOOD}	V_{PGOOD} Sink Current	Power Good Power Bad	● ●	 10		10	µA mA
V_{OLPG}	V_{PGOOD} Output Low Voltage	I_{PGOOD} = 1mA	●		0.03	0.1	V
t_{PGOOD}	V_{PGOOD} Falling Edge Delay	(Note 8)	●	0.5	1	4	µs
	V_{PGOOD} Rising Edge Delay	(Note 8)	●	10	20	40	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1704E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: PV_{CC} and BV_{CC} (V_{BOOST} – V_{SW}) must be greater than $V_{GS(ON)}$ of the external MOSFETs to ensure proper operation.

Note 5: Supply current in normal operation is dominated by the current needed to charge and discharge the external MOSFET gates. This current will vary with supply voltage and the external MOSFETs used.

Note 6: Supply current in shutdown is dominated by external MOSFET leakage and may be significantly higher than the quiescent current drawn by the LTC1704, especially at elevated temperature.

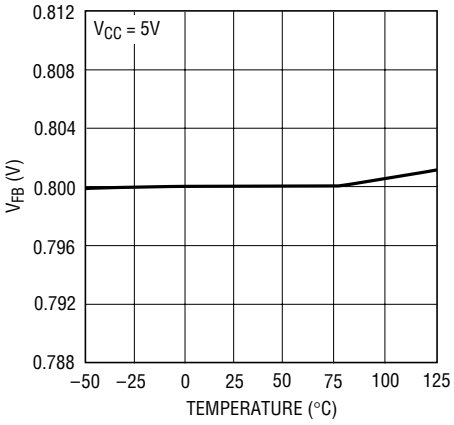
Note 7: Guaranteed by design, not subject to test.

Note 8: Rise and fall times are measured using 10% and 90% levels. Delay and nonoverlap times are measured using 50% levels.

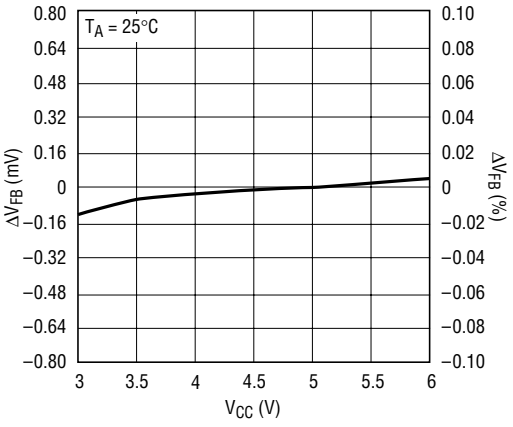
Note 9: Dropout voltage is the minimum V_{CC} to V_{REGDR} voltage differential required to maintain regulation at the specified driver output current.

TYPICAL PERFORMANCE CHARACTERISTICS

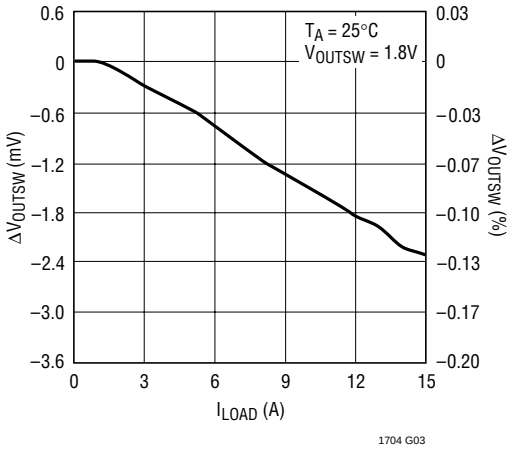
V_{FB} vs Temperature



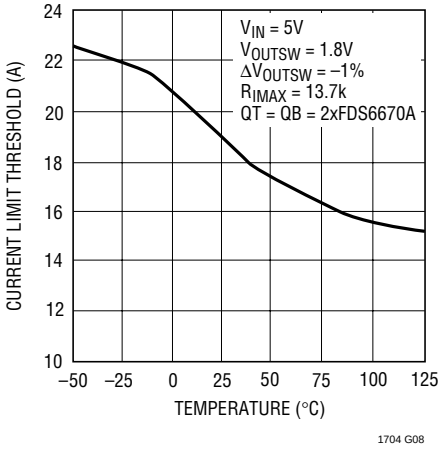
V_{FB} Line Regulation



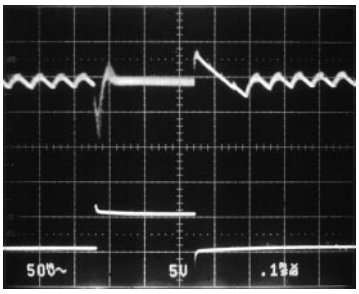
V_{OUTSW} Load Regulation



Switcher Current Limit Threshold vs Temperature



V_{OUTSW} 0.5A to 5.5A Load Step (Burst Mode Operation)

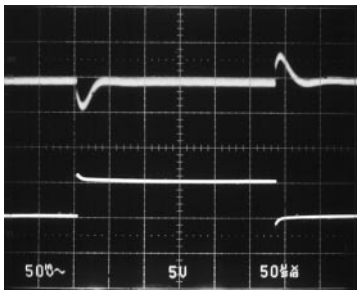


100µs/DIV 1704 G05

CH1: V_{OUTSW} = 1.8V, AC 50mV/DIV

CH2: 0.5A to 5.5A LOAD, 5A DIV

V_{OUTSW} 5A to 10A Load Step

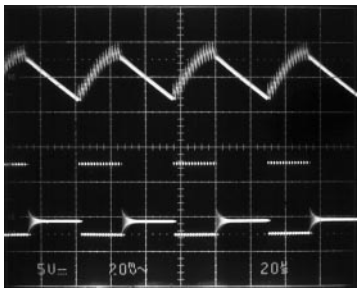


50µs/DIV 1704 G06

CH1: V_{OUTSW} = 1.8V, AC 50mV/DIV

CH2: 5A to 10A LOAD, 5A DIV

V_{OUTSW} Burst Mode Operation at 1A Load



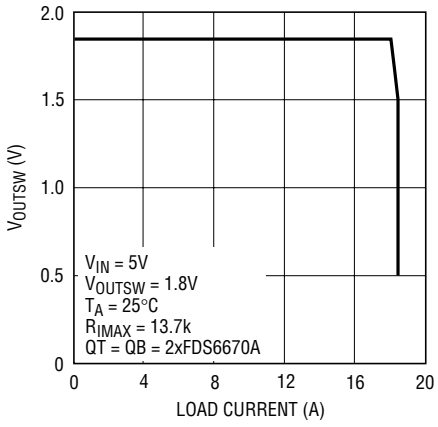
20µs/DIV 1704 G07

CH1: V_{OUTSW} = 1.8V, AC 20mV/DIV

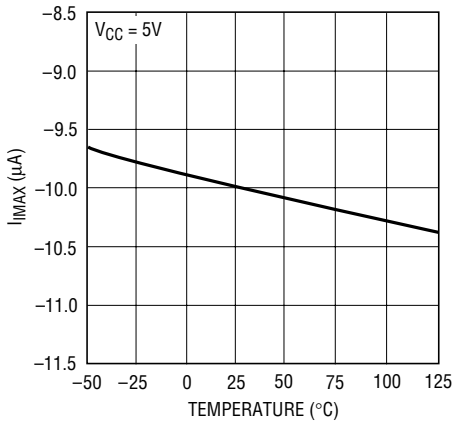
CH2: V_{TG}, 5V DIV

TYPICAL PERFORMANCE CHARACTERISTICS

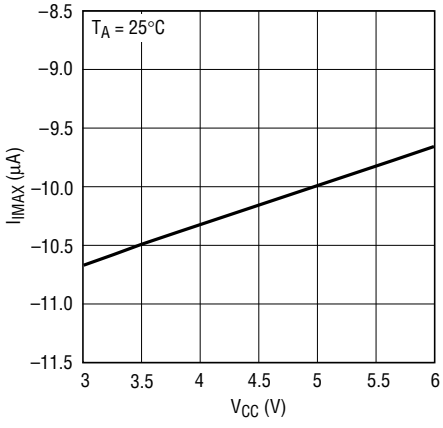
V_{OUTSW} vs Load Current



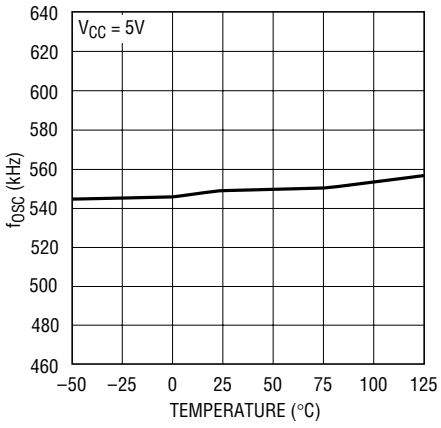
I_{IMAX} vs Temperature



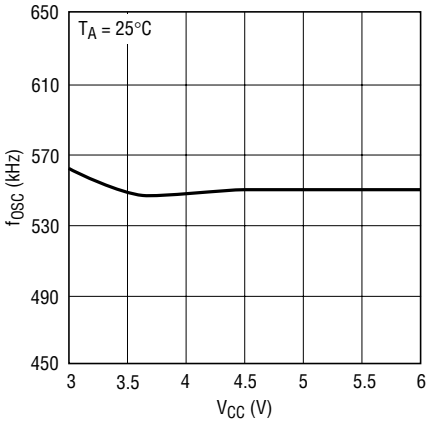
I_{IMAX} vs V_{CC}



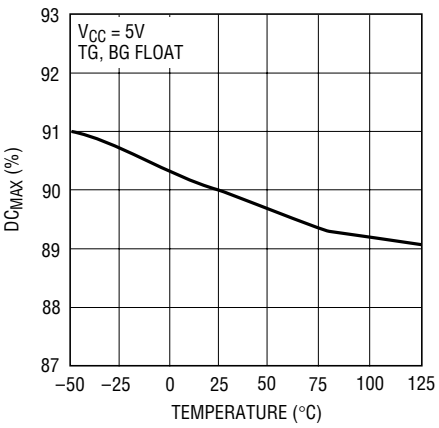
f_{OSC} vs Temperature



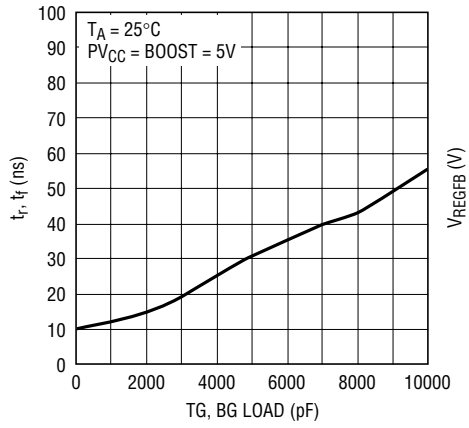
f_{OSC} vs V_{CC}



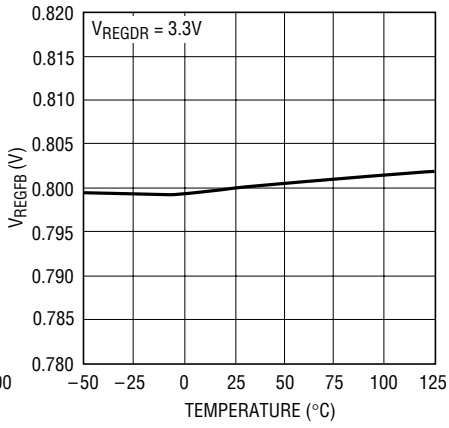
Maximum TG Duty Cycle vs Temperature



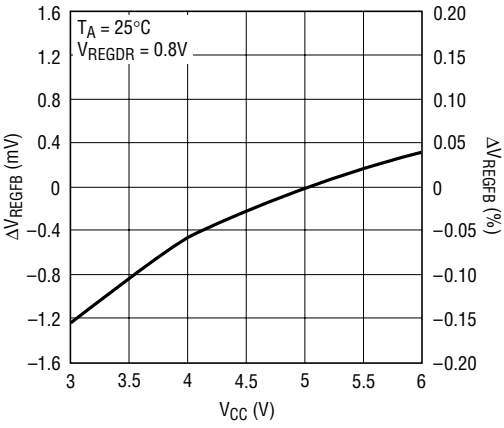
Drivers Rise and Fall Time vs Load



V_{REGFB} vs Temperature

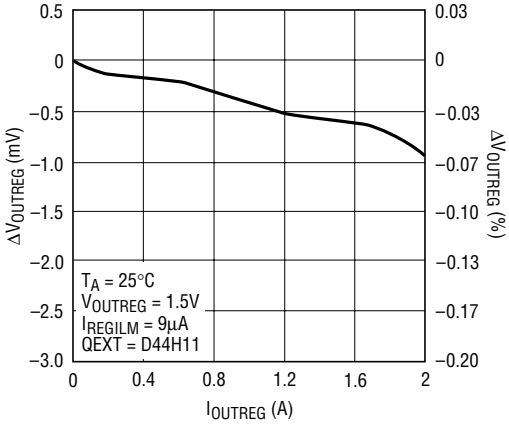


V_{REGFB} Line Regulation

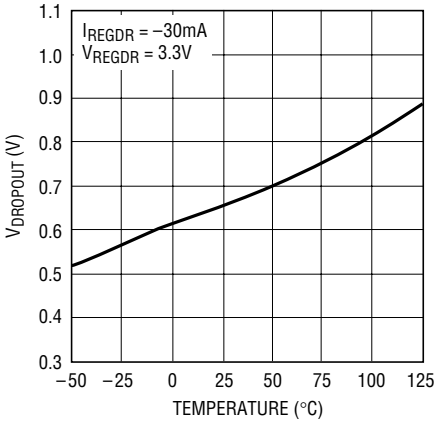


TYPICAL PERFORMANCE CHARACTERISTICS

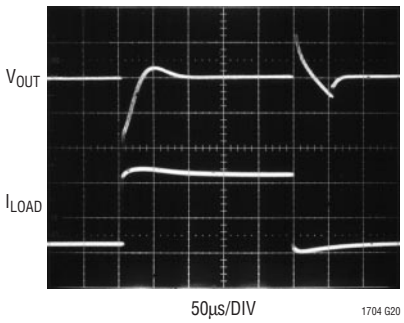
V_{OUTREG} Load Regulation



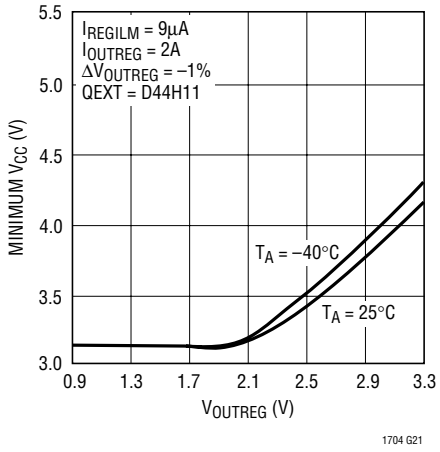
Linear Regulator Dropout Voltage vs Temperature



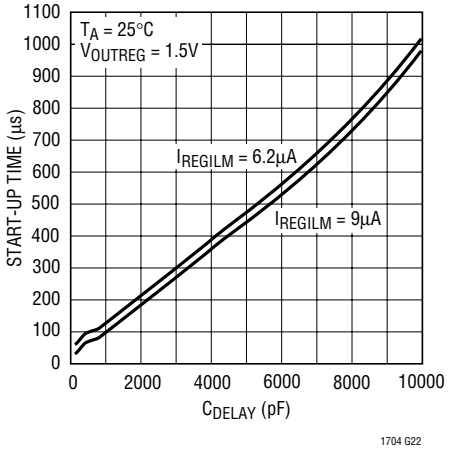
V_{OUTREG} 0.1A to 2.1A Load Step



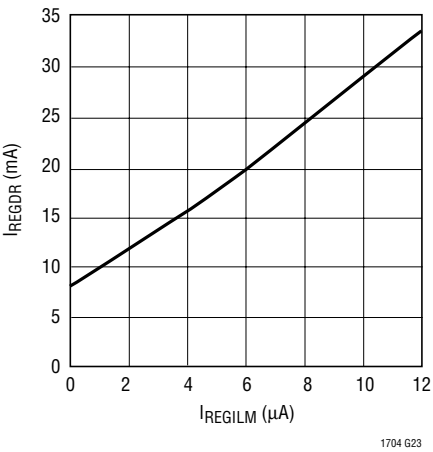
Minimum V_{CC} vs V_{OUTREG}



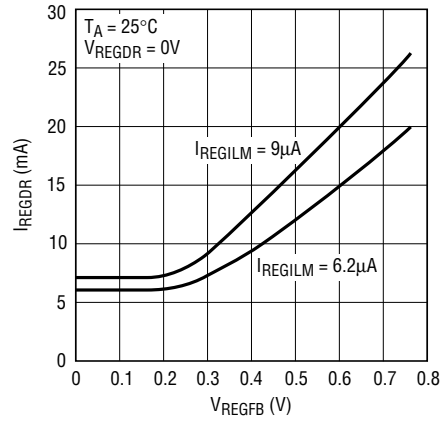
Linear Regulator Start-Up Time vs C_{DELAY}



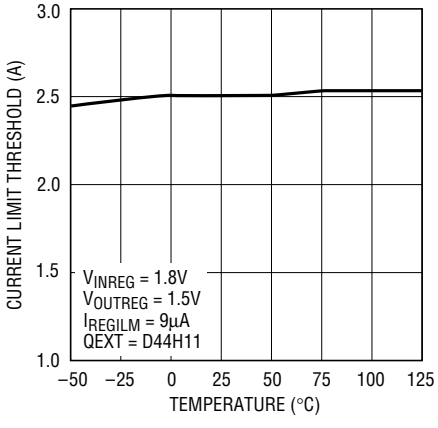
I_{REGDR} vs I_{REGILM}



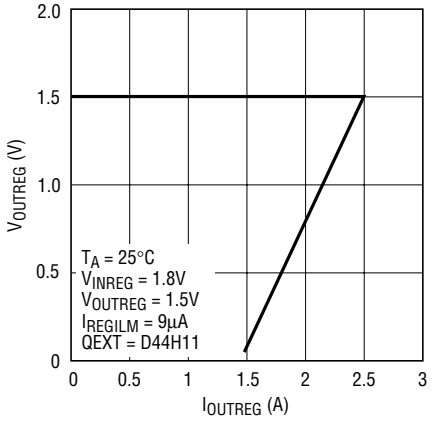
I_{REGDR} vs V_{REGFB}



Linear Regulator Current Limit Threshold vs Temperature

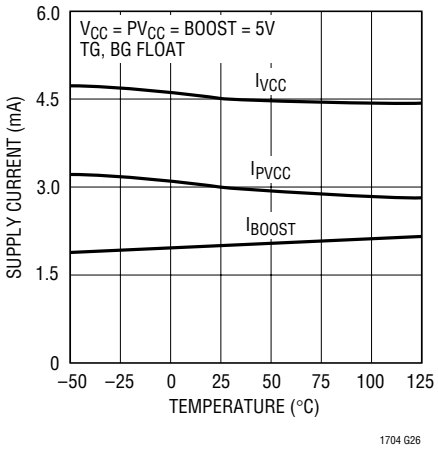


V_{OUTREG} vs Load Current

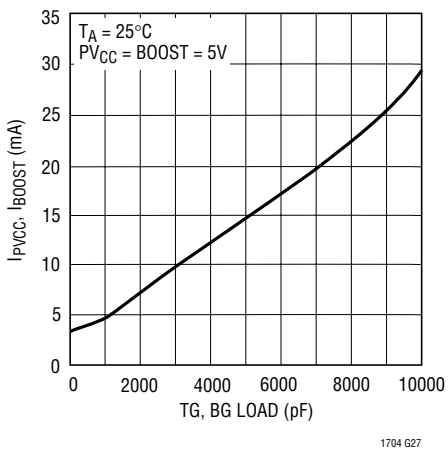


TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



I_{PVCC}, I_{BOOST} vs Driver Load



PIN FUNCTIONS

TG (Pin 1): Switcher Controller Top Gate Drive. The TG pin drives the gate of the top N-channel MOSFET, QT. The TG driver draws power from the BOOST pin and returns it to the SW pin, providing true floating drive to QT. TG is designed to typically drive up to 10,000pF of gate capacitance.

SW (Pin 2): Switcher Controller Switching Node. Connect SW to the switching node of the main converter. The TG driver ground returns to SW, providing floating gate drive to the top N-channel MOSFET, QT. The voltage at SW is compared to I_{MAX} by the current limit comparator while the bottom MOSFET, QB is on. The Burst comparator (BURST, see Block Diagram) monitors the potential at SW and switches to Burst Mode operation under light load conditions.

I_{MAX} (Pin 3): Switcher Controller Current Limit Set. The I_{MAX} pin sets the current limit comparator threshold for the switcher controller. If the voltage drop across the bottom MOSFET, QB, exceeds the magnitude of the voltage at I_{MAX}, the switcher controller enters current limit. The I_{MAX} pin has an internal 10μA current source pull-up, allowing the current threshold to be set with a single external resistor to PGND. Kelvin connect this current setting resistor to the source of QB. Refer to the Current Limit Programming section for more information on choosing R_{IMAX}.

RUN/SS (Pin 4): Switcher Controller Soft-Start. A capacitor from RUN/SS to GND controls the turn-on time and rate of rise of the switcher output voltage at power up. An internal 3μA current source pull-up at RUN/SS sets the turn-on time at approximately 300ms/μF. If both RUN/SS and REGILM are pulled low, the LTC1704 enters shutdown mode.

COMP (Pin 5): Switcher Controller Loop Compensation. The COMP pin is connected directly to the output of the switcher controller's error amplifier and the input to the PWM comparator. Use an RC network between the COMP pin and the FB pin to compensate the feedback loop for optimum transient response.

FB (Pin 6): Switcher Controller Feedback Input. FB should be connected through a resistor divider network to V_{OUTSW} to set the switcher output voltage. Also, connect the switcher loop compensation network to FB.

REGDR (Pin 7): Linear Regulator Controller Driver Output. Connect REGDR to the base of the external NPN Pass transistor. The REGILM pin input current controls the linear regulator controller maximum driving capability.

GND (Pin 8): Signal Ground. All internal low power circuitry returns to the GND pin. Connect to a low impedance ground, separated from the PGND node. All feedback,

PIN FUNCTIONS

compensation and soft-start connections should return to GND. GND and PGND should connect only at a single point, near the PGND pin and the negative plate of the V_{IN} bypass capacitor.

REGFB (Pin 9): Linear Regulator Controller Feedback Input. REGFB should be connected through a resistor divider network to V_{OUTREG} to set the output voltage of the linear regulator.

REGILM (Pin 10): Linear Regulator Controller Current Limit Setting cum ON/OFF Control. This pin is internally servoed to 0.8V. An external resistor R_{REGILM} between V_{CC} and REGILM programs the REGILM pin input current. This current determines the maximum pass transistor base current and directly controls the linear regulator current sourcing capabilitiy. An external capacitor, C_{DELAY} is added to this pin to control the turn-on time of the linear regulator, the minimum value for this capacitor is 100pF. Refer to the Linear Regulator Current Limit Programming section for more information on choosing R_{REGILM} and C_{DELAY}. Pulling REGILM to GND turns off the linear regulator. If both RUN/SS and REGILM are pulled low, the LTC1704 enters shutdown mode.

V_{CC} (Pin 11): Power Supply Input. All internal circuits except the switcher output drivers are powered from this pin. V_{CC} should be connected to a low noise 5V supply, and should be bypassed to GND with at least a 10µF capacitor in close proximity to the LTC1704.

PGOOD (Pin 12): Power Good. PGOOD is an open-drain logic output. PGOOD pulls low if any of the two supply outputs are outside ±10% of their nominal levels. An external pull-up resistor is required at PGOOD to allow it to swing positive.

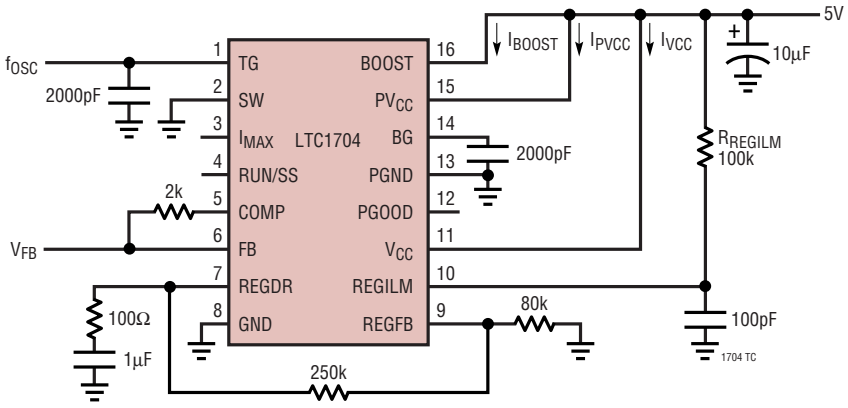
PGND (Pin 13): Power Ground. The BG driver returns to this pin. Connect PGND to a high current ground node in close proximity to the sources of external MOSFET QB, and the V_{IN} and V_{OUTSW} bypass capacitors.

BG (Pin 14): Switcher Controller Bottom Gate Drive. The BG pin drives the gate of the bottom N-channel synchronous switch MOSFET, QB. BG is designed to typically drive up to 10,000pF of gate capacitance.

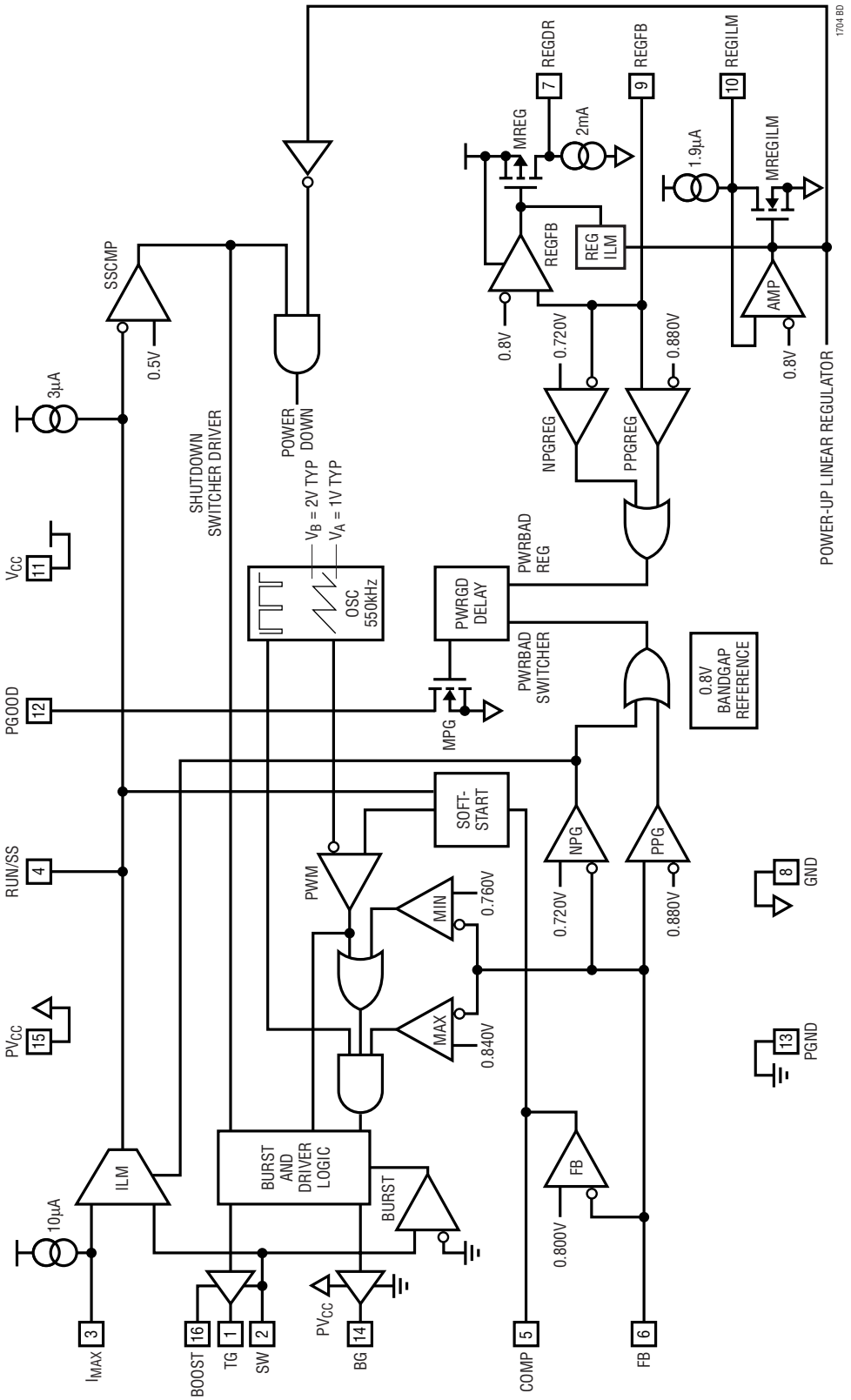
PV_{CC} (Pin 15): Switcher Controller Bottom Gate Driver Supply. PV_{CC} provides power to the BG output driver. PV_{CC} must be connected to a voltage high enough to fully turn on the external MOSFET, QB. PV_{CC} should generally be connected directly to V_{IN}, the main system 5V supply. PV_{CC} requires at least a 10µF bypass capacitor directly to PGND.

BOOST (Pin 16): Switcher Controller Top Gate Driver Supply. The BOOST pin supplies power to the floating TG driver. Bypass BOOST to SW with a 1µF capacitor. An external Schottky diode from V_{IN} to BOOST creates a complete floating charge-pumped supply at BOOST. No other external supplies are required.

TEST CIRCUIT



BLOCK DIAGRAM



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OVERVIEW

The LTC1704 includes a step-down (buck), voltage mode feedback switching regulator controller and a linear regulator controller. The switching regulator controller employs a synchronous switching architecture with two external N-channel MOSFETs. The chip operates from a low voltage input supply (6V maximum) and provides high power, high efficiency, precisely regulated output voltage. The switcher output regulation is extremely tight, with initial accuracy and DC line and load regulation and better than 1.5%. Total regulation, including transient response, is inside of 3.5% with a properly designed circuit. The 550kHz switching frequency allows the use of physically small, low value external components without compromising performance.

The LTC1704's internal feedback amplifier is a 20MHz gain bandwidth op amp, allowing the use of complex multipole/zero compensation networks. This allows the feedback loop to maintain acceptable phase margin at higher frequencies than traditional switching regulator controllers, improving stability and maximizing transient response. The 800mV internal reference allows regulated output voltages as low as 800mV without external level shifting amplifiers. The LTC1704's synchronous switching logic transitions automatically into Burst Mode operation, maximizing efficiency with light loads.

The linear regulator controller drives an external NPN pass transistor to provide a programmable output voltage up to 2A of current. An external pull-up resistor programs the current limit threshold for the linear regulator. Under short-circuit condition, the foldback current limit circuitry prevents excessive pass transistor heating. The switcher and the linear regulator can be individually disabled. When both controllers are disabled, the LTC1704 enters shutdown mode and the supply current reduces to 75μA. An onboard power good (PGOOD) flag goes high when both outputs are regulating.

Small Footprint

The LTC1704 switcher supply operates at a 550kHz switching frequency, allowing it to use low value inductors without generating excessive ripple currents. Because the inductor stores less energy per cycle, the physical size of the inductor can be reduced without risking core saturation, saving PCB board space. The high operating frequency also means less energy is stored in the output capacitors between cycles, minimizing their required value and size. The remaining components, including the LTC1704, are tiny, allowing an entire power convertor to be constructed in $1.5in^2$ of PCB space.

Fast Transient Response

The LTC1704 switcher supply uses a fast 20MHz GBW op amp as an error amplifier. This allows the compensation network to be designed with several poles and zeros in a more flexible configuration than with a typical g_m feedback amplifier. The high bandwidth of the amplifier, coupled with the high switching frequency and the low values of the external inductor and output capacitor, allow very high loop crossover frequencies. The low inductor value is the other half of the equation—with a typical value on the order of 1μH, the inductor allows very fast di/dt slew rates. The result is superior transient response compared with conventional solutions.

High Efficiency

The LTC1704 switcher supply uses a synchronous step-down (buck) architecture, with two external N-channel MOSFETs. A floating topside driver and a simple external charge pump provide full gate drive to the upper MOSFET. The voltage mode feedback loop and MOSFET V_{DS} current limit sensing remove the need for an external current sense resistor, eliminating an external component and a source of power loss in the high current path. Properly designed circuits using low gate charge MOSFETs are capable of efficiencies exceeding 90% over a wide range of output voltages.

Linear Regulator Controller

The LTC1704 linear regulator controller drives an external NPN pass transistor in emitter-follower configuration to provide an externally adjustable output voltage. The controller senses the output voltage via the REGFB pin, drives the base of the NPN through the REGDR pin to regulate the REGFB pin to 0.8V. REGDR is capable of sourcing more than 30mA of base current to the external NPN.

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Overcurrent protection is achieved by limiting the drive current. The input current at the REGILM pin programs the current limit threshold. Refer to the Linear Regulator Supply Current Limit Programming section for more information on choosing R_{REGILM}. The linear regulator controller employs a foldback current limit scheme for overcurrent protection. Under a short-circuit condition, the external NPN transistor is subjected to the full input voltage across its collector-emitter terminal. This increases the power dissipation of the NPN and may eventually cause damage to the transistor. LTC1704 overcomes this problem by using a foldback current limit scheme whereby the available drive current is reduced as the output voltage at REGFB pin drops. This limits the power dissipation and prevents catastrophic damage to the external NPN.

ARCHITECTURE DETAILS

Switcher Supply Architecture

The LTC1704 switcher supply is designed to operate as a synchronous buck converter (Figure 1). The controller includes two high power MOSFET gate drivers to control the external N-channel MOSFETs QT and QB. The drivers have 0.5Ω output impedances and can carry over an amp of continuous current with peak currents up to 5A to slew large MOSFET gates quickly. The drain of QT is connected to the input supply and the source of QT connected to the switching node SW. QB is the synchronous rectifier with its drain at SW and its source at PGND. SW is connected to one end of the inductor, with the other end connected to V_{OUTSW}. The output capacitor is connected from V_{OUTSW} to PGND.

When a switching cycle begins, QB is turned off and QT is turned on. SW rises almost immediately to V_{IN} and the inductor current begins to increase. When the PWM pulse completes, QT turns off and one nonoverlap interval later, QB turns on. Now SW drops to PGND and the inductor current decreases. The cycle repeats with the next tick of the master clock. The percentage of time spent in each mode is controlled by the duty cycle of the PWM signal, which in turn is controlled by the feedback amplifier. The master clock runs at a 550kHz rate and turns QT once every 1.8µs. In a typical application with a 5V input and a 1.5V output, the duty cycle will be set at 1.5/5 • 100% or 30% by the feedback loop. This will give roughly a 540ns on-time for QT and a 1.26µs on-time for QB.

This constant frequency operation brings with it a couple of benefits. Inductor and capacitor values can be chosen with a precise operating frequency in mind and the feedback loop components can be similarly tightly specified. Noise generated by the circuit will always be in a known frequency band with the 550kHz frequency designed to leave the 455kHz IF band free of interference. Subharmonic oscillation and slope compensation, common headaches with constant frequency current mode switchers, are absent in voltage mode designs like the LTC1704. During the time that QT is on, its source (the SW pin) is at V_{IN}. V_{IN} is also the power supply for the LTC1704. However, QT requires $V_{IN} + V_{GS(ON)}$ at its gate to achieve minimum R_{ON}. The LTC1704, needs to generate a gate drive signal at TG higher than its highest supply voltage. To accomplish this, the TG driver runs from floating supplies, with its negative supply attached to SW and its power supply at BOOST. This allows it to slew up and down with the source of QT.

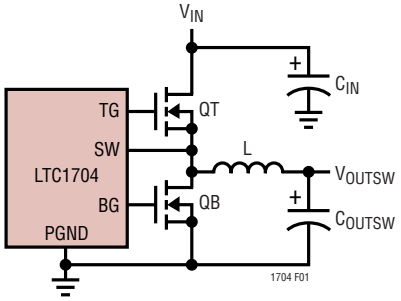

Figure 1. Synchronous Buck Architecture

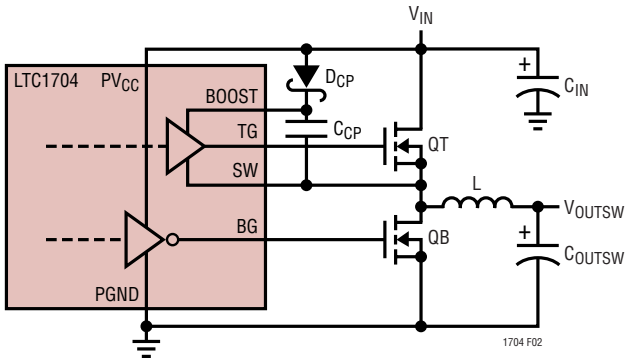

Figure 2. Floating TG Driver Supply

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In combination with a simple external charge pump (Figure 2), this allows the LTC1704 to completely enhance the gate of QT without requiring an additional, higher supply voltage.

Switcher Supply Feedback Amplifier

The LTC1704 senses the switcher output voltage at V_{OUTSW} with an internal feedback op amp (see Block Diagram). This is a real op amp with a low impedance output, 85dB open-loop gain and 20MHz gain bandwidth product. The positive input is connected internally to an 800mV reference, while the negative input is connected to the FB pin. The output is connected to COMP, which is in turn connected to the soft-start circuitry and from there to the PWM generator. The switching regulator output voltage can be obtained using the following equation:

$$V_{OUTSW} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right)$$

Unlike many regulators that use a resistor divider connected to a high impedance feedback input, the LTC1704 switcher supply is designed to use an inverting summing amplifier topology with the FB pin configured as a virtual ground. This allows flexibility in choosing pole and zero locations not available with simple g_m configurations. In particular, it allows the use of "Type 3" compensation, which provides a phase boost at the LC pole frequency and significantly improves loop phase margin (refer to Figure 3).

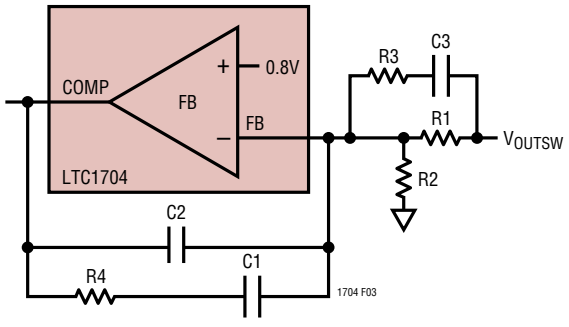

Figure 3. "Type 3" Feedback Loop

Switcher Supply MIN/MAX Comparators

Two additional feedback loops in the switcher supply keep an eye on the primary feedback amplifier and step in if the feedback node moves ±5% from its nominal 800mV value. The MAX comparator (see Block Diagram) activates whenever FB rises more than 5% above 800mV. It immediately turns the top MOSFET (QT) off and the bottom MOSFET (QB) on and keeps them that way until FB falls back within 5% of its nominal value. This pulls the output down as fast as possible, preventing damage to the (often expensive) load. If FB rises because the output is shorted to a higher supply, QB will stay on until the short goes away, the higher supply current limits or QB dies trying to save the load. This behavior provides maximum protection against overvoltage faults at the output, while allowing the circuit to resume normal operation when the fault is removed.

The MIN comparator (see Block Diagram) trips whenever FB is more than 5% below 800mV and immediately forces the switch duty cycle to 90% to bring the output voltage back into range. It releases when FB is within the 5% window. MIN is disabled when the soft-start or current limit circuits are active—the only two times that the output should legitimately be below its regulated value.

Notice that the FB pin is the virtual ground node of the feedback amplifier. A typical compensation network does not include local DC feedback around the amplifier, so that the DC level at FB will be an accurate replica of the output voltage, divided down by R1 and R2 (Figure 3). However, the compensation capacitors will tend to attenuate AC signals at FB, especially with low bandwidth Type 1 feedback loops. This creates a situation where the MIN and MAX comparators do not respond immediately to shifts in the output voltage, since they monitor the output at FB.

PGOOD Flag

The LTC1704 comes with a power good pin (PGOOD). PGOOD is an open-drain output, and requires an external pull-up resistor. If both the regulators are within ±10% from their nominal value, the transistor MPG shuts off (see Block Diagram), and PGOOD is pulled high by the external pull-up resistor. If any of the two outputs is more than 10% outside the nominal value for more than 1μs, PGOOD pulls

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low, indicating that the output is out of regulation. For PGOOD to go high, both the outputs must be in regulation for more than 20µs. PGOOD remains active during soft-start and current limit. Upon power-up, PGOOD is forced low. As soon as the RUN/SS and REGILM pins rise above the shutdown thresholds, the two pairs of power good comparators take over and control the transistor MPG directly. The 1µs and 20µs delay ensures that short output transient glitches that are successfully "caught" by the power good comparators don't cause momentary glitches at the PGOOD pin.

Shutdown/Soft-Start

The RUN/SS pin performs two functions: when pulled to ground, it shuts down the switcher drivers, and acts as a conventional soft-start pin, enforcing a maximum duty cycle limit proportional to the voltage at RUN/SS. An internal 3µA current source pull-up is connected to the RUN/SS pin, allowing a soft-start ramp to be generated with a single external capacitor to ground. The 3µA current source is active even when the LTC1704 is shut down, ensuring the device will start when any external pull-down at RUN/SS is released.

The RUN/SS pin shuts down the switcher drivers when it falls below 0.5V (Figure 4). Between 0.5V and about 1V, the LTC1704 wakes up and the duty cycle is kept to minimum. As the potential at RUN/SS goes higher, the duty cycle increases linearly between 1V and 2V, reaching its final value of 90% when RUN/SS is above 2V. Somewhere before this point, the feedback amplifier will assume control of the loop and the output will come into regulation. When RUN/SS rises to 1V below V_{CC} , the MIN feedback comparator is enabled, and the LTC1704 voltage feedback loop is in full operation.

Switcher Supply Current Limit

The LTC1704 switcher supply includes an onboard current limit circuit that limits the maximum output current to a user-programmed level. It works by sensing the voltage drop across QB during the time that QB is on and comparing that voltage to a user-programmed voltage at I_{MAX}. Since QB looks like a low value resistor during its on-time, the voltage drop across it is proportional to the current flowing in it. In a buck converter, the average current in the inductor is equal to the output current. This current also flows through QB during its on-time. Thus, by watching the voltage across QB, the LTC1704 can monitor the output current.

Any time QB is on and the current flowing to the output is reasonably large, the SW node at the drain of QB will be somewhat negative with respect to PGND. The LTC1704 senses this voltage and inverts it to allow it to compare the sensed voltage with a positive voltage at the I_{MAX} pin. The I_{MAX} pin includes a trimmed 10µA pull-up, enabling the user to set the voltage at I_{MAX} with a single resistor, R_{IMAX}, to ground. The LTC1704 compares the two inputs and begins limiting the output current when the magnitude of the negative voltage at the SW pin is greater than the voltage at I_{MAX}.

The current limit detector is connected to an internal gm amplifier that pulls a current from the RUN/SS pin proportional to the difference in voltage magnitudes between the SW and I_{MAX} pins. This current begins to discharge the soft-start capacitor at RUN/SS, reducing the duty cycle and controlling the output voltage until the current drops below the limit. The soft-start capacitor needs to move a fair amount before it has any effect on the duty cycle, adding a delay until the current limit takes effect (Figure 4). This allows the LTC1704 to experience brief overload conditions without affecting the output voltage regulation.

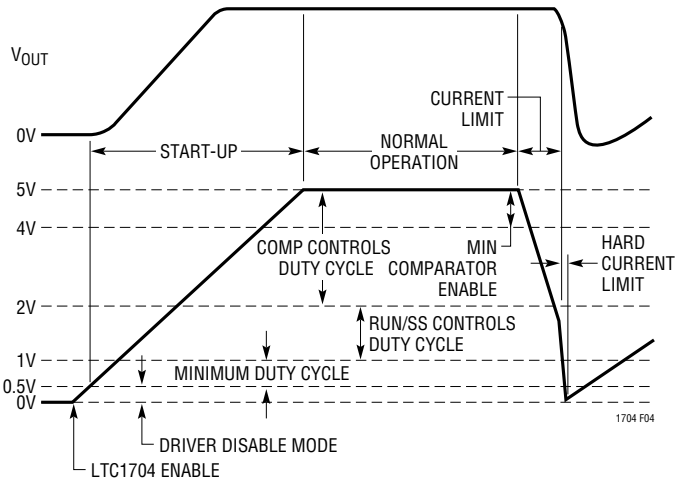

Figure 4. Soft-Start Operation in Start Up and Current Limit

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The delay also acts as a pole in the current limit loop to enhance loop stability. Prolonged overload conditions will allow the RUN/SS pin to reach a steady state, and the output will remain at a reduced voltage until the overload is removed. Under current limit condition, if the output voltage is less than 10% of its normal value, the soft-start capacitor will be forced low immediately and the LTC1704 will rerun a complete soft-start cycle. The soft-start capacitor must be selected such that during power-up the current through QB will not exceed the current limit value.

Power MOSFET $R_{DS(ON)}$ varies from MOSFET to MOSFET, limiting the accuracy obtainable from the LTC1704 current limit loop. Additionally, ringing on the SW node due to parasitics can add to the apparent current, causing the loop to engage early. When the load current increases abruptly, the voltage feedback loop forces the duty cycle to increase rapidly and the on-time of QB will be small momentarily. The $R_{DS(ON)}$ of QB must be low enough to ensure that the SW node is pulled low within the QB on-time for proper current sensing. The LTC1704 current limit is designed primarily as a disaster prevention, "no blow-up" circuit, and is not useful as a precision current regulator. It should typically be set around 50% above the maximum expected normal output current to prevent component tolerances from encroaching on the normal current range. See the Switching Supply Current Limit Programming section for advice on choosing a valve for R_{IMAX}.

BURST MODE OPERATION (For Non-B Parts Only)

Theory of Operation

The LTC1704 (non-B part) switcher supply has two modes of operation. Under heavy loads, it operates as a fully synchronous, continuous conduction switching regulator. In this mode of operation ("Continuous" mode), the current in the inductor flows in the positive direction (toward the output) during the entire switching cycle, constantly supplying current to the load. In this mode, the synchronous switch (QB) is on whenever QT is off, so the current always flows through a low impedance switch, minimizing voltage drop and power loss. This is the most efficient mode of operation at heavy loads, where the resistive losses in the power devices are the dominant loss term.

Continuous mode works efficiently when the load current is greater than half of the ripple current in the inductor. In a buck converter like the LTC1704, the average current in the inductor (averaged over one switching cycle) is equal to the load current. The ripple current is the difference between the maximum and the minimum current during a switching cycle (see Figure 5a). The ripple current depends on inductor value, clock frequency and output voltage, but is constant regardless of load as long as the LTC1704 remains in Continuous mode. See the Inductor Selection section for a detailed description of ripple current.

As the output load current decreases in Continuous mode, the average current in the inductor will reach a point where it drops below half the ripple current. At this point, the current in the inductor will reverse during a portion of the switching cycle, or begin to flow from the output back to the input. This does not adversely affect regulation, but does cause additional losses as a portion of the inductor current flows back and forth through the resistive power switches, giving away a little more power each time and lowering the efficiency. There are some benefits to allowing this reverse current flow: the circuit will maintain regulation even if the load current drops below zero (the load supplies current to the LTC1704) and the output ripple voltage and frequency remain constant at all loads, easing filtering requirements.

Besides the reverse current loss, the LTC1704 drivers are still switching QT and QB on and off once a cycle. Each time an external MOSFET is turned on, the internal driver must charge its gate to PV_{CC}. Each time it is turned off, that charge is lost to ground. At the high switching frequency that the LTC1704 operates, the charge lost to the gates can add up to tens of milliamps from PV_{CC}. As the load current continues to drop, this quickly becomes the dominant power loss term, reducing efficiency once again.

To minimize the efficiency loss due to switching loss and reverse current flow at light loads, the LTC1704 (non-B part) switches to a second mode of operation: Burst Mode operation (Figure 5b). In Burst Mode operation, the LTC1704 detects when the inductor current approaches zero and turns off both drivers. During this time, the voltage at the SW pin will float around V_{OUTSW}, the voltage

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across the inductor will be zero, and the inductor current remains zero. This prevents current from flowing backwards in QB, eliminating that power loss term. It also reduces the ripple current in the inductor as the output current approaches zero.

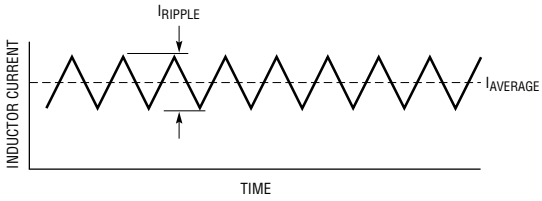

Figure 5a. Continous Mode

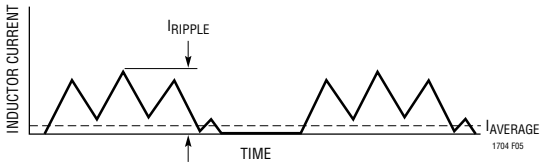

Figure 5b. Burst Mode Operation

The LTC1704B does not shift into Burst Mode operation at light loads, eliminating low frequency output ripple at the expense of light load efficiency.

The LTC1704 detects when the inductor current has reached zero by monitoring the voltage at the SW pin while QB is on (see BURST in Block Diagram). Since QB acts like a resistor, SW should ideally be right at 0V when the inductor current reaches zero. In reality, the SW node will ring to some degree immediately after it is switched to ground by QB, causing some uncertainty as to the actual moment the average current in QB goes to zero. The LTC1704 minimizes this effect by turning on the Burst Comparator only at the last 180ns of the switching period, before QB turns off. In addition, the Burst Comparator is disabled if QB turns on for less than 200ns. Despite this, care must still be taken in the PCB layout to ensure that proper kelvin sensing for the SW pin is provided. Connect the SW pin of the LTC1704 as close to the drain of QB as possible through a thick trace. The same applies to the PGND pin of the LTC1704, which is the negative input of the burst comparator and it should be connected close to the source of QB through a thick trace. Ringing on the PGND pin due to an insufficient PV_{CC} bypass capacitor can also cause the burst comparator to trip prematurely. Connect at least a 10µF bypass capacitor directly from the PV_{CC} pin to PGND.

The burst comparator is turned on only at the last 180ns of the switching period, the propagation delay of the comparator is designed to be fast so that a zero or low positive voltage on the SW node can trip the comparator within this 180ns. Low inductor ripple current coupled with low MOSFET $R_{DS(ON)}$ may prolong the delay of the burst comparator and prevent the comparator from tripping. To overcome this, reduce the inductor value to increase the ripple current and the SW node voltage change.

The moment LTC1704 (non-B parts) enters Burst Mode operation, both drivers skip several switching cycles until the output droops. Once the voltage feedback loop requests for an additional 10% duty cycle, the LTC1704 enters Continuous mode operation again. To eliminate audible noise from certain types of inductors when they are lightly loaded, LTC1704 includes an internal timer that forces Continuous mode operation every 15µs.

In Burst Mode operation, both resistive loss and switching loss are minimized while keeping the output in regulation. The total deviation from the regulated output is within the 1.5% regulation tolerance of the LTC1704. As the load current falls to zero in Burst Mode operation, the most significant loss term becomes the 4.5mA quiescent current drawn by the LTC1704—usually much less than the minimum load current in a typical low voltage logic system. Burst Mode operation maximizes efficiency at low load currents, but can cause low frequency ripple in the output voltage as the cycle-skipping circuitry switches on and off.

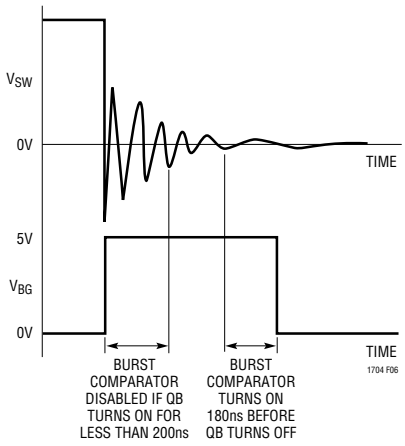

Figure 6. Burst Comparator Turns On 180ns Before QB Turns Off

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Maximizing High Load Current Efficiency

Efficiency at high load currents is primarily controlled by the resistance of the components in the power path (QT, QB, L) and power lost in the gate drive circuits due to MOSFET gate charge. Maximizing efficiency in this region of operation is as simple as minimizing these terms.

The behavior of the load over time affects the efficiency strategy. Parasitic resistances in the MOSFETs and the inductor set the maximum output current the circuit can supply without burning up. A typical efficiency curve shows that peak efficiency occurs near 30% of this maximum current. If the load current will vary around the efficiency peak and spend relatively little time at the maximum load, choosing components so that the average load is at the efficiency peak is a good idea. This puts the maximum load well beyond the efficiency peak, but usually gives the greatest system efficiency over time, which translates to the longest run time in a battery-powered system. If the load is expected to be relatively constant at the maximum level, the components should be chosen so that this load lands at the peak efficiency point, well below the maximum possible output of the converter.

Maximizing Low Load Current Efficiency

Low load current efficiency depends strongly on proper operation in Burst Mode operation. In an ideally optimized system, when Burst Mode operation is activated, gate drive is the dominant loss term. Burst Mode operation turns off all output switching for several clock cycles in a row, significantly cutting gate drive losses. As the load current in Burst Mode operation falls toward zero, the current drawn by the circuit falls to the LTC1704's background quiescent level, about 4.5mA.

To maximize low load efficiency, make sure the LTC1704 (non-B part) is allowed to enter Burst Mode operation as cleanly as possible. Minimize ringing at the SW node so that the Burst comparator leaves as little residual current in the inductor as possible when QB turns off. It helps to connect the SW pin of the LTC1704 as close to the drain of QB as possible. An RC snubber network can also be added from SW to PGND.

SWITCHER SUPPLY EXTERNAL COMPONENT SELECTION

Power MOSFETs Selection

Getting peak efficiency out of the LTC1704 switcher supply depends strongly on the external MOSFETs used. The LTC1704 requires at least two external MOSFETs—more if one or more of the MOSFETs are paralleled to lower on-resistance. To work efficiently, these MOSFETs must exhibit low $R_{DS(ON)}$ at 5V V_{GS} to minimize resistive power loss while they are conducting current. They must also have low gate charge to minimize transition losses during switching. On the other hand, voltage breakdown requirements in a typical LTC1704 circuit are pretty tame; the 6V maximum input voltage limits the V_{DS} and V_{GS} the MOSFETs can see to safe levels for most devices.

Low $R_{DS(ON)}$

$R_{DS(ON)}$ calculations are pretty straightforward. $R_{DS(ON)}$ is the resistance from the drain to the source of the MOSFET when the gate is fully on. Many MOSFETs have $R_{DS(ON)}$ specified at 4.5V gate drive—this is the right number to use in LTC1704 circuits running from a 5V supply. As current flows through this resistance while the MOSFET is on, it generates I^2R watts of heat, where I is the current flowing (usually equal to the output current) and R is the MOSFET $R_{DS(ON)}$. This heat is only generated when the MOSFET is on. When it is off, the current is zero and the power lost is also zero (and the other MOSFET is busy losing power).

This lost power does two things: it subtracts from the power available at the output, costing efficiency, and it makes the MOSFET hotter, both bad things. The effect is worst at maximum load when the current in the MOSFETs and thus the power lost, are at a maximum. Lowering $R_{DS(ON)}$ improves heavy load efficiency at the expense of additional gate charge (usually) and more cost (usually). Proper choice of MOSFET $R_{DS(ON)}$ becomes a trade-off between tolerable efficiency loss, power dissipation and cost. Note that while the lost power has a significant effect on system efficiency, it only adds up to a watt or two in a typical LTC1704 circuit, allowing the use of small, surface mount MOSFETs without heat sinks.

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Gate Charge

Gate charge is amount of charge (essentially, the number of electrons) that the LTC1704 needs to put into the gate of an external MOSFET to turn it on. The easiest way to visualize gate charge is to think of it as a capacitance from the gate pin of the MOSFET to SW (for QT) or to PGND (for QB). This capacitance is composed of MOSFET channel charge, actual parasitic drain-source capacitance and Miller-multiplied gate-drain capacitance, but can be approximated as a single capacitance from gate to source. Regardless of where the charge is going, the fact remains that it all has to come out of PV_{CC} to turn the MOSFET gate on, and when the MOSFET is turned back off, that charge all ends up at ground. In the meanwhile, it travels through the LTC1704's gate drivers, heating them up. More power lost!

In this case, the power is lost in little bite-sized chunks, one chunk per switch per cycle, with the size of the chunk set by the gate charge of the MOSFET. Every time the MOSFET switches, another chunk is lost. Clearly, the faster the clock runs, the more important gate charge becomes as a loss term. Old fashioned switchers that ran at 20kHz could pretty much ignore gate charge as a loss term. In the 550kHz LTC1704, gate charge loss can be a significant efficiency penalty. Gate charge loss can be the dominant loss term at medium load currents, especially with large MOSFETs. Gate charge loss is also the primary cause of power dissipation in the LTC1704 itself.

TG Charge Pump

There's another nuance of MOSFET drive that the LTC1704 needs to get around. The LTC1704 is designed to use N-channel MOSFETs for both QT and QB, primarily because N-channel MOSFETs generally cost less and have lower $R_{DS(ON)}$ than similar P-channel MOSFETs. Turning QB on is no big deal since the source of QB is attached to PGND; the LTC1704 just switches the BG pin between PGND and PV_{CC}. Driving QT is another matter. The source of QT is connected to SW which rises to V_{IN} when QT is on. To keep QT on, the LTC1704 must get TG one MOSFET $V_{GS(ON)}$ above V_{IN}. It does this by utilizing a floating driver with the negative lead of the driver attached to SW (the source of QT) and the PV_{CC} lead of the driver coming out separately at BOOST. An external 1µF capacitor (C_{CP}) connected between SW and BOOST (Figure 2) supplies power to BOOST when SW is high, and recharges itself through DCP when SW is low. This simple charge pump keeps the TG driver alive even as it swings well above V_{IN}. The value of the bootstrap capacitor C_{CP} needs to be at least 100 times that of the total input capacitance of the topside MOSFET(s). For very large external MOSFETs (or multiple MOSFETs in parallel), C_{CP} may need to be increased beyond the 1µF value.

Input Supply

The BiCMOS process that allows the LTC1704 switcher supply to include large MOSFET drivers on-chip also limits the maximum input voltage to 6V. This limits the practical maximum input supply to a loosely regulated 5V or 6V rail. At the same time, the input supply needs to supply several amps of current without excessive voltage drop. The input supply must have regulation adequate to prevent sudden load changes from causing the LTC1704 input voltage to dip. In most typical applications where the LTC1704 is generating a secondary low voltage logic supply, all of these input conditions are met by the main system logic supply when fortified with an input bypass capacitor.

Input Bypass Capacitor Selection

A typical LTC1704 circuit running from a 5V logic supply might provide 1.6V at 10A at its switcher output. 5V to 1.6V implies a duty cycle of 32%, which means QT is on 32% of each switching cycle. During QT's on-time, the current drawn from the input equals the load current and during the rest of the cycle, the current drawn from the input is near zero. This 0A to 10A, 32% duty cycle pulse train results in $4.66A_{RMS}$ ripple current. At 550kHz, switching cycles last about 1.8µs; most system logic supplies have no hope of regulating output current with that kind of speed. A local input bypass capacitor is required to make up the difference and prevent the input supply from dropping drastically when QT kicks on. This capacitor is usually chosen for RMS ripple current capability and ESR as well as value.

Consider our 10A example. The input bypass capacitor gets exercised in three ways: its ESR must be low enough

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to keep the initial drop as QT turns on within reason (100mV or so); its RMS current capability must be adequate to withstand the 4.66A capacitor ripple current is not the same as input RMS current at the input and the capacitance must be large enough to maintain the input voltage until the input supply can make up the difference. Generally, a capacitor that meets the first two parameters will have far more capacitance than is required to keep capacitance-based droop under control. In our example, we need 0.01Ω ESR to keep the input drop under 100mV with a 10A current step and $5.65A_{RMS}$ ripple current capacity to avoid overheating the capacitor. These requirements can be met with multiple low ESR tantalum or electrolytic capacitors in parallel, or with a large monolithic ceramic capacitor.

$$I_{RMSIN} = 5.65$$

$$I_{DCIN} = 3.2A$$

$$I_{RIPP} = \sqrt{(5.65)^2 - (3.2)^2} = 4.66A_{RMS}$$

Tantalum capacitors are a popular choice as input capacitors for LTC1704 applications, but they deserve a special caution here. Generic tantalum capacitors have a destructive failure mechanism when they are subjected to large RMS currents (like those seen at the input of an LTC1704). At some random time after they are turned on, they can blow up for no apparent reason. The capacitor manufacturers are aware of this and sell special "surge tested" tantalum capacitors specifically designed for use with switching regulators. When choosing a tantalum input capacitor, make sure that it is rated to carry the RMS current that the LTC1704 will draw. If the data sheet doesn't give an RMS current rating, chances are the capacitor isn't surge tested. Don't use it!

Output Bypass Capacitor Selection

The output bypass capacitor has quite different requirements from the input capacitor. The ripple current at the output of a buck regulator, like the LTC1704's switcher controller, is much lower than at the input because the inductor current is constantly flowing at the output whenever the LTC1704 is operating in Continuous mode. The primary concern at the output is capacitor ESR. Fast load current transitions at the output will appear as voltage across the ESR of the output bypass capacitor until the feedback loop in the LTC1704 can change the inductor current to match the new load current value. This ESR step at the output is often the single largest budget item in the load regulation calculation. As an example, our hypothetical 1.6V, 10A switcher with a 0.01Ω ESR output capacitor would experience a 100mV step at the output with a 0A to 10A load step—a 6.3% output change!

Usually the solution is to parallel several capacitors at the output. For example, to keep the transient response inside of 3% with the previous design, we'd need an output ESR better than 0.0048Ω. This can be met with three 0.014Ω, 470µF tantalum capacitors in parallel.

Inductor Selection

The inductor in a typical LTC1704 circuit is chosen primarily for value and saturation current. The inductor value sets the ripple current, which is commonly chosen at around 40% of the anticipated full load current. Ripple current is set by:

$$I_{RIPPLE} = \frac{t_{ON(QB)}(V_{OUT})}{L}$$

In our hypothetical 1.6V, 10A example, we'd set the ripple to 40% of 10A or 4A, and the inductor value would be:

$$L = \frac{t_{ON(QB)}(V_{OUT})}{I_{RIPPLE}} = \frac{(1.2\mu s)(1.6V)}{4A} = 0.5\mu H$$

$$\text{with} \quad t_{ON(QB)} = \left(1 - \frac{1.6V}{5V}\right)/550kHz = 1.2\mu s$$

The inductor must not saturate at the expected peak current. In this case, if the current limit was set to 15A, the inductor should be rated to withstand 15A + $1/2I_{RIPPLE}$, or 17A without saturating.

FEEDBACK LOOP/COMPENSATION

Feedback Loop Types

In a typical LTC1704 switcher circuit, the feedback loop consists of the modulator, the external inductor and output capacitor, and the feedback amplifier and its com-

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pensation network. All of these components affect loop behavior and need to be accounted for in the loop compensation. The modulator consists of the internal PWM generator, the output MOSFET drivers and the external MOSFETs themselves. From a feedback loop point of view, it looks like a linear voltage transfer function from COMP to SW and has a gain roughly equal to the input voltage. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency.

The external inductor/output capacitor combination makes a more significant contribution to loop behavior. These components cause a second order LC roll-off at the output, with the attendant 180° phase shift. This roll-off is what filters the PWM waveform, resulting in the desired DC output voltage, but the phase shift complicates the loop compensation if the gain is still higher than unity at the pole frequency. Eventually (usually well above the LC pole frequency), the reactance of the output capacitor will approach its ESR, and the roll-off due to the capacitor will stop, leaving 6dB/octave and 90° of phase shift (Figure 7).

So far, the AC response of the loop is pretty well out of the user's control. The modulator is a fundamental piece of the LTC1704 design, and the external L and C are usually chosen based on the regulation and load current requirements without considering the AC loop response. The feedback amplifier, on the other hand, gives us a handle with which to adjust the AC response. The goal is to have 180° phase shift at DC (so the loop regulates) and something less than 360° phase shift at the point that the loop gain falls to 0dB. The simplest strategy is to set up the feedback amplifier as an inverting integrator, with the 0dB frequency lower than the LC pole (Figure 8). This "Type 1" configuration is stable but transient response will be less than exceptional if the LC pole is at a low frequency.

Figure 9 shows an improved "Type 2" circuit that uses an additional pole-zero pair to temporarily remove 90° of phase shift. This allows the loop to remain stable with 90° more phase shift in the LC section, provided the loop reaches 0dB gain near the center of the phase "bump." Type 2 loops work well in systems where the ESR zero in the LC roll-off happens close to the LC pole, limiting the total phase shift due to the LC. The additional phase compensation in the feedback amplifier allows the 0dB point to be at or above the LC pole frequency, improving loop bandwidth substantially over a simple Type 1 loop. It has limited ability to compensate for LC combinations where low capacitor ESR keeps the phase shift near 180° for an extended frequency range. LTC1704 circuits using conventional switching grade electrolytic output capacitors can often get acceptable phase margin with Type 2 compensation.

"Type 3" loops (Figure 10), use two poles and two zeros to obtain a 180° phase boost in the middle of the frequency band. A properly designed Type 3 circuit can maintain acceptable loop stability even when low output capacitor ESR causes the LC section to approach 180° phase shift well above the initial LC roll-off. As with a Type 2 circuit, the loop should cross through 0dB in the middle of the phase bump to maximize phase margin. Many LTC1704 circuits use low ESR tantalum or OS-CON output capacitors need Type 3 compensation to obtain acceptable phase margin with a high bandwidth feedback loop.

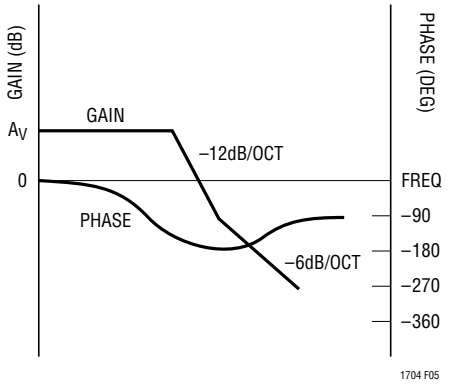

Figure 7. Transfer Function of Buck Modulator

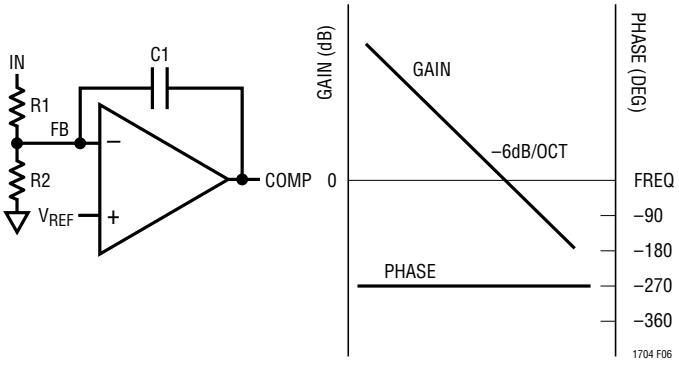

Figure 8. Type 1 Schematic and Transfer Function

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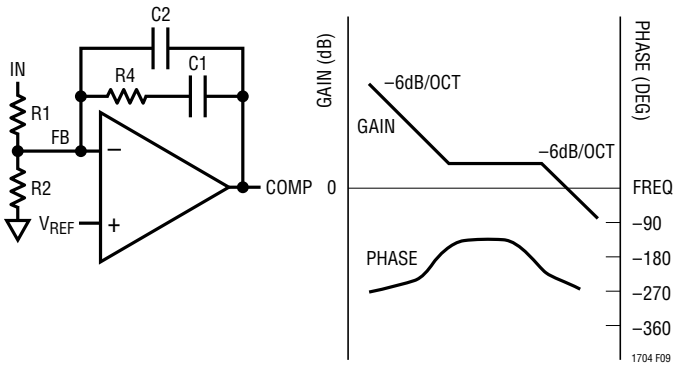

Figure 9. Type 2 Schematic and Transfer Function

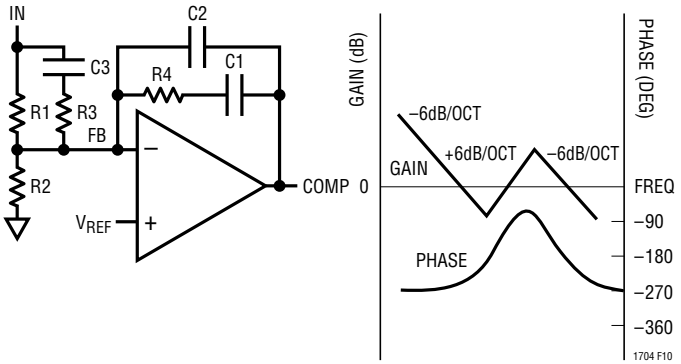

Figure 10. Type 3 Schematic and Transfer Function

Feedback Component Selection

Selecting the R and C values for a typical Type 2 or Type 3 loop is a nontrivial task. The applications shown in this data sheet show typical values, optimized for the power components shown. They should give acceptable performance with similar power components, but can be way off if even one major power component is changed significantly. Applications that require optimized transient response will need to recalculate the compensation values specifically for the circuit in question. The underlying mathematics are complex, but the component values can be calculated in a straightforward manner if we know the gain and phase of the modulator at the crossover frequency.

Modulator gain and phase can be measured directly from a breadboard, or can be simulated if the appropriate parasitic values are known. Measurement will give more accurate results, but simulation can often get close enough to give a working system. To measure the modulator gain and phase directly, wire up a breadboard with an LTC1704 and the actual MOSFETs, inductor, and input and output capacitors that the final design will use. This breadboard should use appropriate construction techniques for high speed analog circuitry: bypass capacitors located close to the LTC1704, no long wires connecting components, appropriately sized ground returns, etc. Wire the feedback amplifier as a simple Type 1 loop, with a 10k resistor from V_{OUTSW} to FB and a 0.1µF feedback capacitor from COMP to FB. Choose the bias resistor (R2) as required to set the desired output voltage. Disconnect R2 from ground and connect it to a signal generator or to the source output of a network analyzer (Figure 11) to inject a test signal into the loop. Measure the gain and phase from the COMP pin to the output node at the positive terminal of the output capacitor. Make sure the analyzer's input is AC coupled so that the DC voltages present at both the COMP and V_{OUTSW} nodes don't corrupt the measurements or damage the analyzer.

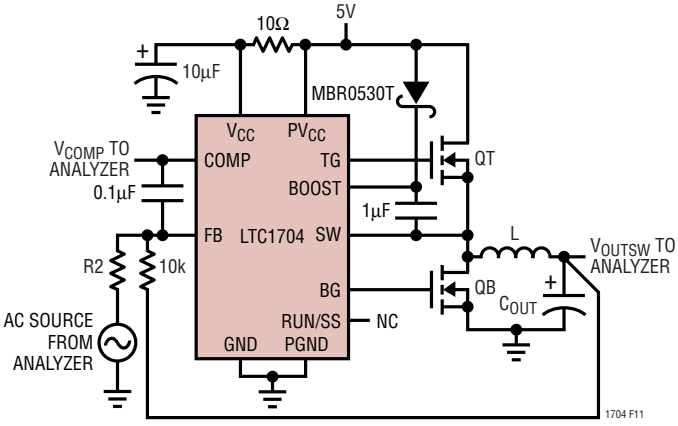

Figure 11. Modulator Gain/Phase Measurement Setup

If breadboard measurement is not practical, a SPICE simulation can be used to generate approximate gain/phase curves. Plug the expected capacitor, inductor and MOSFET values into the following SPICE deck and generate an AC plot of V(V_{OUTSW})/V(COMP) in dB and phase of V(OUTSW) in degrees. Refer to your SPICE manual for details of how to generate this plot.

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```
*1704 modulator gain/phase
*2001 Linear Technology
*this file written to run with PSpice 9.0
*may require modifications for other SPICE
simulators

  *MOSFETs
  rfet mod sw 0.02        ;MOSFET rdson

  *inductor
  lext sw out1 1u         ;inductor value
  rl out1 outsw 0.005     ;inductor series R

  *output cap
  cout outsw out2 1000u   ;capacitor value
  resr out2 0 0.01        ;capacitor ESR

  *1704 internals
  emod mod 0 comp 0 5     ;3.3 for 3.3V supply
  vstim comp 0 0 ac 1     ;ac stimulus
  .ac dec 100 1k 1meg
  .probe
  .end
```

With the gain/phase plot in hand, a loop crossover frequency can be chosen. Usually the curves look something like Figure 7. Choose the crossover frequency in the rising or flat parts of the phase curve, beyond the external LC poles. Frequencies between 10kHz and 50kHz usually work well. Note the gain (GAIN, in dB) and phase (PHASE, in degrees) at this point. The desired feedback amplifier gain will be –GAIN to make the loop gain at 0dB at this frequency. Now calculate the needed phase boost, assuming 60° as a target phase margin:

BOOST = –(PHASE + 30°)

If the required BOOST is less than 60°, a Type 2 loop can be used successfully, saving two external components. BOOST values greater than 60° usually require Type 3 loops for satisfactory performance.

Finally, choose a convenient resistor value for R1 (10k is usually a good value). Now calculate the remaining values:

(K is a constant used in the calculations)

f = chosen crossover frequency

G = $10^{(GAIN/20)}$ (this converts GAIN in dB to G in absolute gain)

TYPE 2 Loop:

$$K = Tan\left(\frac{BOOST}{2} + 45°\right)$$

$$C2 = \frac{1}{2\pi fGKR1}$$

$$C1 = C2\left(K^2 - 1\right)$$

$$R4 = \frac{K}{2\pi fC1}$$

$$R2 = \frac{V_{REF}(R1)}{V_{OUTSW} - V_{REF}}$$

TYPE 3 Loop:

$$K = Tan^2\left(\frac{BOOST}{4} + 45°\right)$$

$$C2 = \frac{1}{2\pi fGR1}$$

$$C1 = C2(K - 1)$$

$$R4 = \frac{\sqrt{K}}{2\pi fC1}$$

$$R3 = \frac{R1}{K - 1}$$

$$C3 = \frac{1}{2\pi f\sqrt{K}R3}$$

$$R2 = \frac{V_{REF}(R1)}{V_{OUTSW} - V_{REF}}$$

SWITCHING SUPPLY CURRENT LIMIT PROGRAMMING

Programming the current limit on the LTC1704 switcher supply is straightforward. The I_{MAX} pin sets the current limit by setting the maximum allowable voltage drop across QB (the bottom MOSFET) before the current limit circuit engages. The voltage across QB is set by its on-resistance and the current flowing in the inductor, which

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is the same as the output current. The LTC1704 current limit circuit inverts the voltage at I_{MAX} before comparing it with the negative voltage across QB, allowing the current limit to be set with a positive voltage.

To set the current limit, calculate the expected voltage drop across QB at the maximum desired current:

$$V_{PROG} = (I_{LIMIT})(R_{DS(ON)})$$

I_{LIMIT} should be chosen to be quite a bit higher than the expected operating current, to allow for MOSFET $R_{DS(ON)}$ changes with temperature. Setting I_{LIMIT} to 150% of the maximum normal operating current is usually safe and will adequately protect the power components if they are chosen properly. Note that the ringing on the switch node can cause error for the current limit threshold (illustrated in Figure 6). This factor will change depending on the layout and the components used. V_{PROG} is then programmed at the I_{MAX} pin using the internal 10µA pull-up and an external resistor:

$$R_{IMAX} = V_{PROG}/10\mu A$$

The resulting value of R_{IMAX} should be checked in an actual circuit to ensure that the current circuit kicks in as expected. MOSFET $R_{DS(ON)}$ specs are like horsepower ratings in automobiles, and should be taken with a grain of salt. Circuits that use very low values for R_{IMAX} (<10k) should be checked carefully, since small changes in R_{IMAX} can cause large I_{LIMIT} changes when the switch node ringing makes up a large percentage of the total V_{PROG} value. If V_{PROG} is set too low, the LTC1704 may fail to start up.

Accuracy Trade-Offs

The V_{DS} sensing scheme used in the LTC1704 is not particularly accurate, primarily due to uncertainty in the $R_{DS(ON)}$ from MOSFET to MOSFET. A second error term arises from the ringing present at the SW pin, which causes the V_{DS} to look larger than $(I_{LOAD})(R_{DS(ON)})$ at the beginning of QB's on-time. Another important error is due to poor PCB layout. Care should be taken to ensure that proper kelvin sensing of the SW pin is provided. These inaccuracies do not prevent the LTC1704 current limit circuit from protecting itself and the load from damaging overcurrent conditions, but they do prevent the user from setting the current limit to a tight tolerance if more than one copy of the circuit is being built. The 50% factor in the current setting equation above reflects the margin necessary to ensure that the circuit will stay out of current limit at the maximum normal load, even with a hot MOSFET that is running quite a bit higher than its $R_{DS(ON)}$ spec.

REGULATION OVER COMPONENT TOLERANCE/TEMPERATURE

DC Regulation Accuracy

The LTC1704's switcher controller initial DC output accuracy depends mainly on internal reference accuracy and internal op amp offset. Two LTC1704 specs come into play: feedback voltage and feedback voltage line regulation. The feedback voltage spec is 800mV ±12mV over the full temperature range and is specified at the FB pin, which encompasses both reference accuracy and any op amp offset. This accounts for 1.5% error at the output with a 5V input supply. The feedback voltage line regulation spec adds an additional 0.1%/V term that accounts for change in reference output with change in input supply voltage. With a 5V supply, the errors contributed by the LTC1704 itself add up to no more than 1.5% DC error at the output.

The output voltage setting resistors (see R1 and R2 in the Typical Applications) are the other major contributor to DC error. At a typical 1.xV output voltage, the resistors are of roughly the same value, which tends to halve their error terms, improving accuracy. Still, using 1% resistors for R1 and R2 will add 1% to the total output error budget. Using 0.1% resistors in just those two positions can nearly halve the DC output error for very little additional cost.

Load Regulation

Load regulation is affected by feedback voltage, feedback amplifier gain and external ground drops in the feedback path. Feedback voltage is covered above and is within 1.5% over temperature. A full range load step might require a 10% duty cycle change to keep the output constant, requiring the COMP pin to move about 100mV. With amplifier gain at 85dB, this adds up to only a 10µV shift at FB, negligible compared to the reference accuracy terms.

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External ground drops aren't so negligible. The LTC1704 can sense the positive end of the output voltage by attaching the feedback resistor directly at the load, but it cannot do the same with the ground lead. Just 0.001Ω of resistance in the ground lead at 10A load will cause a 10mV error in the output voltage—as much as all the other DC errors put together. Proper layout becomes essential to achieving optimum load regulation from the LTC1704. A properly laid out LTC1704 circuit should move less than a millivolt at the output from zero to full load.

Transient Response

Transient response is the other half of the regulation equation. The LTC1704 can keep the DC output voltage constant to within 1% when averaged over hundreds of cycles. Over just a few cycles, however, the external components conspire to limit the speed that the output can move. Consider a typical 5V to 1.5V circuit, subjected to a 1A to 5A load transient. Initially, the loop is in regulation and the DC current in the output capacitor is zero. Suddenly, an extra 4A start flowing out of the output capacitor while the inductor is still supplying only 1A. This sudden change will generate a (4A)(R_{ESR}) voltage step at the output; with a typical 0.015Ω output capacitor ESR, this is a 60mV step at the output, or 4% (for a 1.5V output voltage.)

Very quickly, the feedback loop will realize that something has changed and will move at the bandwidth allowed by the external compensation network towards a new duty cycle. If the bandwidth is set to 50kHz, the COMP pin will get to 60% of the way to 90% duty cycle in 3µs. Now the inductor is seeing 3.5V across itself for a large portion of the cycle, and its current will increase from 1A at a rate set by di/dt = V/L. If the inductor value is 0.5µH, the di/dt will be 3.5V/0.5µH or 7A/µs. Sometime in the next few microseconds after the switch cycle begins, the inductor current will have risen to the 5A level of the load current and the output voltage will stop dropping. At this point, the inductor current will rise somewhat above the level of the output current to replenish the charge lost from the output capacitor during the load transient. During the next couple of cycles, the MIN comparator may trip on and off, preventing the output from falling below its –5% threshold until the time constant of the compensation loop runs out and the main feedback amplifier regains control. With a properly compensated loop, the entire recovery time will be inside of 10µs.

Most loads care only about the maximum deviation from ideal, which occurs somewhere in the first two cycles after the load step hits. During this time, the output capacitor does all the work until the inductor and control loop regain control. The initial drop (or rise if the load steps down) is entirely controlled by the ESR of the capacitor and amounts to most of the total voltage drop. To minimize this drop, reduce the ESR as much as possible by choosing low ESR capacitors and/or paralleling multiple capacitors at the output. The capacitance value accounts for the rest of the voltage drop until the inductor current rises. With most output capacitors, several devices paralleled to get the ESR down will have so much capacitance that this drop term is negligible. Ceramic capacitors are an exception; a small ceramic capacitor can have suitably low ESR with relatively small values of capacitance, making this second drop term significant.

Optimizing Loop Compensation

Loop compensation has a fundamental impact on transient recovery time, the time it takes the LTC1704 to recover after the output voltage has dropped due to output capacitor ESR. Optimizing loop compensation entails maintaining the highest possible loop bandwidth while ensuring loop stability. The Feedback Component Selection section describes in detail the techniques used to design an optimized Type 3 feedback loop, appropriate for most LTC1704 systems.

Measurement Techniques

Measuring transient response presents a challenge in two respects: obtaining an accurate measurement and generating a suitable transient to use to test the circuit. Output measurements should be taken with a scope probe directly across the output capacitor. Proper high frequency probing techniques should be used. In particular, don't use the 6" ground lead that comes with the probe! Use an adapter that fits on the tip of the probe and has a short ground clip to ensure that inductance in the ground path

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doesn't cause a bigger spike than the transient signal being measured. Conveniently, the typical probe tip ground clip is spaced just right to span the leads of a typical output capacitor. Make sure the bandwidth limit on the scope is turned off, since a significant portion of the transient energy occurs above the 20MHz cutoff.

Now that we know how to measure the signal, we need to have something to measure. The ideal situation is to use the actual load for the test, and switch it on and off while watching the output. If this isn't convenient, a current step generator is needed. This generator needs to be able to turn on and off in nanoseconds to simulate a typical switching logic load, so stray inductance and long clip leads between the LTC1704 and the transient generator must be minimized.

Figure 12 shows an example of a simple transient generator. Be sure to use a noninductive resistor as the load element—many power resistors use an inductive spiral pattern and are not suitable for use here. A simple solution is to take ten 1/4W film resistors and wire them in parallel to get the desired value. This gives a noninductive resistive load which can dissipate 2.5W continuously or 50W if pulsed with a 5% duty cycle, enough for most LTC1704 circuits. Solder the MOSFET and the resistor(s) as close to the output of the LTC1704 circuit as possible and set up the signal generator to pulse at a 100Hz rate with a 5% duty cycle. This pulses the LTC1704 with 500µs transients 10ms apart, adequate for viewing the entire transient recovery time for both positive and negative transitions while keeping the load resistor cool.

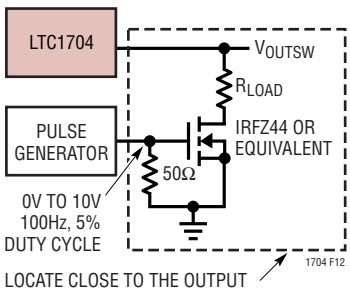

Figure 12. Transient Load Generator

LINEAR REGULATOR SUPPLY

Linear Regulator Output Voltage

The linear regulator senses the output voltage at V_{OUTREG} with an internal amplifier (see Figure 13). The amplifier negative input is connected internally to an 800mV reference, while the positive input is connected to the REGFB pin. The amplifier output drives a P-channel transistor MREG, which is in turn connected to the external NPN pass transistor. The linear regulator output voltage can be obtained using the following equation:

$$V_{OUTREG} = 0.8V\left(1+\frac{R5}{R6}\right)$$

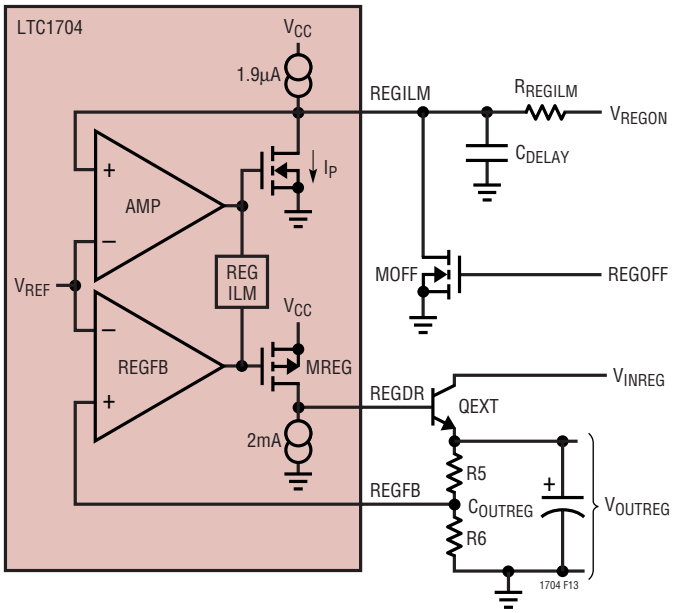

Figure 13. Linear Regulator

Linear Regulator Supplies Requirement

The linear regulator operates with two supplies: V_{CC} for the LTC1704 and V_{INREG} for the external NPN transistor QEXT. Both supplies must be higher than the minimum value determined by the linear regulator output voltage, V_{OUTREG}. For a desired V_{OUTREG}, use the following formula to calculate the minimum required V_{CC}:

$$\text{Minimum } V_{CC} = V_{OUTREG} + V_{BE(QEXT)} + V_{DROPOUT}$$

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where $V_{BE(QEXT)}$ is base emitter voltage of QEXT and $V_{DROPOUT}$ is the LTC1704 linear regulator controller dropout voltage.

The MJD44H11 from ON Semiconductor has a V_{BE} of around 0.9V at I_C = 2A, 25°C and the LTC1704's $V_{DROPOUT}$ is 1.1V maximum with 30mA of drive current.

If the computed minimum V_{CC} is less than the LTC1704 requirement of 3.15V then 3.15V should be used.

The minimum V_{INREG} is determined by the V_{CE} saturation voltage of QEXT when it is driven with a base current equal to the maximum REGDR pin drive current. The D44H11 has a saturation voltage of around 0.2V at I_C = 2A, 25°C.

A typical 1.5V V_{OUTREG}, 2A application will need a minimum V_{CC} of 1.5V + 0.9V + 1.1V = 3.5V and a minimum V_{INREG} of 1.5V + 0.2V = 1.7V to operate.

If a V_{OUTREG} of 0.8V is needed, the minimum V_{CC} should be 3.15V and the minimum V_{INREG} is 0.8V + 0.2V = 1V.

External NPN Pass Transistor

The external NPN Pass transistor for the LTC1704 linear regulator supply should be selected based on the following criteria:

1. Maximum output current
2. DC current gain h_{FE}
3. Total allowable power dissipation
4. Gain bandwidth product f_T

The NPN transistor must be able to supply the maximum operating current for the linear regulator supply. At the same time, the DC current gain h_{FE} must be large enough such that the pass transistor can supply the maximum load current with 30mA of base current. The transistor must not be subjected to power dissipation higher than the rated value, both during normal operation and overload conditions. Heat sink can be used to increase the alloweable power dissipation rating. The gain bandwidth product f_T of the transistor determines how fast the linear regulator can follow an output load change without losing voltage regulation.

The MJD44H11 from ON Semiconductor and SGS-Thomson can be used in the LTC1704 linear regulator supply with current ratings up to 2A. The MJD44H11 from ON Semiconductor can supply 8A of output current and the minimum DC Current Gain h_{FE} is 60 at IC = 2A. The power dissipation rating is 1.75W without heat sink and the gain bandwidth product f_T of the MJD44H11 is typically 50MHz.

Linear Regulator Supply Current Limit Programming

The LTC1704 linear regulator uses an external resistor R_{REGILM} to program the NPN pass transistor base current. This indirectly programs the linear regulator current limit threshold. Figure 13 shows the setup. One end of the resistor R_{REGILM} is connected to an external voltage source V_{REGON} or, alternatively, it can be connected to the V_{CC} pin. The other end of the resistor is connected to the REGILM pin. REGILM is internally regulated to 0.8V. The voltage difference across this resistor generates the REGILM pin input current. This current, together with the internal 1.9µA current source, programs the REGDR maximum output current. The actual linear regulator current limit depends on the pass transistor's widely distributed DC current gain h_{FE}, which makes this current limit scheme not particularly accurate. Nevertheless, this method removes the expensive current sense resistor and with careful design, it is sufficient to protect the external NPN from over damaging.

The following equation shows the relationship between R_{REGILM} and the linear regulator current limit threshold I_{LT}:

$$R_{REGILM} = \frac{(V_{REGON} - 0.8)(2100)}{\left(\frac{I_{LT}}{h_{FE}} - 7.5mA\right)}$$

where V_{REGON} is the pull-up voltage source for R_{REGILM} (see Figure 13).

When there is an overload at the linear regulator output, the current limit circuit fires and the output voltage drops. To protect the NPN from excessive heating, the controller

APPLICATIONS INFORMATION

reduces the available base current to minimize the $I_{LOAD} \bullet V_{CE}$ product across the pass transistor. The amount of current reduction depends on the REGFB pin voltage and the R_{REGILM} resistance (refer to the Typical Performance Characteristics Curves). This current limit foldback scheme limits the NPN power dissipation and prevents it from blowing up. However, in cases when there is a constant current load at the regulator output, this current limit foldback scheme can create a start-up problem. In spite of this, most applications do not have full load requirement during start-up. To fulfill majority applications requirements, the LTC1704 linear regulator allows a small amount of base current when the linear regulator output is shorted or V_{REGFB} = 0V. The actual regulator short-circuit current can be calculated from the following equation:

$$I_{SH} = h_{FE}\left(4.8mA + \frac{V_{REGON} - 0.8}{R_{REGILM}} \bullet 300\right)$$

This short-circuit current should be checked against the load requirement to allow proper start-up.

Linear Regulator Power Down

The linear regulator can be powered down easily. A pull-down device (MOFF as shown in Figure 13) that is capable of overcoming the REGILM pin 1.9µA weak pull-up current can shut down the linear regulator. As shown in Figure 13, if the resistor R_{REGILM} is smaller than 400k, forcing V_{REGON} to ground can overcome the pull-up current and power down the linear regulator. When both the REGILM and RUN/SS pins are forced low, LTC1704 enters shut-down mode and the quiescent current is reduced to 75µA.

Linear Regulator Turn-On Delay

The external capacitor C_{DELAY} from the REGILM pin to ground allows the REGILM pin to ramp up slowly and adds a delay to the turn-on time of the linear regulator. The current through the resistor R_{REGILM}, the internal pull-up current and the external capacitor C_{DELAY} controls the REGILM pin slew rate. To power up the linear regulator, the potential at the REGILM pin should not be below 0.8V.

To add power sequencing to the linear regulator is easy. Once the current limit resistor R_{REGILM} is chosen, the capacitor C_{DELAY} can be added to program the turn on delay using the following equation:

$$t_{DELAY} = \frac{0.8 \bullet C_{DELAY}}{\frac{V_{REGON} - 0.8}{R_{REGILM}} + 1.9\mu A}$$

The actual turn-on delay, which includes the time for the external NPN to charge the output capacitor, will be longer than the calculated value.

The LTC1704 linear regulator turn-on delay circuit is versatile; C_{DELAY} capacitance should be larger than 100pF to allow instantaneous power up to seconds long delay.

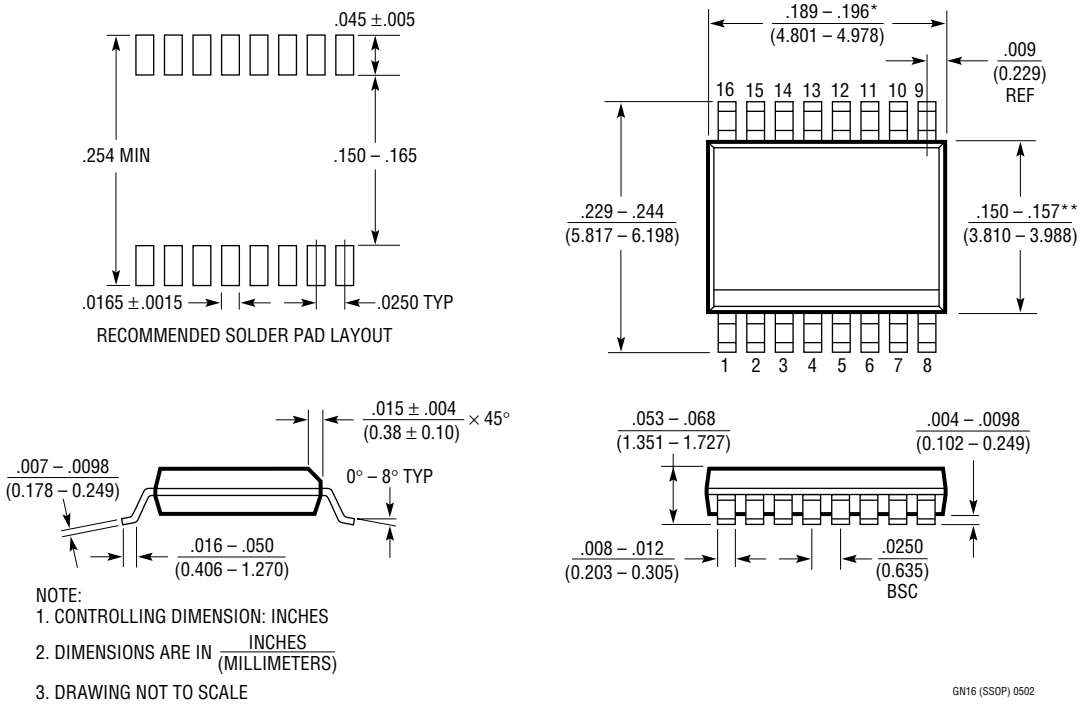
Linear Regulator Output Bypass Capacitor

The linear regulator requires the use of an output capacitor as part of the frequency compensation network. A minimum output capacitor of 10µF with an ESR lower than 100mΩ is recommended to prevent oscillations. Larger values of output capacitance with low ESR should be used to provide improved transient response for large load current changes.

Many different types of capacitors are available and have widely varying characteristics. These capacitors differ in capacitor tolerance (sometimes ranging up to ±100%), equivalent series resistance, equivalent series inductance and capacitance temperature coefficient. Low ESR tantalum capacitors are recommended for this linear regulator.

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

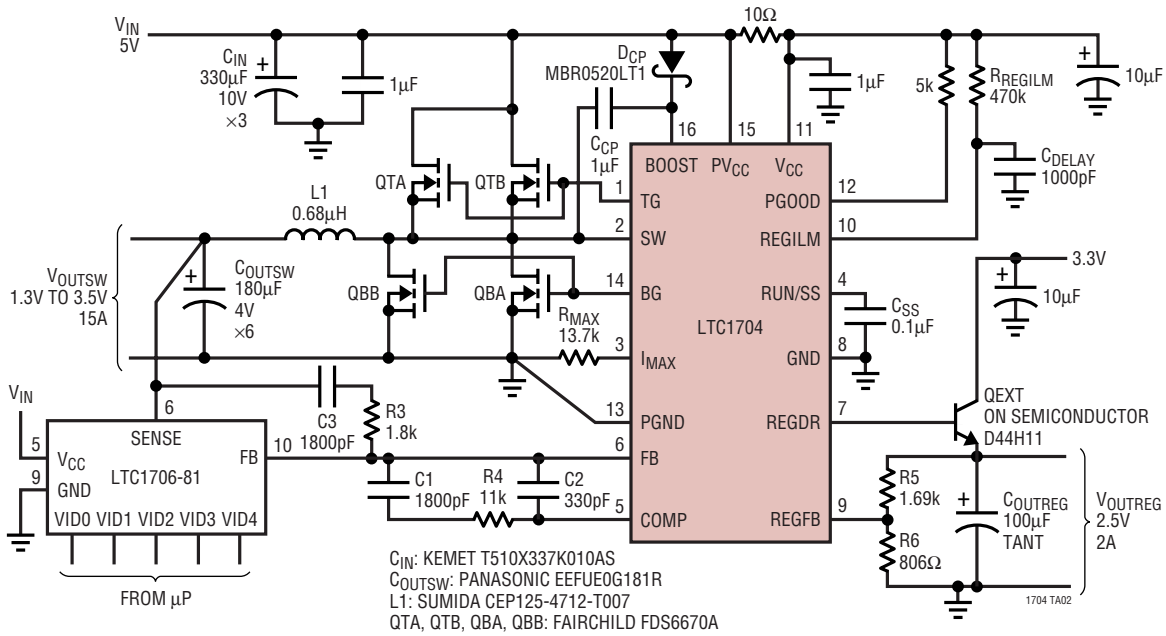
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

TYPICAL APPLICATION

VID Controlled Power Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1530	High Power Synchronous Step-Down Controller	SO-8 with Current Limit, No R_{SENSE}™ Required
LTC1628	Dual High Efficiency 2-Pass Synchronous Step-Down Controller	Constant Frequency, Standby 5V and 3.3V LDOs, $3.5V \le V_{IN} \le 36V$
LTC1699	SMBus VID Voltage Programmers	SMBus Interface, Intel 5-Bit Mobile, Intel Desktop VID Codes VRM8.4 and VRM9.0
LTC1703	Dual 550kHz Synchronous 2-Phase Switching Regulator Controller with VID	VID Control with 25MHz GBW Voltage Mode, $V_{IN} \le 7V$
LTC1705	Dual 550kHz Synchronous Switching Regulator Controller with 5-Bit VID Plus LDO	VID Control with 20MHz GBW Voltage Mode, $V_{IN} \le 6V$
LTC1706-81	5-Bit Desktop VID Programmer	Parallel Interface, 0.8V Reference Intel Desktop VID Codes (VRM8.4)
LTC1706-82	VID Programmer for Intel VRM9.0	Parallel Interface, 0.8V Reference Intel Desktop VID Codes (VRM9.0)
LTC1736	Synchronous Step-Down Controller with 5-Bit VID Control	Output Fault Protection, Power Good Output, 3.5V to 36V Input
LTC1778	No R_{SENSE} Current Mode Synchronous Step-Down Controller	Up to 97% Efficiency, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)(V_{IN})$, I_{OUT} Up to 20A
LTC3701	2-Phase, Low V_{IN}, Dual Step-Down Controller	$2.5V \le V_{IN} \le 9.8V$, 550kHz Operation, Minimum C_{IN}, 16-Lead SSOP Package

No R_{SENSE} is a trademark of Linear Technology Corporation.

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