



New Product

SUD50P10-43
Vishay Siliconix

P-Channel 100-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

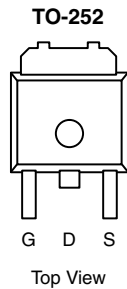
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ)
-100	0.043 at $V_{GS} = -10$ V	-38	105 nC

FEATURES

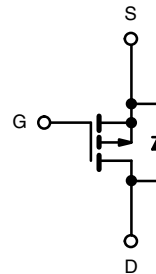
- TrenchFET[®] Power MOSFET



RoHS
COMPLIANT



Drain Connected to Tab



Ordering Information: SUD50P10-43-E3 (Lead (Pb)-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	-100	V	
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current ($T_J = 175$ °C)	$T_C = 25$ °C	I_D	-38 ^a	A	
	$T_C = 70$ °C		-31.8 ^a		
	$T_A = 25$ °C		-9.4 ^{b, c}		
	$T_A = 70$ °C		-7.8 ^{b, c}		
Pulsed Drain Current		I_{DM}	-50		
Continuous Source-Drain Diode Current	$T_C = 25$ °C	I_S	-50 ^a		
	$T_A = 25$ °C		-6.9 ^{b, c}		
Avalanche Current		I_{AS}	-40	mJ	
Single-Pulse Avalanche Energy		E_{AS}	80		
Maximum Power Dissipation	$T_C = 25$ °C	P_D	136	W	
	$T_C = 70$ °C		95		
	$T_A = 25$ °C		8.3 ^{b, c}		
	$T_A = 70$ °C		5.8 ^{b, c}		
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-50 to 175		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	$t \leq 10$ sec	R_{thJA}	15	18	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	0.85	1.1	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 Board.
- $t = 10$ sec.
- Maximum under steady state conditions is 40 °C/W.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = -250 μA	-100			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = -250 μA		-105		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			7		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-2	-3	-4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -100 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -100 V, V _{GS} = 0 V, T _J = 55 °C			-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = -10 V	-35			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -9.4 A		0.036	0.043	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -9.4 A		30		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = -50 V, V _{GS} = 0 V, f = 1 MHz		5230		pF
Output Capacitance	C _{oss}			230		
Reverse Transfer Capacitance	C _{rss}			165		
Total Gate Charge	Q _g	V _{DS} = -50 V, V _{GS} = -10 V, I _D = -9.4 A		105	160	nC
Gate-Source Charge	Q _{gs}			21		
Gate-Drain Charge	Q _{gd}			29		
Gate Resistance	R _g	f = 1 MHz		4.1		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -50 V, R _L = 6.4 Ω I _D ≅ -7.8 A, V _{GEN} = -10 V, R _g = 1 Ω		30	50	ns
Rise Time	t _r			115	175	
Turn-Off Delay Time	t _{d(off)}			80	120	
Fall Time	t _f			60	90	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			-50	A
Pulse Diode Forward Current ^a	I _{SM}				-50	
Body Diode Voltage	V _{SD}	I _S = -7.8 A		-0.8	-1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = -7.8 A, di/dt = 100 A/μs, T _J = 25 °C		60	90	ns
Body Diode Reverse Recovery Charge	Q _{rr}			180	270	nC
Reverse Recovery Fall Time	t _a			48		ns
Reverse Recovery Rise Time	t _b			12		

Notes

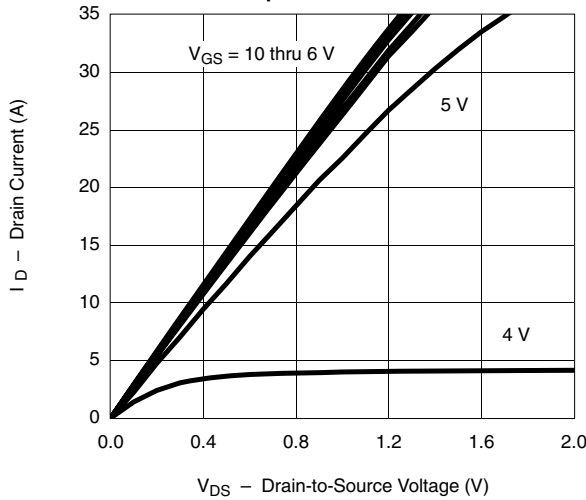
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

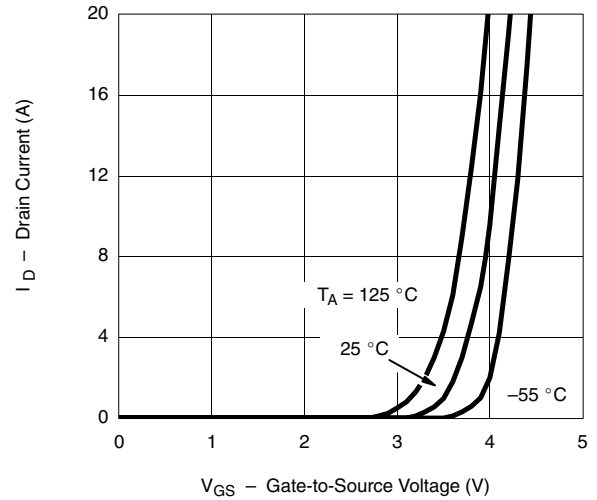


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

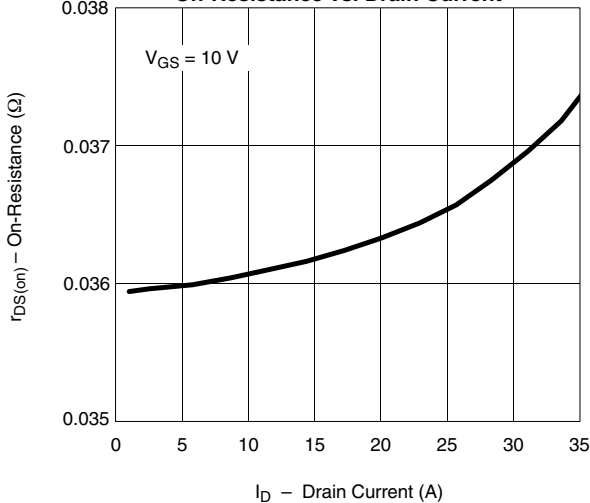
Output Characteristics



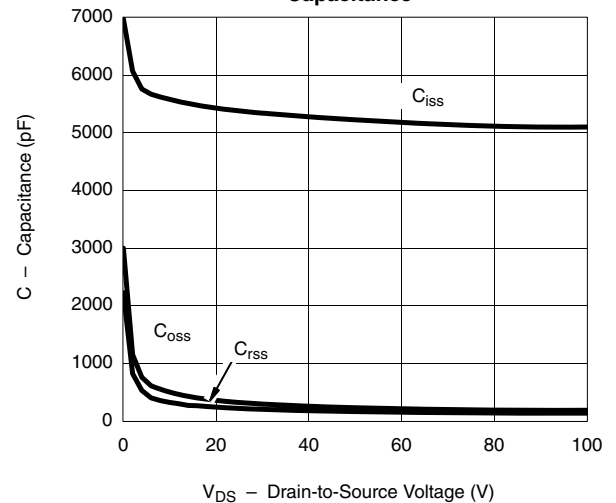
Transfer Characteristics



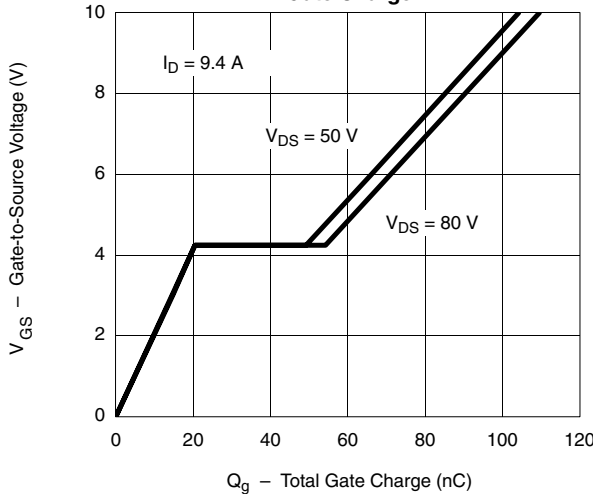
On-Resistance vs. Drain Current



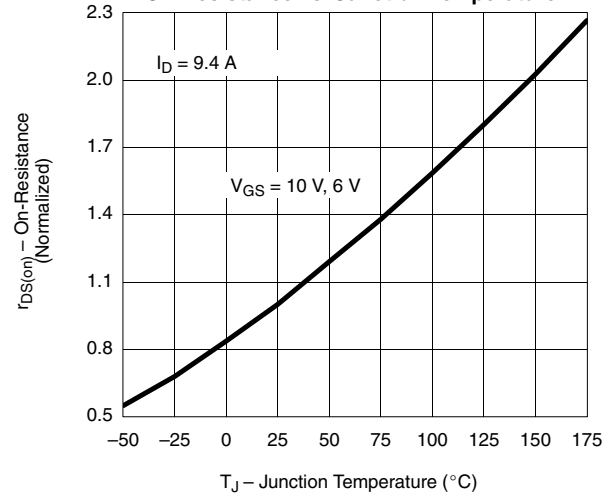
Capacitance



Gate Charge

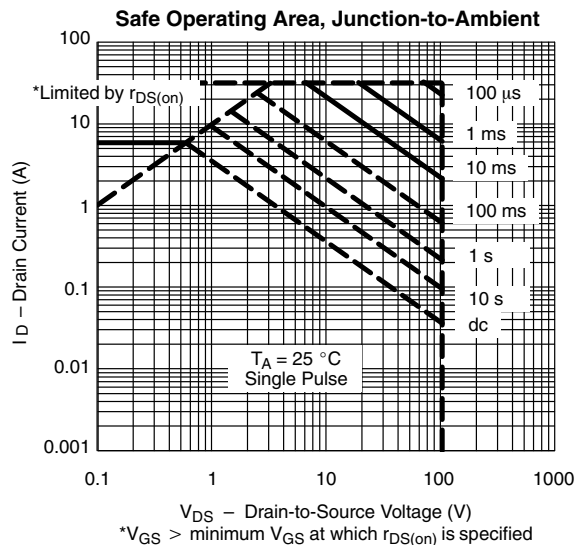
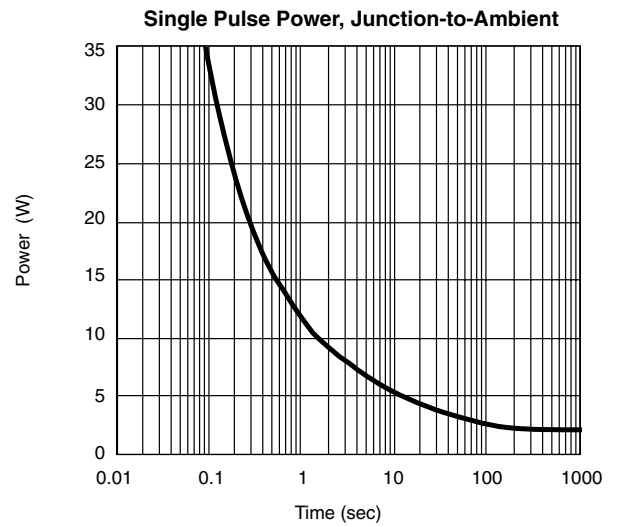
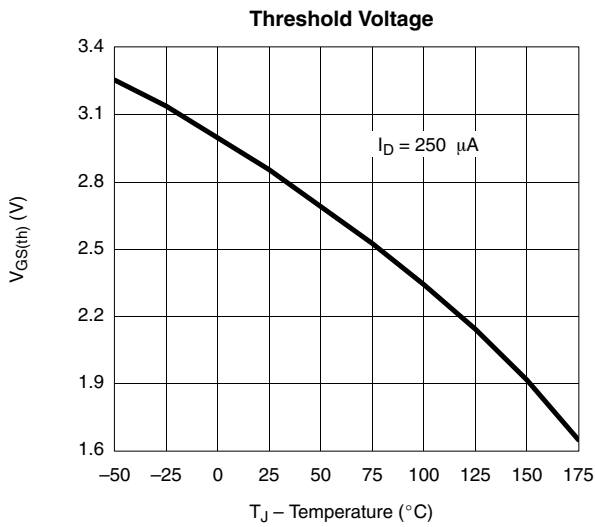
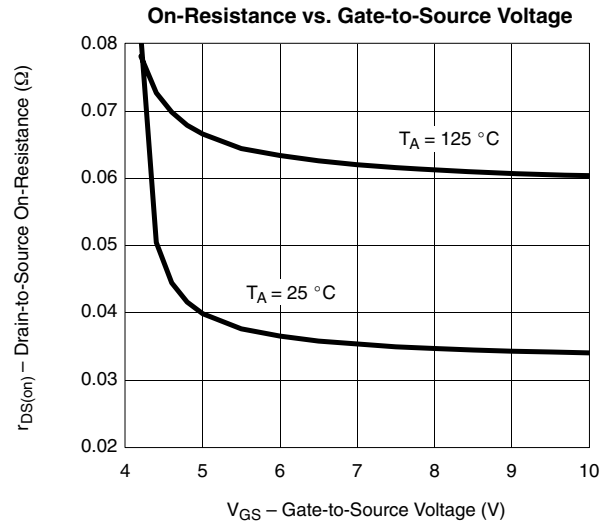
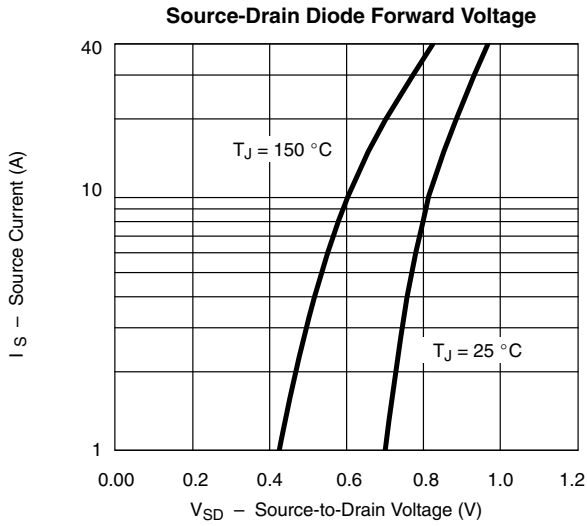


On-Resistance vs. Junction Temperature





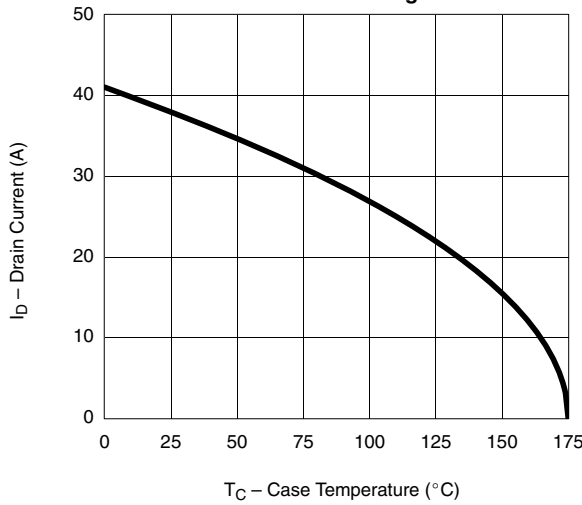
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



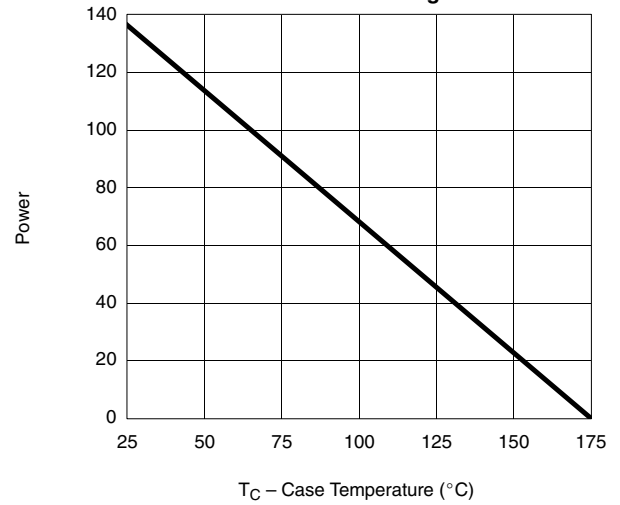


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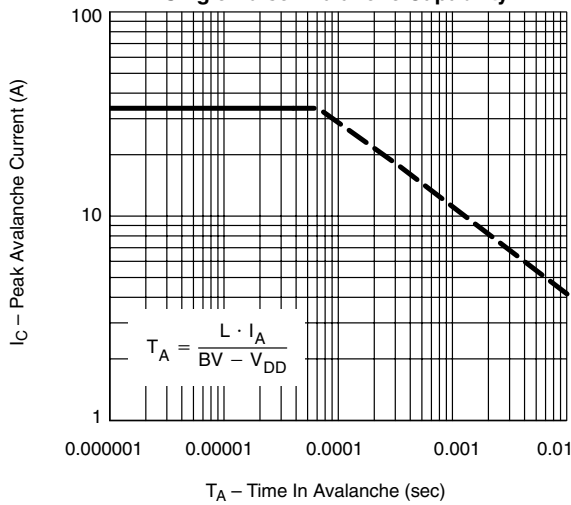
Current De-Rating*



Power De-Rating



Single Pulse Avalanche Capability

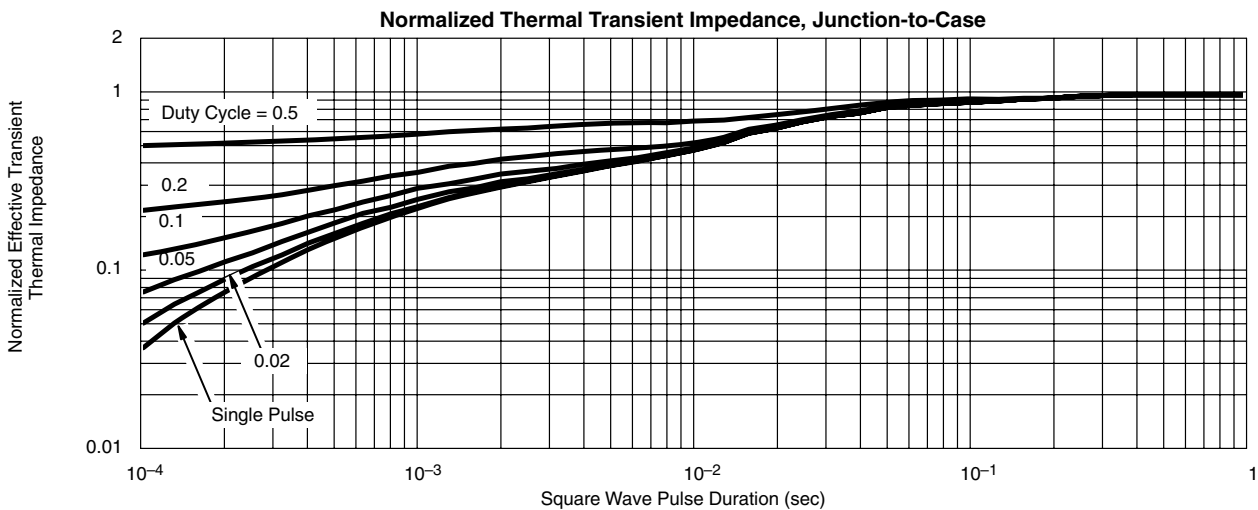
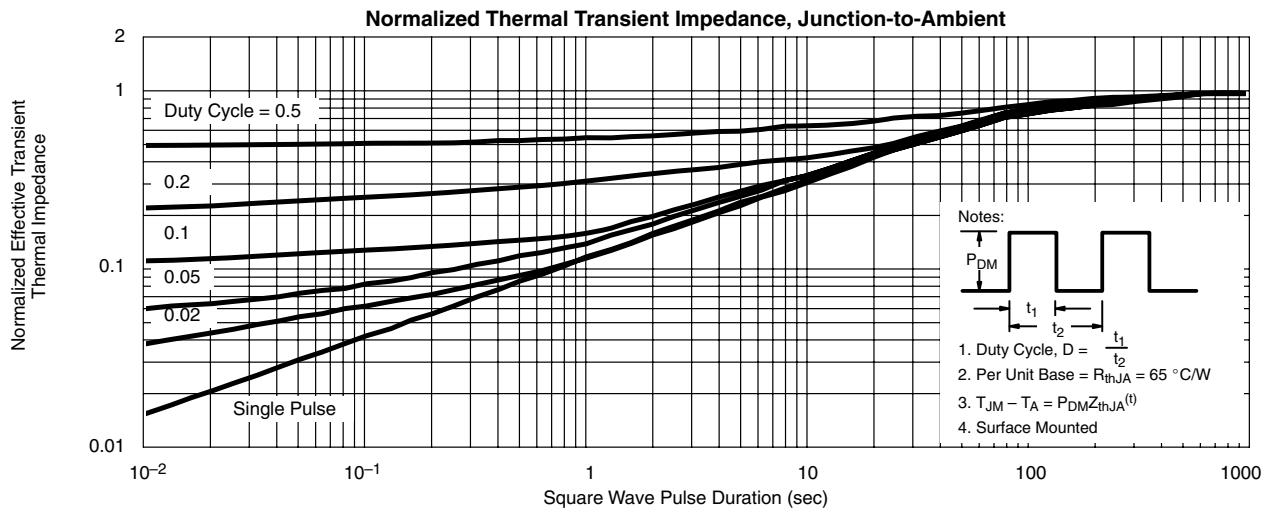


$$T_A = \frac{L \cdot I_A}{BV - V_{DD}}$$

*The power dissipation P_D is based on $T_{J(max)} = 175\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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