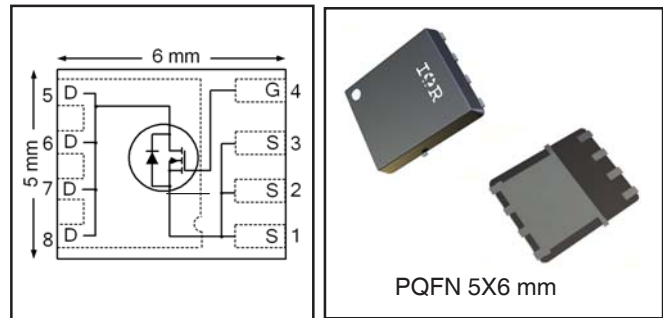


HEXFET® Power MOSFET

$V_{DS}$	<b>20</b>	<b>V</b>
$V_{GS\ max}$	<b>± 12</b>	<b>V</b>
$R_{DS(on)\ max}$ (@ $V_{GS} = 4.5V$ )	<b>3.0</b>	<b>mΩ</b>
(@ $V_{GS} = 2.5V$ )	<b>4.0</b>	
$Q_g\ typ$	<b>44</b>	<b>nC</b>
$I_D$ (@ $T_{c(Bottom)} = 25^\circ C$ )	<b>80</b> ⑦	<b>A</b>



**Applications**

- Battery Protection Switch

**Features and Benefits**

Features
Low Thermal Resistance to PCB (< 2.4°C/W)
100% Rg tested
Low Profile (<1.2mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in  
 ⇒

Benefits
Enable better thermal dissipation
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLH6224TRPBF	PQFN 5mm x 6mm	Tape and Reel	4000	
IRLH6224TR2PBF	PQFN 5mm x 6mm	Tape and Reel	400	EOL notice # 259

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	20	V
$V_{GS}$	Gate-to-Source Voltage	± 12	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	28	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	22	
$I_D @ T_{c(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	105 ⑥ ⑦	
$I_D @ T_{c(Bottom)} = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	67 ⑥	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	80 ⑦	
$I_{DM}$	Pulsed Drain Current ①	400	
$P_D @ T_A = 25^\circ C$	Power Dissipation ②	3.6	W
$P_D @ T_{c(Bottom)} = 25^\circ C$	Power Dissipation ②	52	
	Linear Derating Factor ③	0.029	W/°C
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		

Notes ① through ⑥ are on page 9

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

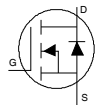
	Parameter	Min.	Typ.	Max.	Units	Conditions		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA		
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	5.0	—	mV/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA		
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	2.3	3.0	mΩ	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 20A ③		
		—	3.2	4.0		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 16A ③		
V <sub>GS(th)</sub>	Gate Threshold Voltage	0.5	0.8	1.1	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50μA		
ΔV <sub>GS(th)</sub>	Gate Threshold Voltage Coefficient	—	-4.2	—	mV/°C			
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	1	μA	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V		
		—	—	150		V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C		
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 12V		
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -12V		
gfs	Forward Transconductance	150	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 20A		
Q <sub>g</sub>	Total Gate Charge	—	86	—	nC	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 20A		
Q <sub>g</sub>	Total Gate Charge	—	44	—	nC	V <sub>DS</sub> = 10V V <sub>GS</sub> = 4.5V I <sub>D</sub> = 20A		
		Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	—			3.8	—
		Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	—			4.7	—
		Q <sub>gd</sub>	Gate-to-Drain Charge	—			8.5	—
		Q <sub>godr</sub>	Gate Charge Overdrive	—			27	—
		Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	—			13	—
Q <sub>oss</sub>	Output Charge	—	30	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V		
R <sub>G</sub>	Gate Resistance	—	2.0	—	Ω			
t <sub>d(on)</sub>	Turn-On Delay Time	—	9.4	—	ns	V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 20A R <sub>G</sub> = 1.8Ω		
t <sub>r</sub>	Rise Time	—	23	—				
t <sub>d(off)</sub>	Turn-Off Delay Time	—	67	—				
t <sub>f</sub>	Fall Time	—	36	—				
C <sub>iss</sub>	Input Capacitance	—	3710	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 10V f = 1.0MHz		
C <sub>oss</sub>	Output Capacitance	—	1050	—				
C <sub>rss</sub>	Reverse Transfer Capacitance	—	770	—				

**Avalanche Characteristics**

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	125	mJ
I <sub>AR</sub>	Avalanche Current ①	—	20	A

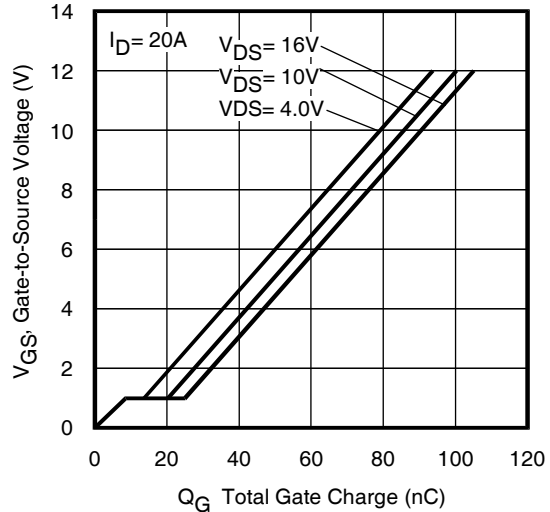
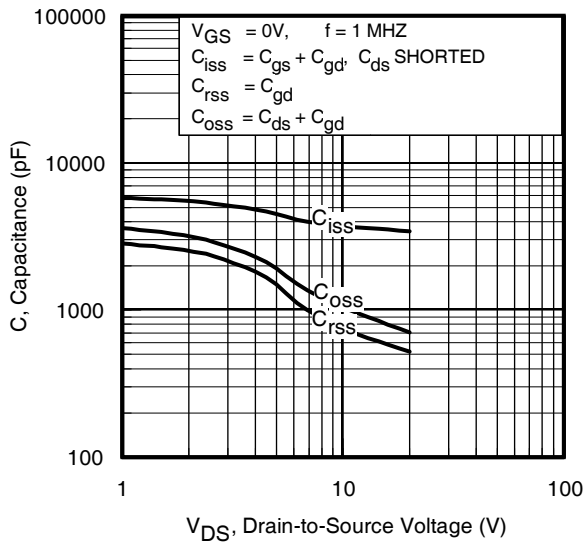
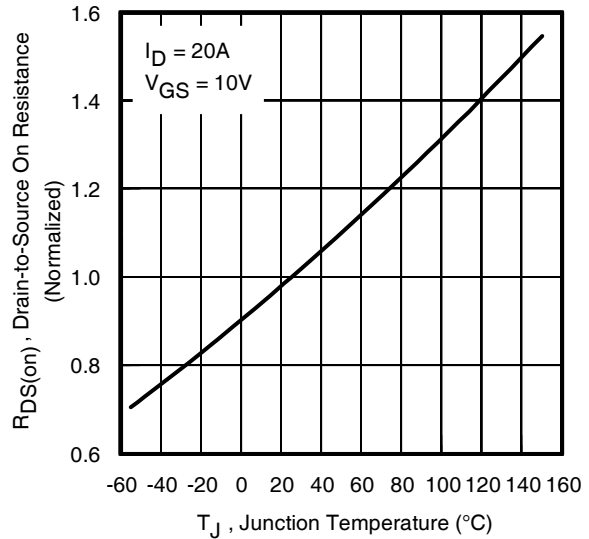
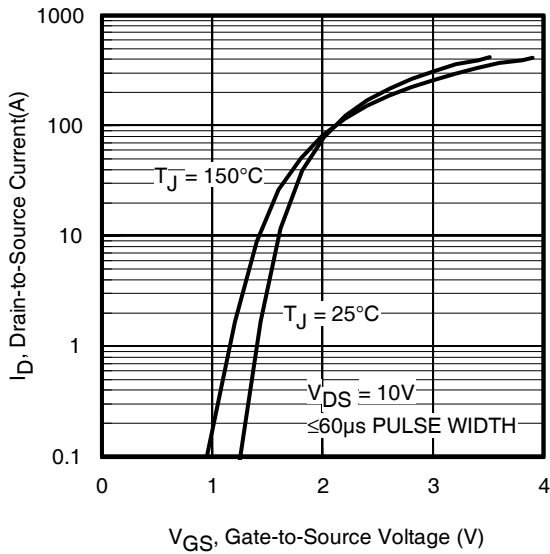
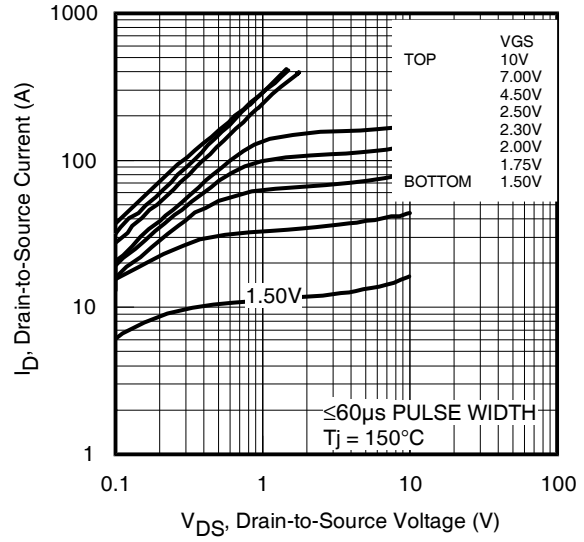
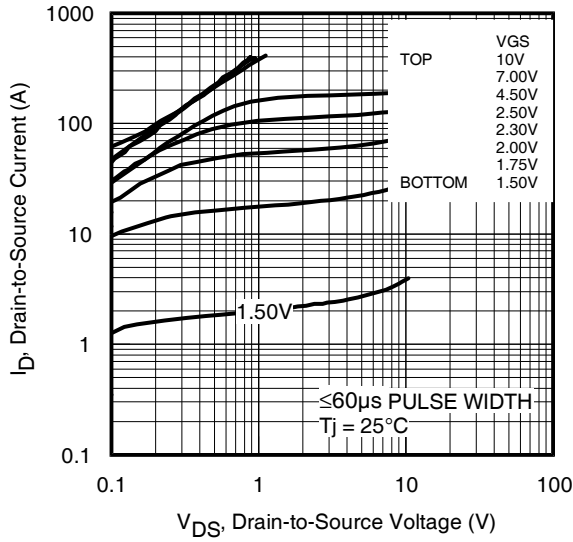
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	67	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	400		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	38	57	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	82	125	nC	di/dt = 300A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Time is dominated by parasitic inductance				



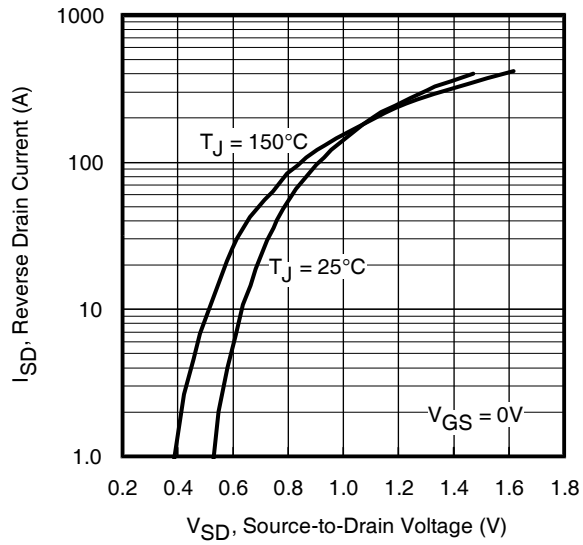
**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub> (Bottom)	Junction-to-Case ④	—	2.4	°C/W
R <sub>θJC</sub> (Top)	Junction-to-Case ④	—	34	
R <sub>θJA</sub>	Junction-to-Ambient ⑤	—	35	
R <sub>θJA</sub> (<10s)	Junction-to-Ambient ⑤	—	22	

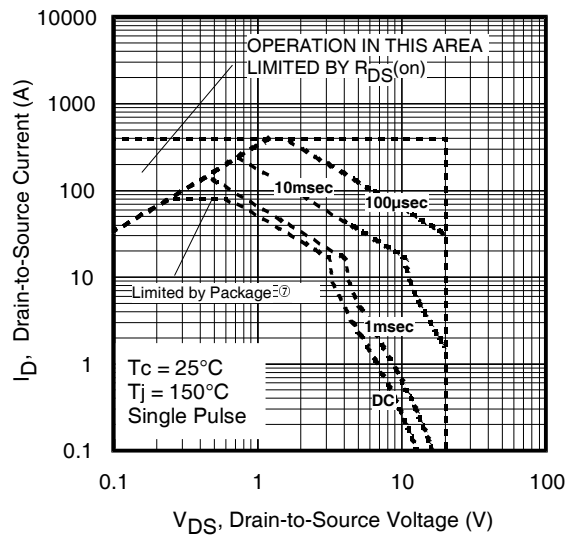


**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

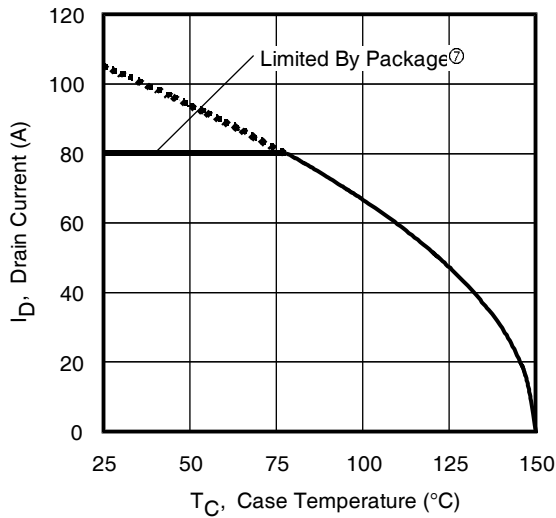
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



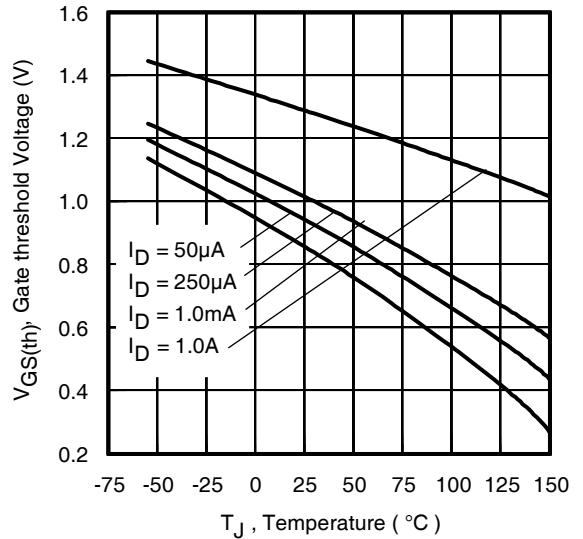
**Fig 7.** Typical Source-Drain Diode Forward Voltage



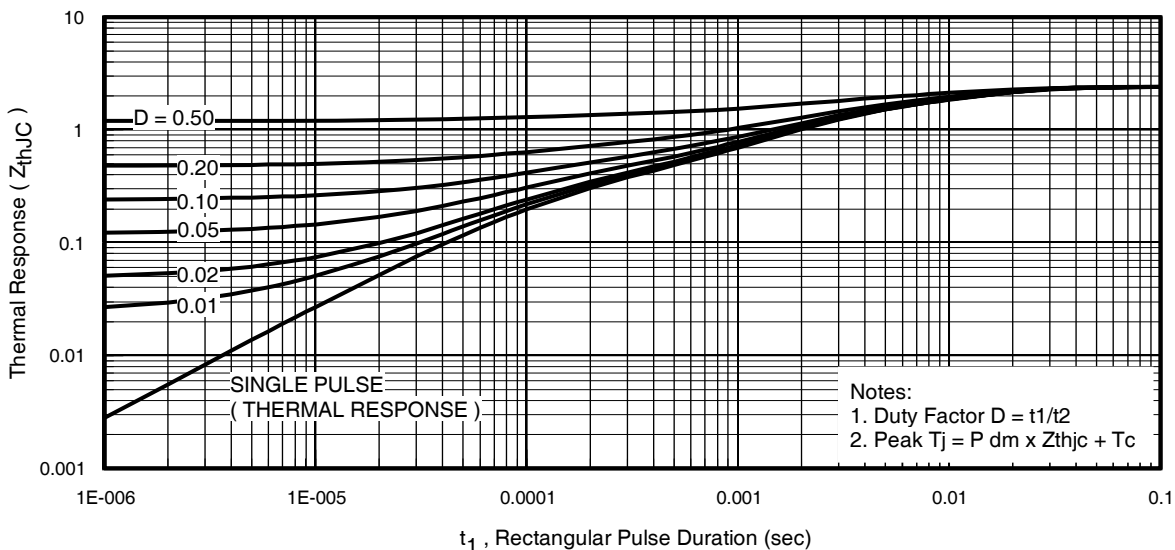
**Fig 8.** Maximum Safe Operating Area



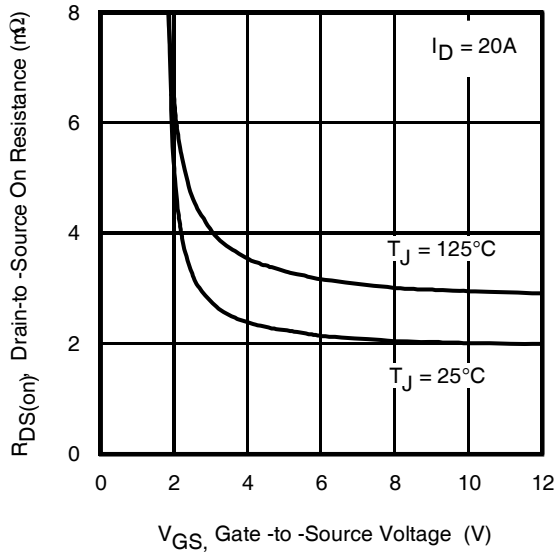
**Fig 9.** Maximum Drain Current vs. Case (Bottom) Temperature



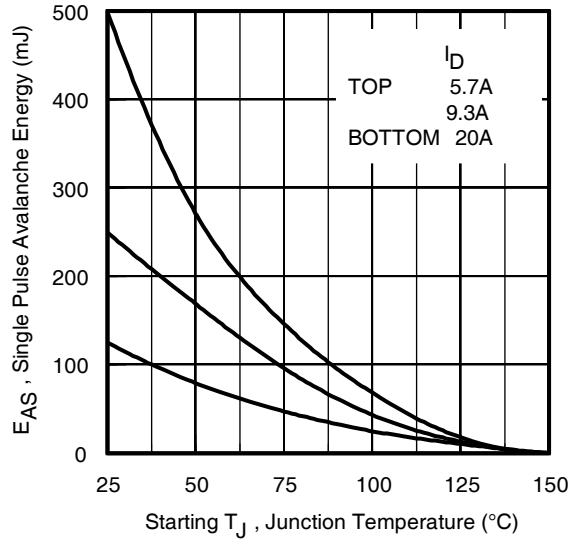
**Fig 10.** Threshold Voltage vs. Temperature



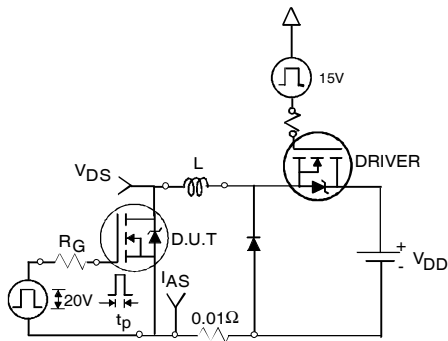
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)



**Fig 12.** On-Resistance vs. Gate Voltage



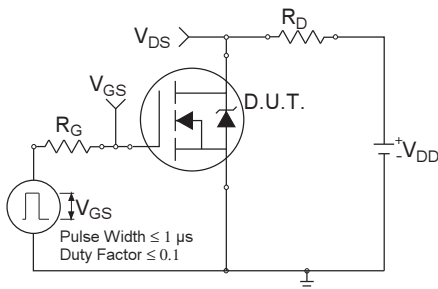
**Fig 13.** Maximum Avalanche Energy vs. Drain Current



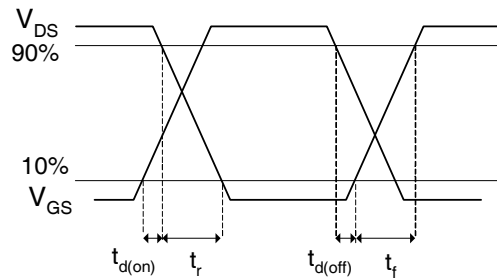
**Fig 14a.** Unclamped Inductive Test Circuit



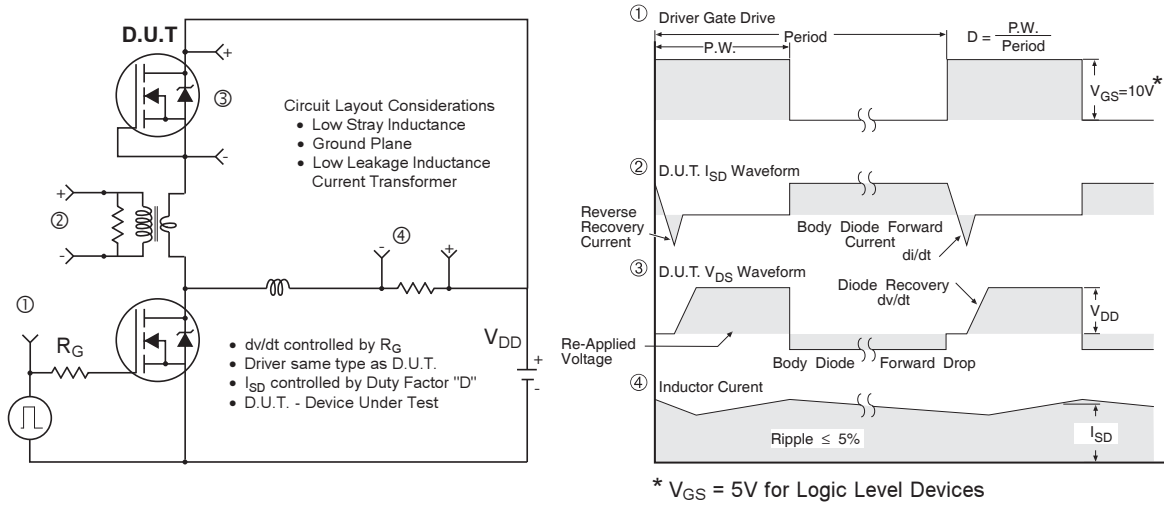
**Fig 14b.** Unclamped Inductive Waveforms



**Fig 15a.** Switching Time Test Circuit



**Fig 15b.** Switching Time Waveforms



**Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**

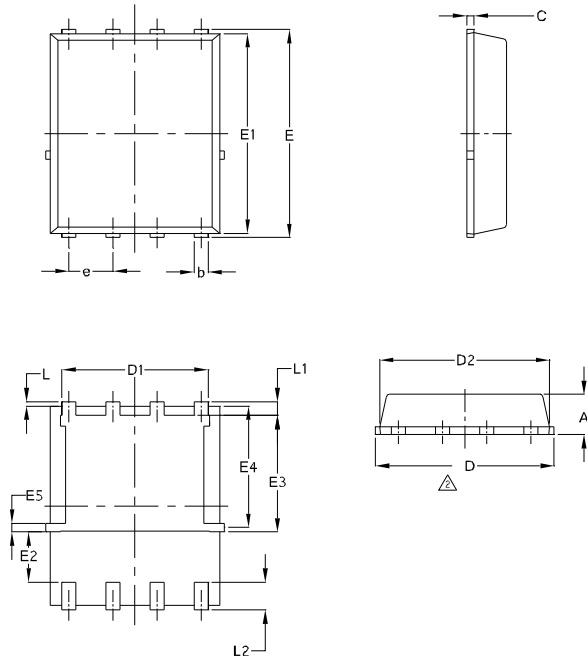


**Fig 17. Gate Charge Test Circuit**



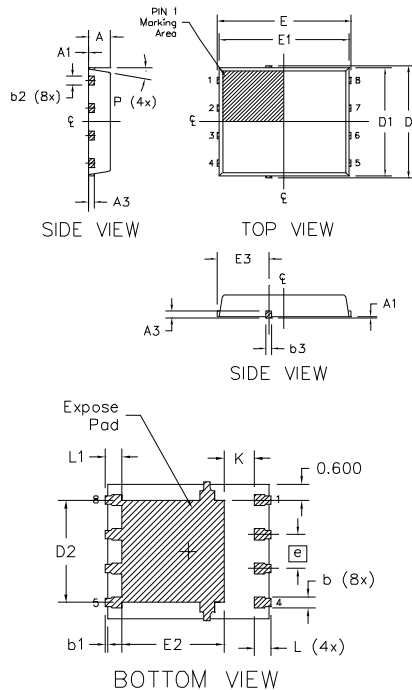
**Fig 18. Gate Charge Waveform**

## PQFN 5x6 Outline "E" Package Details



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.17	0.0354	0.0461
b	0.33	0.48	0.0130	0.0189
C	0.195	0.300	0.0077	0.0118
D	4.80	5.15	0.1890	0.2028
D1	3.91	4.31	0.1539	0.1697
D2	4.80	5.00	0.1890	0.1968
E	5.90	6.15	0.2323	0.2421
E1	5.65	6.00	0.2224	0.2362
E2	1.51	—	0.0594	—
E3	3.32	3.78	0.1307	0.1480
E4	3.42	3.58	0.1346	0.1409
E5	0.18	0.32	0.0071	0.0126
e	1.27	BSC	0.050	BSC
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.66	0.0150	0.0260
L2	0.51	0.86	0.0201	0.0339
I	0	0.18	0	0.0071

## PQFN 5x6 Outline "G" Package Details



DIM SYMBOL	MILLIMETERS		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.950	1.050	0.0374	0.0413
A1	0.000	0.050	0.0000	0.0020
A3	0.254	REF	0.0100	REF
b	0.310	0.510	0.0122	0.0201
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.180	0.450	0.0071	0.0177
D	5.150	BSC	0.2028	BSC
D1	5.000	BSC	0.1969	BSC
D2	3.700	3.900	0.1457	0.1535
E	6.150	BSC	0.2421	BSC
E1	6.000	BSC	0.2362	BSC
E2	3.560	3.760	0.1402	0.1488
E3	2.270	2.470	0.0894	0.0972
e	1.27	REF	0.050	REF
K	0.830	1.400	0.0327	0.0551
L	0.510	0.710	0.0201	0.0280
L1	0.510	0.710	0.0201	0.0280
P	10 deg	12 deg	0 deg	12 deg

**Note:**

- Dimensions and tolerancing confirm to ASME Y14.5M-1994
- Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
- Coplanarity applies to the expose Heat Slug as well as the terminal
- Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136:

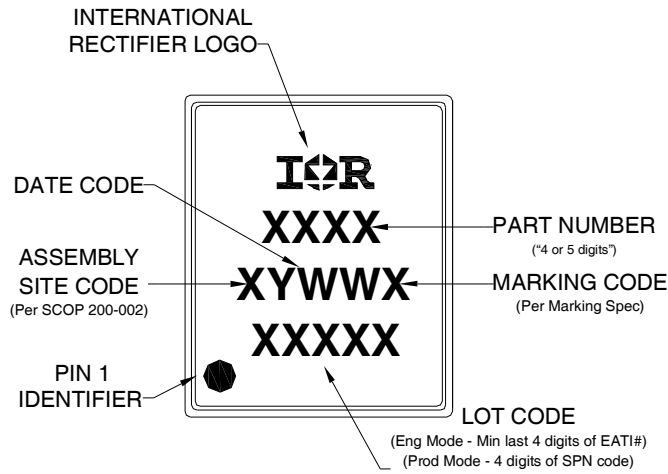
<http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154:

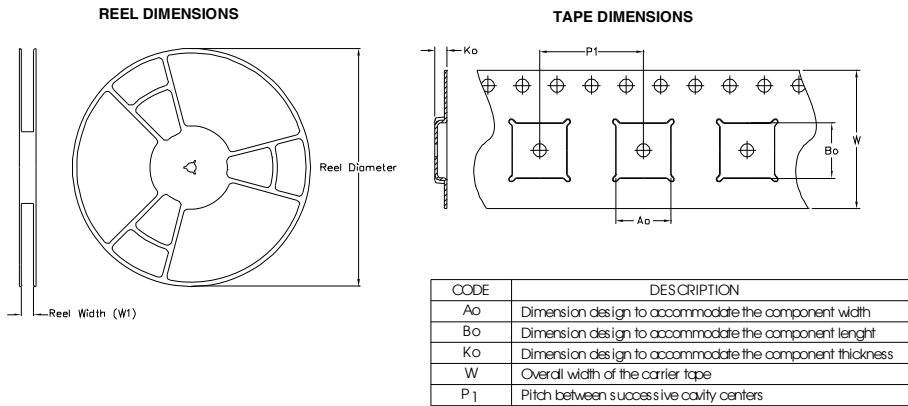
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**Note:** For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

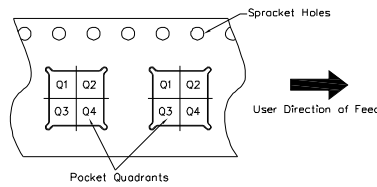
# PQFN 5x6 Part Marking



# PQFN 5x6 Tape and Reel



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>



**Qualification information†**

Qualification level	Industrial <sup>††</sup> (per JEDEC JES D47F <sup>†††</sup> guidelines )	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site  
<http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements.  
 Please contact your International Rectifier sales representative for further information:  
<http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.63\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 20\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④  $R_\theta$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Package is limited to 80A by die-source to lead-frame bonding technology

**Revision History**

Date	Comment
5/12/2014	<ul style="list-style-type: none"> <li>• Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259)</li> <li>• Updated Tape and Reel on page 8.</li> <li>• Updated data sheet based on corporate template.</li> </ul>
6/2/2015	<ul style="list-style-type: none"> <li>• Updated package outline for “option E” and added package outline for “option G” on page 7.</li> <li>• Updated “IFX” logo on page 1 &amp; 9.</li> <li>• Updated tape and reel on page 8.</li> </ul>
7/7/2015	<ul style="list-style-type: none"> <li>• Corrected package outline for “option E” on page 7.</li> </ul>