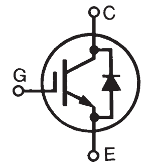
IXYS

Preliminary Technical Information

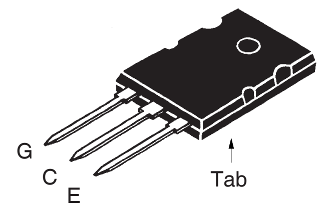
BiMOSFET™ Monolithic Bipolar MOS Transistor

IXBK75N170
IXBX75N170

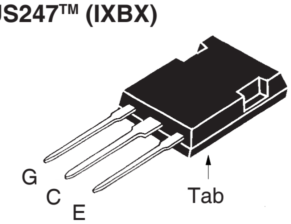
V_{CES} = 1700V
I_{C110} = 75A
$V_{CE(sat)}$ ≤ 3.1V



TO-264 (IXBK)



PLUS247™ (IXBX)



G = Gate C = Collector
E = Emitter Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	1700	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	1700	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C (Chip Capabilitty)	200	A
I_{LRMS}	T_C = 25°C (Lead RMS Limit)	160	A
I_{C110}	T_C = 110°C	75	A
I_{CM}	T_C = 25°C, 1ms	580	A
SSOA	V_{GE}= 15V, T_{VJ} = 125°C, R_G = 1Ω	I_{CM} = 150	A
(RBSOA)	Clamped Inductive Load	V_{CE} ≤ 0.8 • V_{CES}	
P_C	T_C = 25°C	1040	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in.
F_C	Mounting Force (PLUS247)	20..120/4.5..27	N/lb.
Weight	TO-264	10	g
	PLUS247	6	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 250μA, V_{GE} = 0V	1700			V
$V_{GE(th)}$	I_C = 1.5mA, V_{CE} = V_{GE}	2.5		5.5	V
I_{CES}	V_{CE} = 0.8 • V_{CES}, V_{GE} = 0V			25	μA
	T_J = 125°C			2	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 20V			±100	nA
$V_{CE(sat)}$	I_C = I_{C110}, V_{GE} = 15V, Note 1		2.6	3.1	V
	T_J = 125°C		3.1		V

Features

- International Standard Packages
- High Blocking Voltage
- High Current Handling Capability
- Anti-Parallel Diode

Advantages

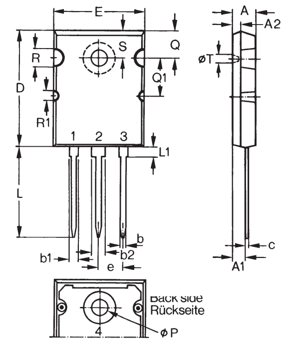
- High Power Density
- Low Gate Drive Requirement
- Intergrated Diode Can Be Used for Protection

Applications

- Capacitor Discharge
- AC Switches
- Switch-Mode and Resonant-Mode Power Supplies
- UPS
- AC Motor Drives

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fS}	$I_C = I_{C110}$, V_{CE} = 10V, Note 1	34	56		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		6930		pF
C_{oes}			400		pF
C_{res}			150		pF
Q_g	$I_C = I_{C110}$, V_{GE} = 15V, V_{CE} = 0.5 • V_{CES}		350		nC
Q_{ge}			50		nC
Q_{gc}			160		nC
$t_{d(on)}$	**Resistive load, T_J = 25°C**		46		ns
t_r	$I_C = I_{C110}$, V_{GE} = 15V		160		ns
$t_{d(off)}$	R_G = 1Ω, V_{CE} = 0.5 • V_{CES}		260		ns
t_f			440		ns
$t_{d(on)}$	**Resistive load, T_J = 125°C**		47		ns
t_r	$I_C = I_{C110}$, V_{GE} = 15V		230		ns
$t_{d(off)}$	R_G = 1Ω, V_{CE} = 0.5 • V_{CES}		260		ns
t_f			580		ns
R_{thJC}				0.12	°C/W
R_{thCS}			0.15		°C/W

TO-264 AA (IXBK) Outline



Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.82	5.13	.190	.202
A1	2.54	2.89	.100	.114
A2	2.00	2.10	.079	.083
b	1.12	1.42	.044	.056
b1	2.39	2.69	.094	.106
b2	2.90	3.09	.114	.122
c	0.53	0.83	.021	.033
D	25.91	26.16	1.020	1.030
E	19.81	19.96	.780	.786
e	5.46 BSC		.215 BSC	
J	0.00	0.25	.000	.010
K	0.00	0.25	.000	.010
L	20.32	20.83	.800	.820
L1	2.29	2.59	.090	.102
P	3.17	3.66	.125	.144
Q	6.07	6.27	.239	.247
Q1	8.38	8.69	.330	.342
R	3.81	4.32	.150	.170
R1	1.78	2.29	.070	.090
S	6.04	6.30	.238	.248
T	1.57	1.83	.062	.072

Reverse Diode

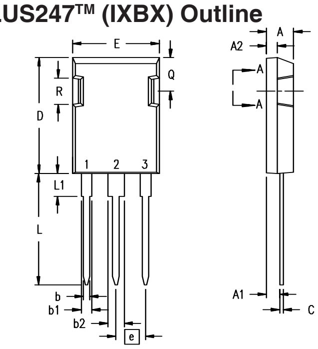
Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
V_F	$I_F = I_{C110}$, V_{GE} = 0V, Note 1			3.0	V
t_{rr}	I_F = 37A, V_{GE} = 0V, -di_F/dt = 100A/μs		1.5		μs
I_{RM}	V_R = 100V, V_{GE} = 0V		50		A
Q_{RM}			38.2		μC

Note

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.

Additional provisions for lead-to-lead isolation are required at V_{CE} >1200V.

PLUS247™ (IXBX) Outline



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ 25ºC

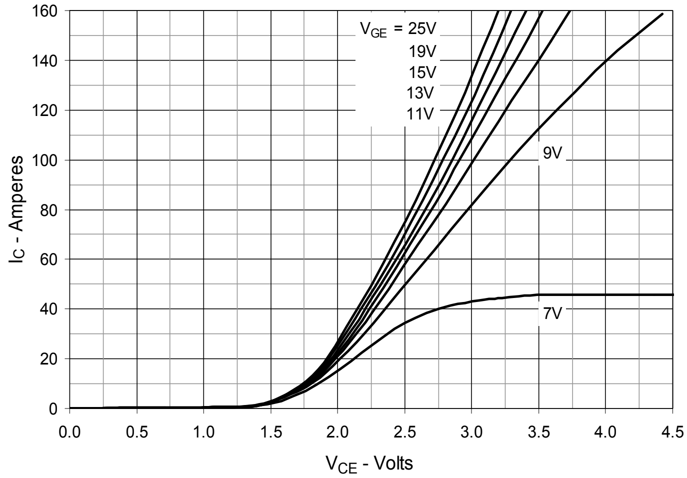


Fig. 2. Extended Output Characteristics @ 25ºC

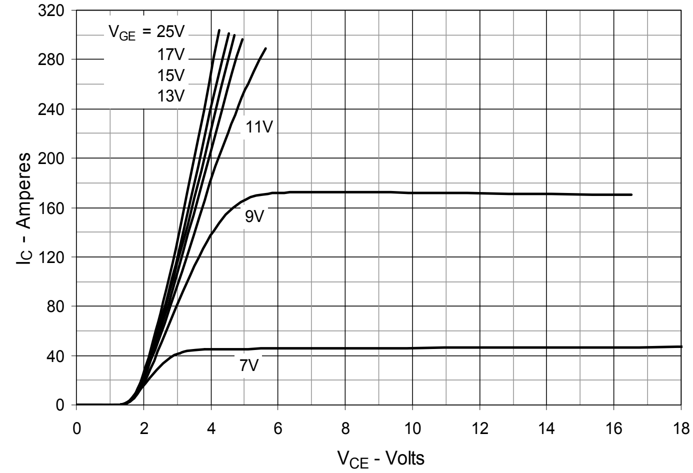


Fig. 3. Output Characteristics @ 125ºC

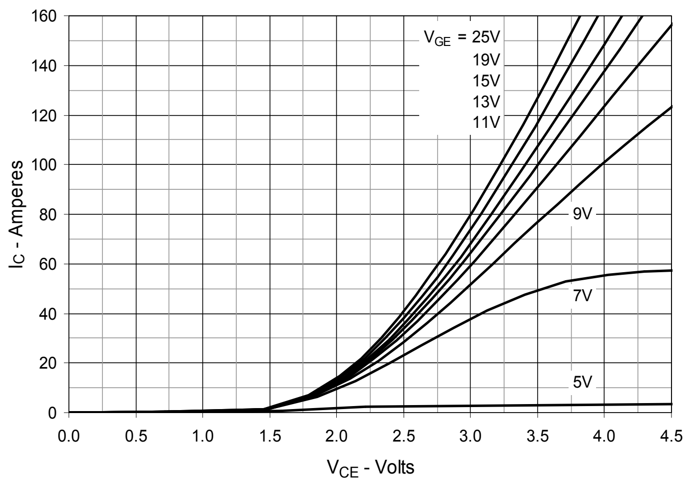


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

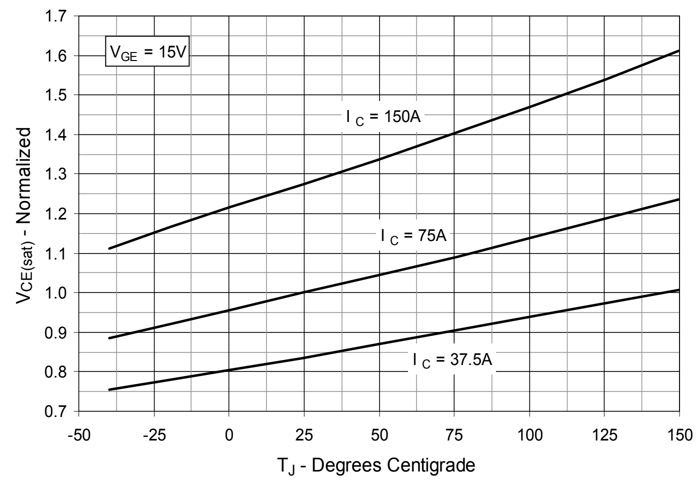


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

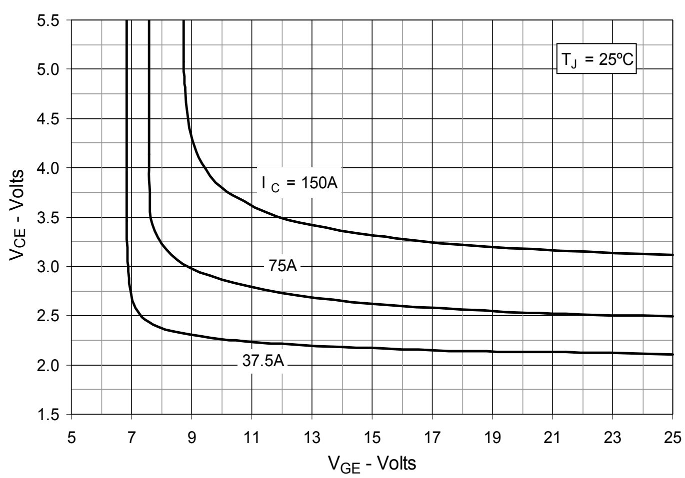


Fig. 6. Input Admittance

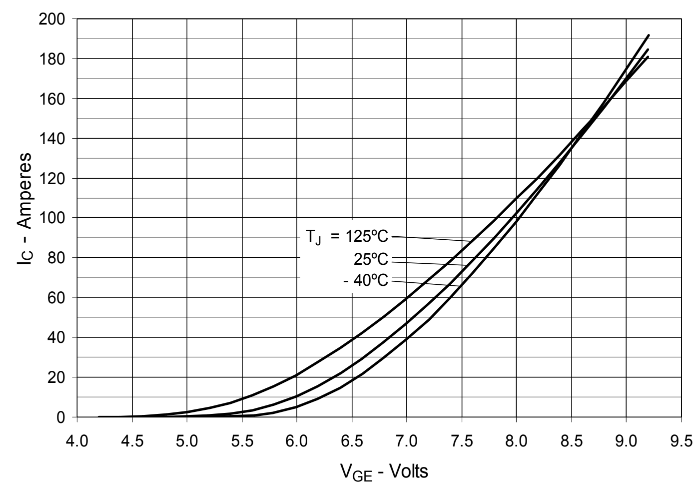


Fig. 7. Transconductance

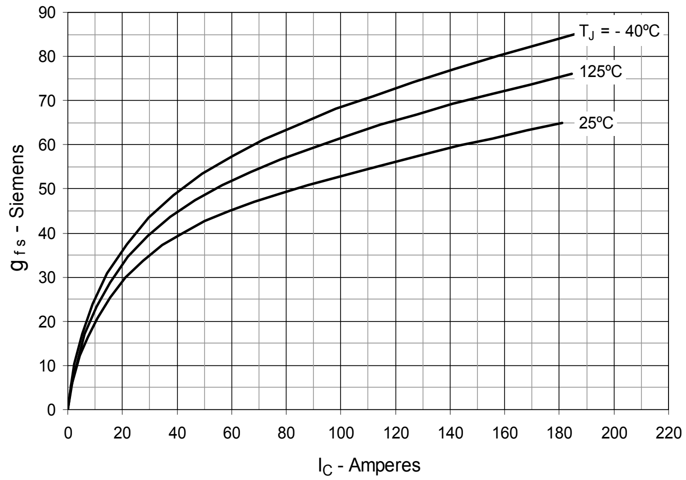


Fig. 8. Forward Voltage Drop of Intrinsic Diode

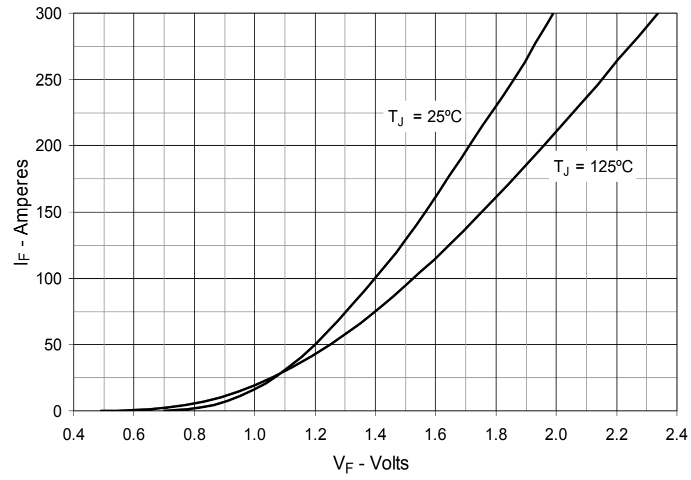


Fig. 9. Gate Charge

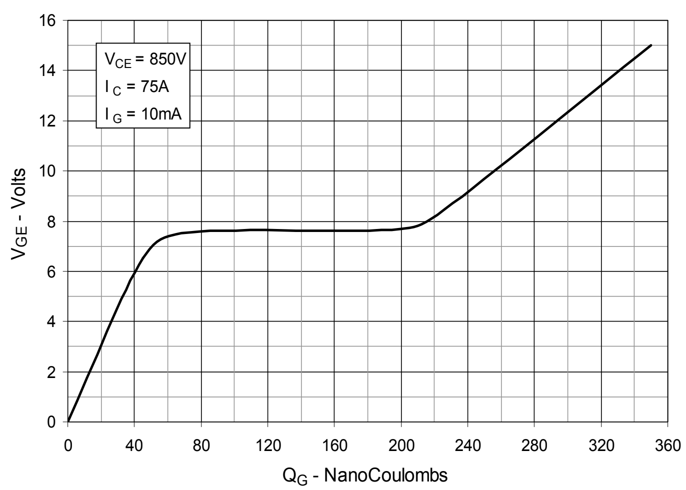


Fig. 10. Capacitance

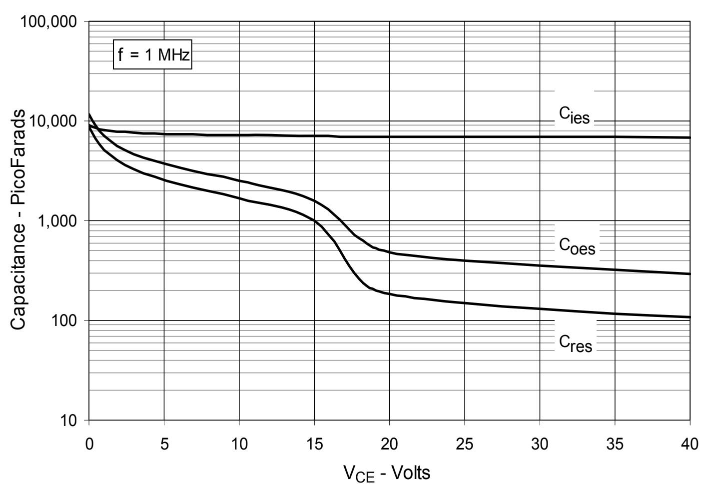


Fig. 11. Reverse-Bias Safe Operating Area

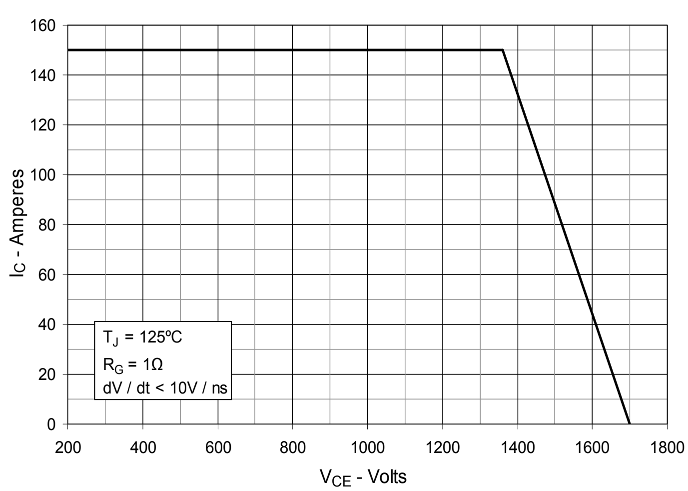


Fig. 12. Maximum Transient Thermal Impedance

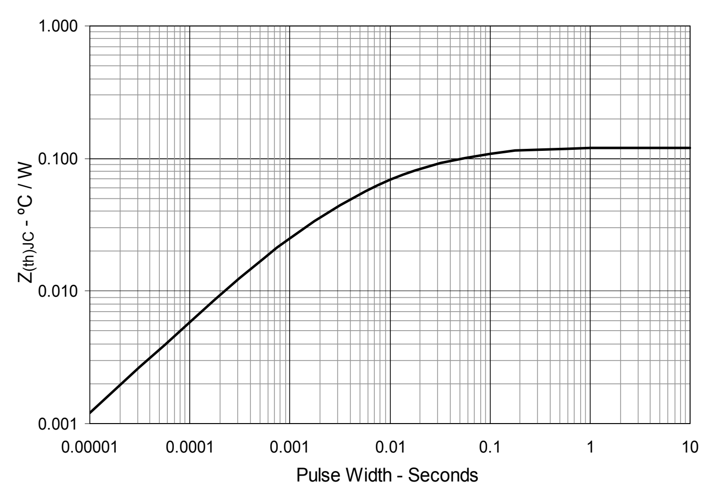


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

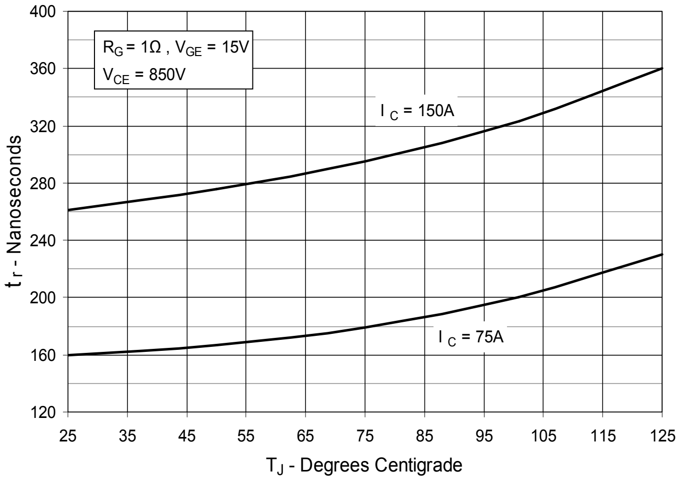


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

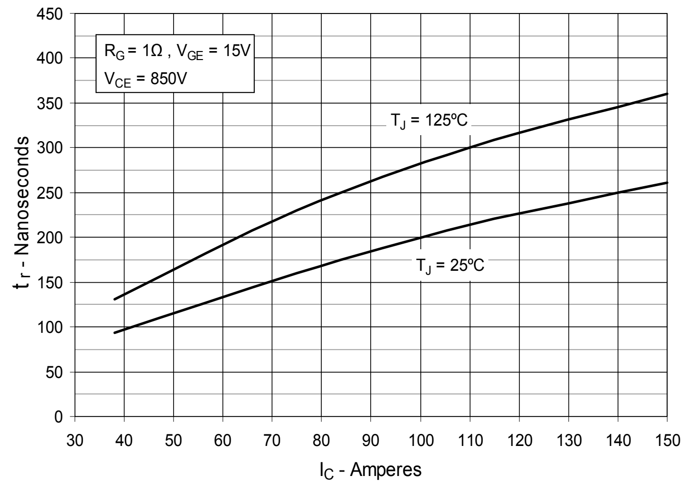


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

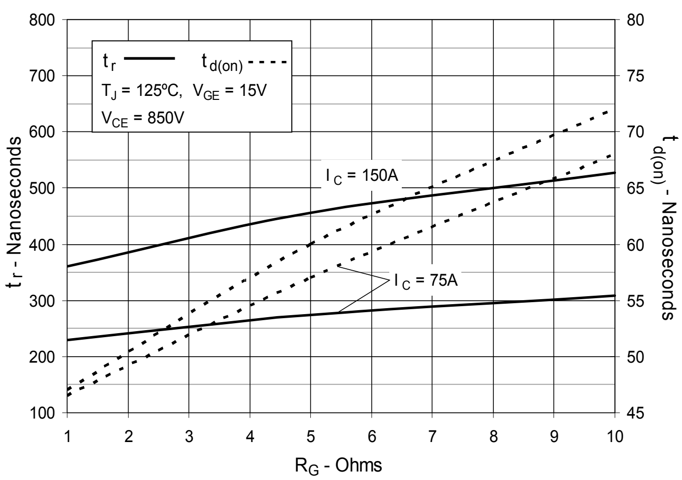


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

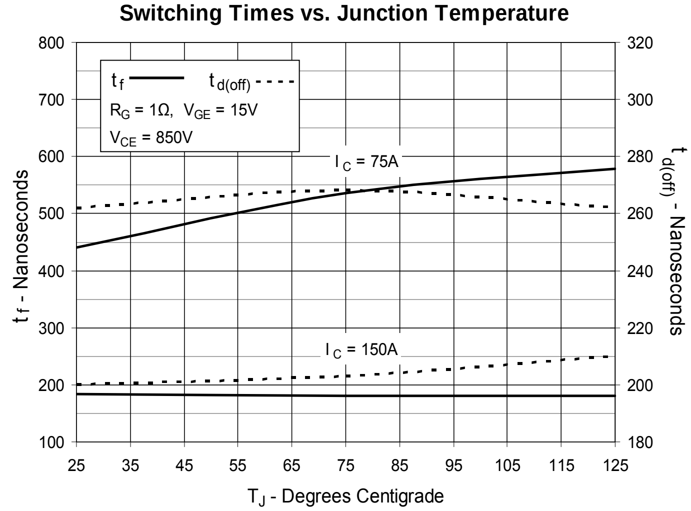


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

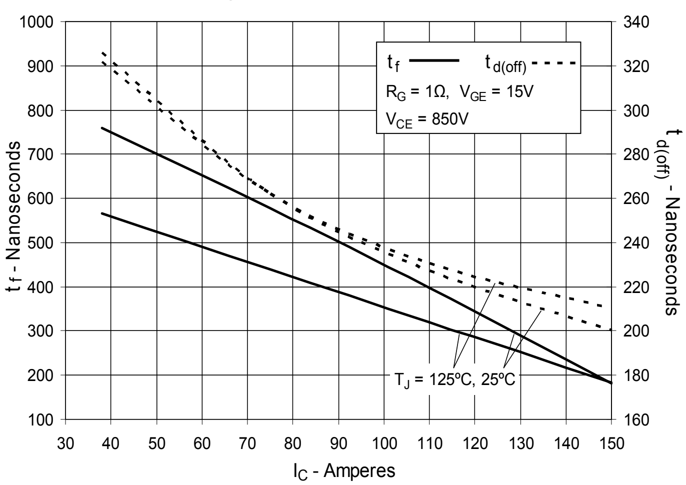


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance