NOT RECOMMENDED FOR NEW DESIGNS
SEE ISL6414

November 2003 FN9081.2

Triple Output, Low-Noise LDO Regulator with Integrated Reset Circuit

The ISL6411 is an ultra low noise triple output LDO regulator with microprocessor reset circuit and is optimized for powering wireless chip sets. The IC accepts an input voltage range of 3.0V to 3.6V and provides three regulated output voltages: 1.8V (LDO1), 2.84V (LDO2), and another ultra clean 2.84V (LDO3). On chip logic provides sequencing between LDO1 and LDO2 for BBP/MAC and I/O supply voltage outputs. LDO3 features ultra low noise that does not typically exceed 30µV RMS to aid VCO stability. High integration and the thin Quad Flat No-lead (QFN) package makes ISL6411 an ideal choice to power many of today's small form factor industry standard wireless cards, such as PCMCIA, mini-PCI and Cardbus-32.

The ISL6411 uses an internal PMOS transistor as the pass device. The SHDN pin controls LDO1 and LDO2 outputs whereas SHDN3 controls LDO3 output. Internal voltage sequencing insures that LDO1 output (1.8V supply) is always stabilized before LDO2 is turned on. When powering down, power to the LDO2 is removed before the LDO1 output goes off. The ISL6411 also integrates RESET function, which eliminates the need for additional RESET IC required in WLAN applications. The IC asserts a RESET signal whenever the VIN supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after Vin has risen above the reset threshold. An output fault detection circuit indicates loss of regulation on any of the three outputs. Other features include an over current protection, thermal shutdown and reverse battery protection.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6411IR	-40 to +85	16 Ld QFN	L16.4x4
ISL6411IRZ (Note)	-40 to +85	16 Ld QFN	L16.4x4

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

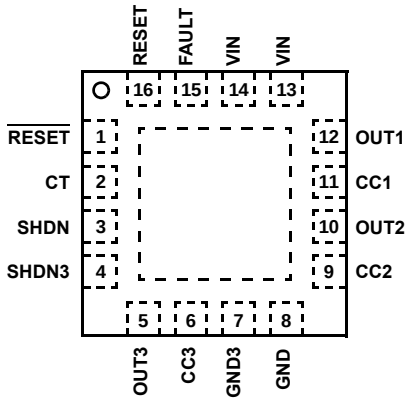
- Small DC/DC Converter Size
  - Three LDOs and RESET Circuitry in a Low-Profile 4x4mm QFN Package
- High Output Current
  - LDO1, 1.8V 500mA
  - LDO2, 2.84V 300mA
  - LDO3, 2.84V 200mA
- Ultra-Low Dropout Voltage
  - LDO2, 2.84V . . . . . 125mV (typ.) at 300mA
  - LDO3, 2.84V . . . . . 100mV (typ.) at 200mA
- Ultra-Low Output Voltage Noise
  - $<30\mu V_{RMS}$ (typ.) for LDO3 (VCO Supply)
- Stable with Smaller Ceramic Output Capacitors
- Voltage Sequencing for BBP/MAC and Analog Supplies
- Extensive Protection and Monitoring Features
  - Over current protection
  - Short circuit protection
  - Thermal shutdown
  - Reverse battery protection
  - FAULT indicator
- Logic-Controlled Dual Shutdown Pins
- Integrated Microprocessor Reset Circuit
  - Programmable Reset Delay
  - Complimentary Reset Outputs
- Proven Reference Design for Total WLAN System Solution
- QFN Package Option
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale Package Footprint Improves PCB Efficiency and Is Thinner in Profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

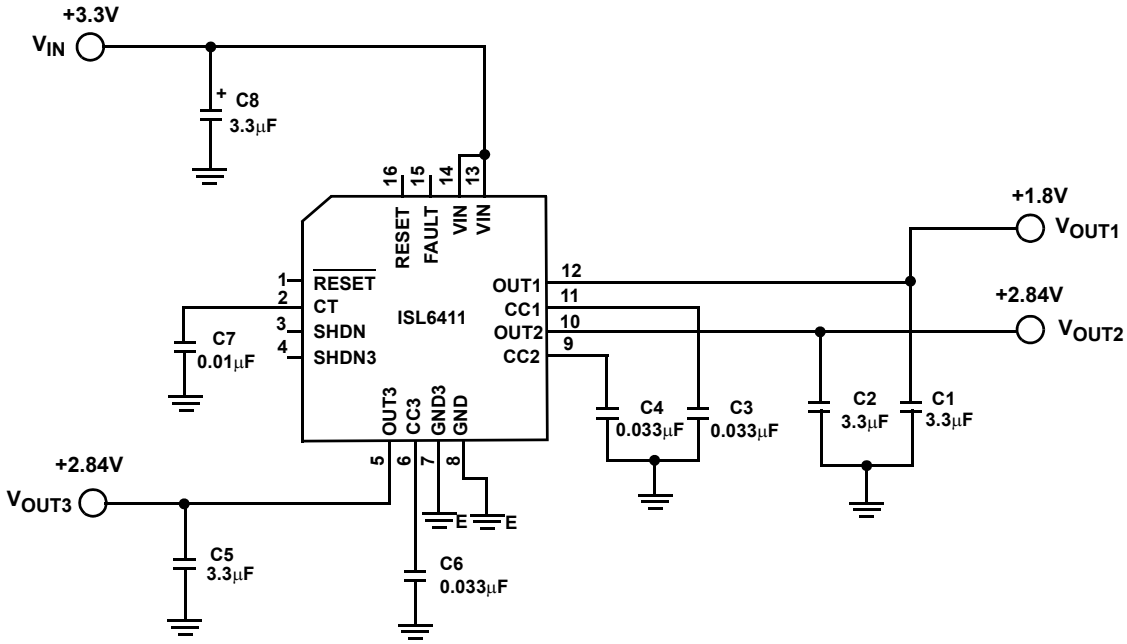
- PRISM® 3, PRISM GT™, and PRISM WWR Chipsets
- WLAN Cards
  - PCMCIA, Cardbus32, MiniPCI Cards
  - Compact Flash Cards
- Hand-Held Instruments

Pinout

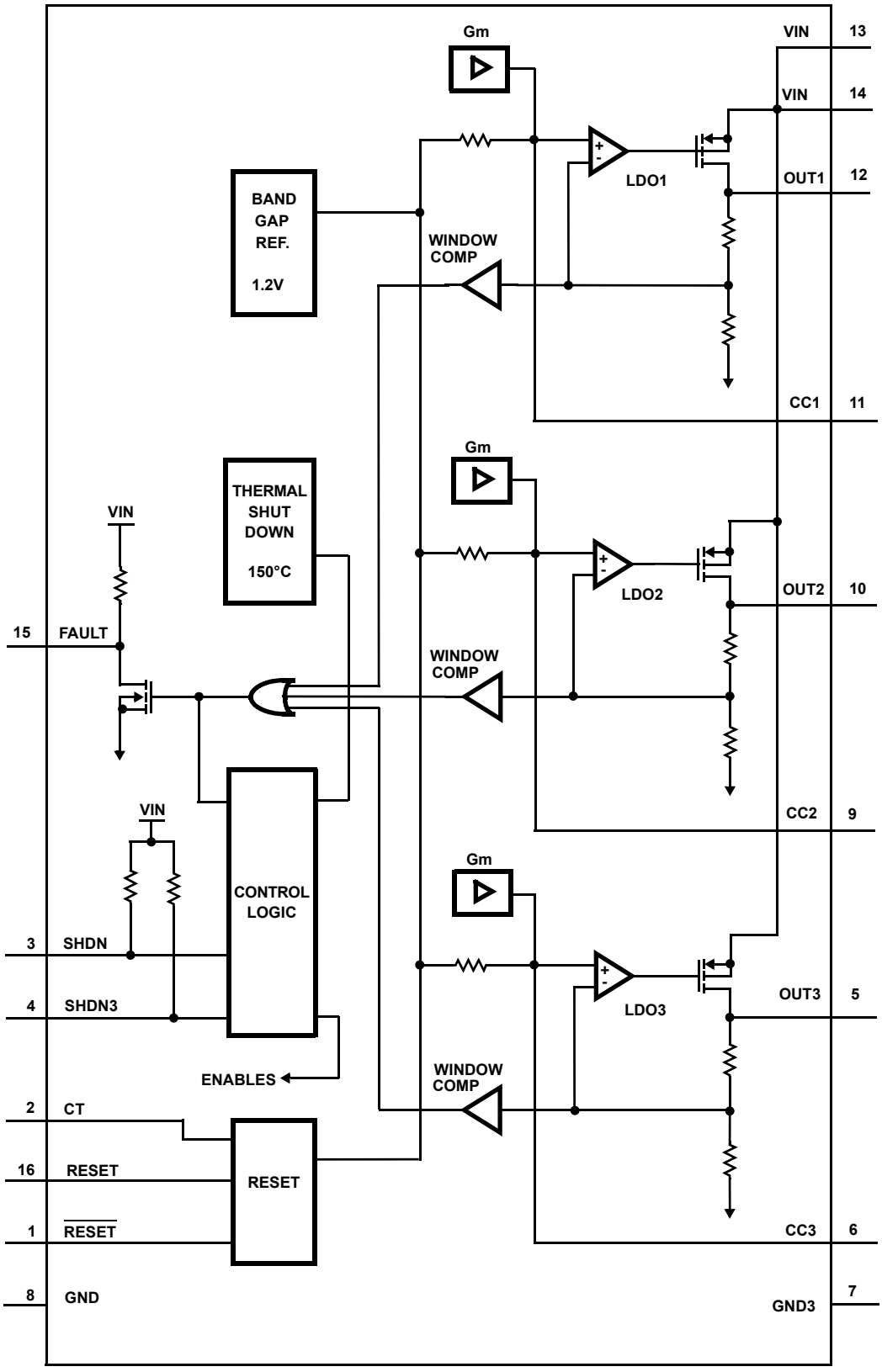
ISL6411 (QFN)
TOP VIEW



Typical Application Schematic



Functional Block Diagram



Absolute Maximum Ratings (Note 1)

V_{IN}, SHDN/SHDN3 to GND/GND3 . . . . . -7.0V to 7.0V
SET, CC, FAULT to GND/GND3 . . . . . -0.3V to 7.0V
Output Current (Continuous)
LDO1 . . . . . 500mA
LDO2 . . . . . 300mA
LDO3 . . . . . 200mA
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical, Notes 2, 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package.	46	7.5

Maximum Junction Temperature (Plastic Package) . -55°C to 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
Operating Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. All voltages are with respect to GND.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

V_{IN} = +3.3V, Compensation Capacitor = 33nF, T_A = 25°C, Unless Otherwise Noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL SPECIFICATIONS					
V_{IN} Voltage Range		3.0	3.3	3.6	V
Operating Supply Current	IOUT = 0mA	-	600	850	µA
Shutdown Supply Current	SHDN/SHDN3 = GND	-	5	10	µA
SHDN/SHDN3 Input Threshold	VIH, VIN = 3V to 3.6V	2.0	-	-	V
	VIL, VIN = 3V to 3.6V	-	-	0.4	V
FAULT Output Low Voltage	I_{SINK} = 2mA	-	-	0.25	V
Thermal Shutdown Temperature (Note 7)		145	150	160	°C
Thermal Shutdown Hysteresis		-	20	-	°C
Start-up Time	C_{OUT} = 10µF, V_{OUT} = 90% of final value	-	120	-	µs
Input Undervoltage Lockout (Note 7)	Rising 75mV Hysteresis	2.2	2.45	2.65	V
LDO1 SPECIFICATIONS					
Output Voltage (V_{OUT1})		-	1.8	-	V
Output Voltage Accuracy	I_{OUT} = 10mA	-1.5	-	1.5	%
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 500mA	-1.5	-	1.5	%
Maximum Output Current (I_{OUT1}) (Note 7)		500	-	-	mA
Output Current Limit (Note 7)		0.55	0.6	1.0	A
Output Voltage Noise	10Hz < f < 100kHz, C_{OUT} = 4.7µF, I_{OUT} = 50mA	-	115	-	μV_{RMS}
LDO2 SPECIFICATIONS					
Output Voltage (V_{OUT2})		-	2.84	-	V
Output Voltage Accuracy	I_{OUT} = 10mA	-1.5	-	1.5	%
Maximum Output Current (I_{OUT2}) (Note 7)	VIN = 3.6V	300	-	-	mA
Output Current Limit (Note 7)		330	770	-	mA
Dropout Voltage (Note 5)	I_{OUT} = 300mA	-	125	220	mV
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V

Electrical Specifications V_{IN} = +3.3V, Compensation Capacitor = 33nF, T_A = 25°C, Unless Otherwise Noted. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Load Regulation	I_{OUT} = 10mA to 300mA	-	0.2	1.0	%
Output Voltage Noise	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	65	-	μV_{RMS}
	C_{OUT} = 10µF	-	60	-	μV_{RMS}
LDO3 SPECIFICATIONS					
Output Voltage (V_{OUT3})		-	2.84	-	V
Output Voltage Accuracy	I_{OUT} = 10mA	-1.5	-	1.5	%
Maximum Output Current (I_{OUT3}) (Note 7)	VIN = 3.6V	200	-	-	mA
Output Current Limit (Note 7)		250	400	-	mA
Dropout Voltage (Note 5)	I_{OUT} = 200mA	-	100	200	mV
Line Regulation	V_{IN} = 3.0V to 3.6V, I_{OUT} = 10mA	-0.15	0.0	0.15	%/V
Load Regulation	I_{OUT} = 10mA to 200mA	-	0.2	1.0	%
Output Voltage Noise	10Hz < f < 100kHz, I_{OUT} = 10mA				
	C_{OUT} = 2.2µF	-	30	-	μV_{RMS}
	C_{OUT} = 10µF	-	20	-	μV_{RMS}
RESET BLOCK SPECIFICATIONS					
RESET Threshold		2.564	2.630	2.696	V
RESET Threshold Hysteresis (Note 7)		6.3	-	-	mV
V_{IN} to RESET Delay	VCC = V_{TH} to V_{TH} - 100mV	-	20	-	µs
RESET/$\overline{\text{RESET}}$ Active Timeout Period (Notes 6, 7)		25	-	-	ms

NOTES:

4. Specifications at -40°C are guaranteed by design/characterization, not production tested.
5. The dropout voltage is defined as V_{IN} - V_{OUT} , when V_{OUT} is 50mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 0.5V.
6. The RESET time is linear with CT at a slope of 2.5ms/nF. Thus, at 10nF (0.01µF) the RESET time is 25ms; at 100nF (0.1µF) the RESET time would be 250ms.
7. Guaranteed by design, not production tested.

Typical Performance Curves

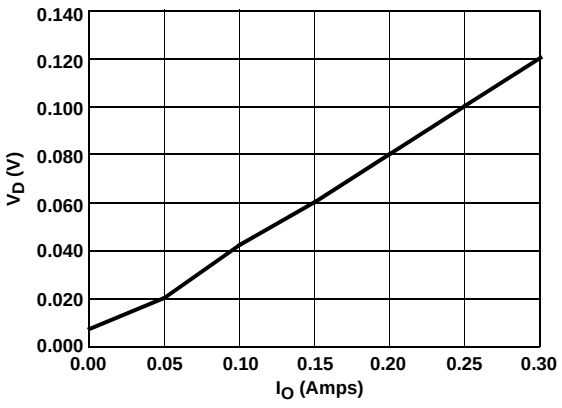


FIGURE 1. LD02 DROPOUT VOLTAGE

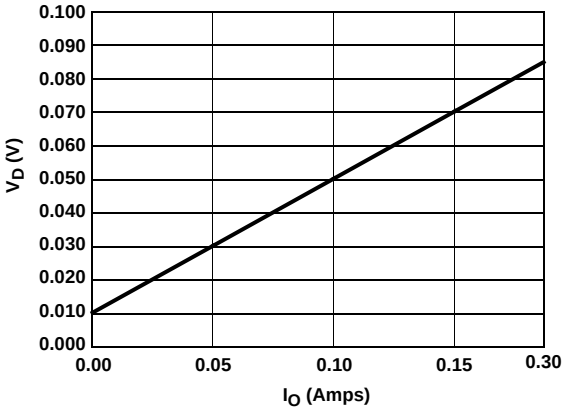


FIGURE 2. LD03 DROPOUT VOLTAGE

Typical Performance Curves (Continued)

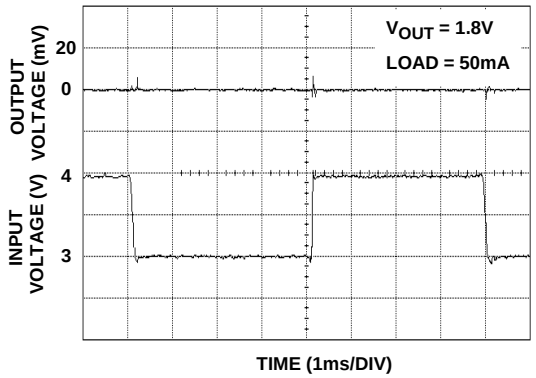


FIGURE 3. LINE REGULATION RESPONSE ($V_{OUT}1$)

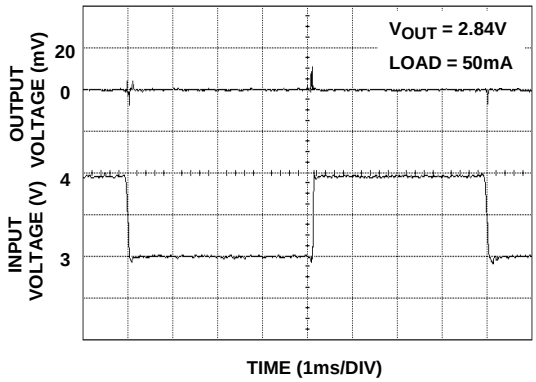


FIGURE 4. LINE REGULATION RESPONSE ($V_{OUT}2$)

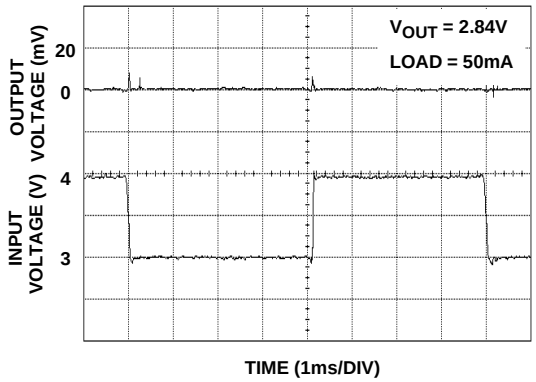


FIGURE 5. LINE REGULATION RESPONSE ($V_{OUT}3$)

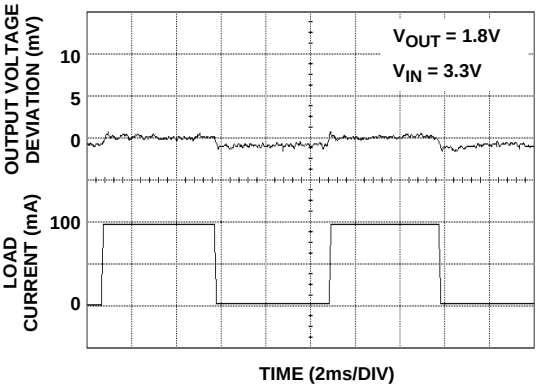


FIGURE 6. LOAD REGULATION RESPONSE ($V_{OUT}1$)

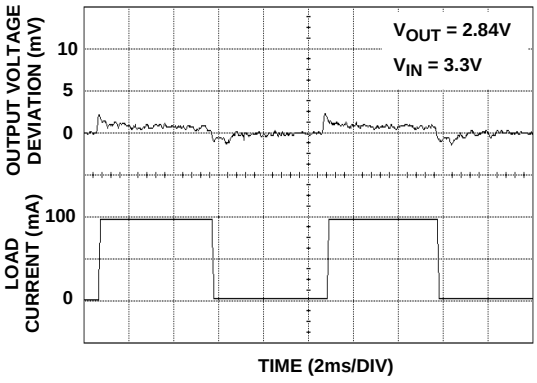


FIGURE 7. LOAD REGULATION RESPONSE ($V_{OUT}2$)

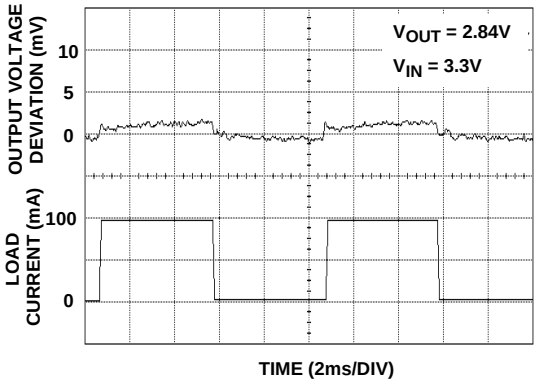


FIGURE 8. LOAD REGULATION RESPONSE ($V_{OUT}3$)

Typical Performance Curves (Continued)

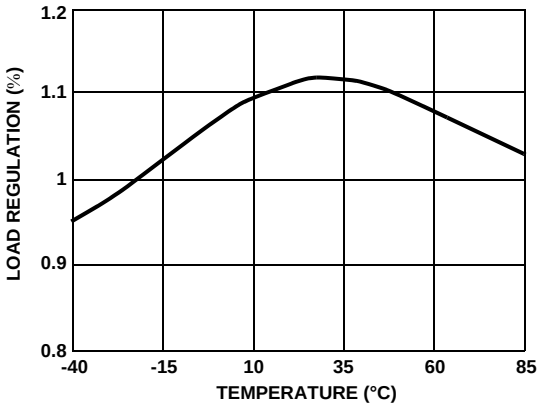


FIGURE 9. LD01 LOAD REGULATION vs TEMPERATURE

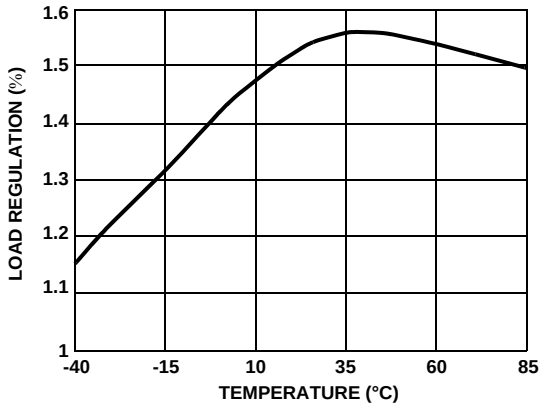


FIGURE 10. LD02 LOAD REGULATION vs TEMPERATURE

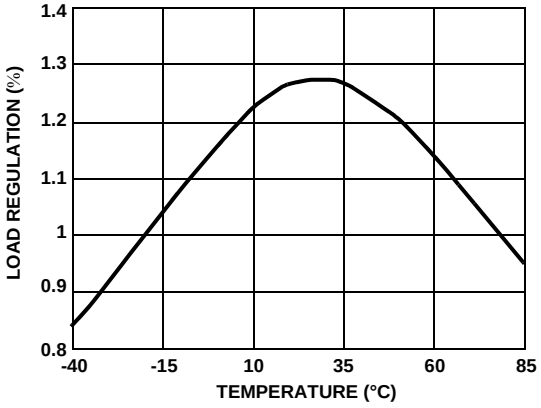


FIGURE 11. LD03 LOAD REGULATION vs TEMPERATURE

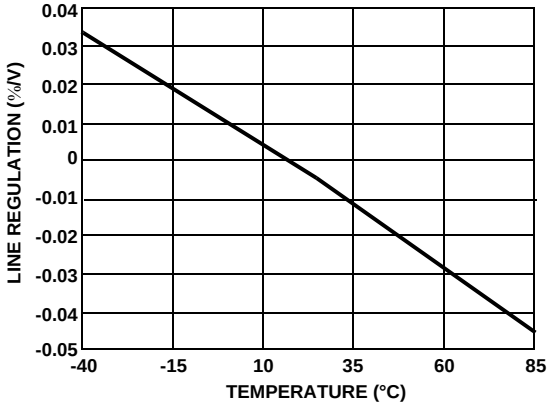


FIGURE 12. LD01 LINE REGULATION vs TEMPERATURE

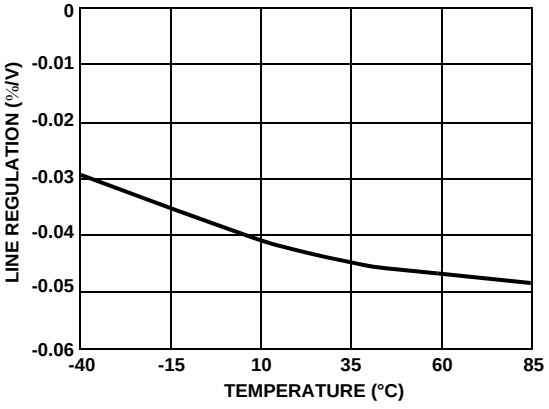


FIGURE 13. LD02 LINE REGULATION vs TEMPERATURE

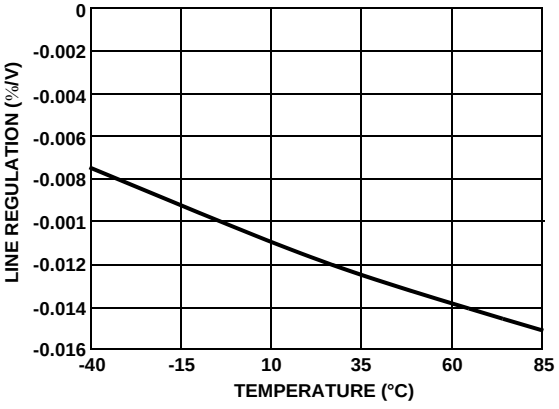


FIGURE 14. LD03 LINE REGULATION vs TEMPERATURE

Typical Performance Curves (Continued)

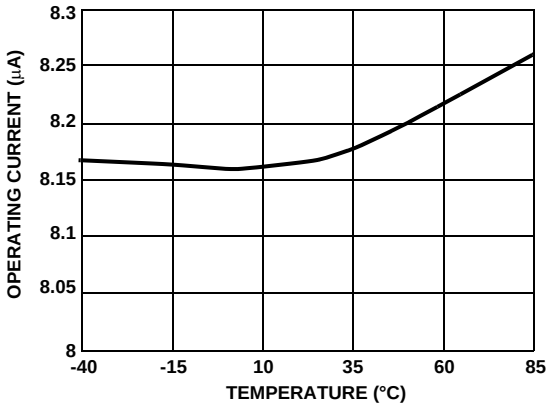


FIGURE 15. SHUTDOWN CURRENT vs TEMPERATURE

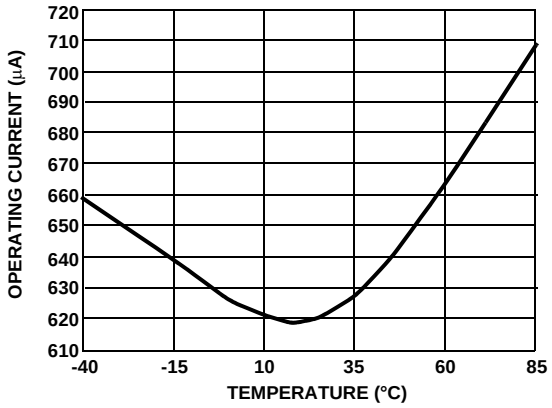


FIGURE 16. OPERATING CURRENT vs TEMPERATURE

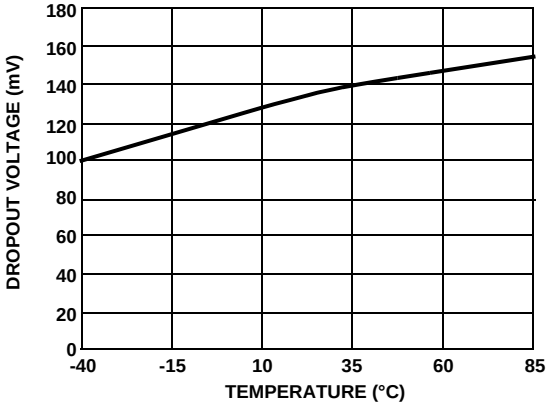


FIGURE 17. LD02 DROPOUT VOLTAGE vs TEMPERATURE

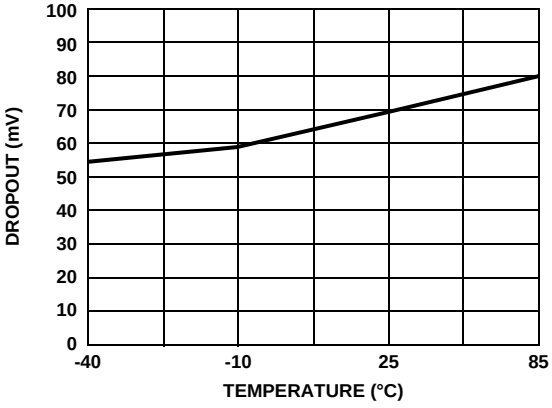


FIGURE 18. LD03 DROPOUT VOLTAGE vs TEMPERATURE

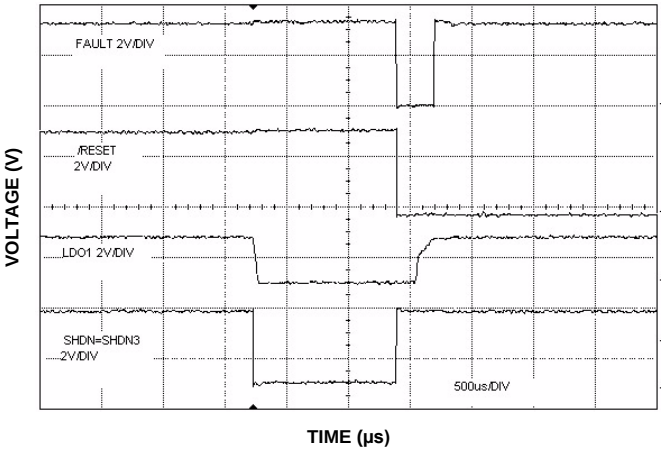


FIGURE 19. SHUTDOWN

Pin Descriptions

OUT1 - This pin is the output for LDO1. Bypass with a minimum of 2.2µF, low ESR capacitor to GND for stable operation.

V_{IN} - Supply input pins. Connect to input power source. Bypass with 2.2µF capacitor to GND. Both V_{IN} pins must be tied together on the PC board, close to the IC.

GND - Ground pin for LDO1 and LDO2.

CC1 - Compensation Capacitor for LDO1. Connect a 0.033µF capacitor from CC1 to GND.

SHDN - Shutdown input for LDO1 and LDO2. Connect to IN for normal operation. Drive SHDN pin LOW to turn off LDO1 and LDO2.

OUT2 - This pin is the output for LDO2. Bypass with a minimum of 2.2µF, low ESR capacitor to GND for stable operation.

CT - Timing pin for the RESET circuit pulse width.

CC2 - Compensation capacitor for LDO2. Connect a 0.033µF capacitor from CC2 to GND.

OUT3 - This pin is output for LDO3. Bypass with a minimum of 2.2µF, low ESR capacitor to GND3 for stable operation.

GND3 - Ground pin for LDO3.

CC3 - Compensation capacitor for LDO3. Connect a 0.033µF capacitor from CC3 to GND3.

SHDN3 - Shutdown input for LDO3. Connect to V_{IN} for normal operation. Drive SHDN3 pin LOW to turn off LDO3.

FAULT - FAULT output for LDO's. This output is combined for LDO1, LDO2 and LDO3. When any LDO is out of regulation, FAULT goes LOW; when all SHDN inputs are low, FAULT will be high (refer to Figure 19). Connect to GND, if unused.

$\overline{\text{RESET}}$ - This pin is the active-LOW output of the push-pull output stage of the integrated reset supervisory circuit. The reset circuit monitors V_{IN} and asserts a $\overline{\text{RESET}}$ output at this pin, if V_{IN} falls below the RESET threshold. The $\overline{\text{RESET}}$ output remains LOW, while the V_{IN} pin voltage is below the reset threshold, and for at least 25ms, after V_{IN} rises above the RESET threshold.

RESET - This pin is the active-HIGH output of the push-pull output stage of the integrated reset supervisory circuit. The reset circuit monitors V_{IN} and asserts a RESET output at this pin, if V_{IN} falls below the RESET threshold. The RESET output remains HIGH, while the V_{IN} pin voltage is below the RESET threshold, and for at least 25ms, after V_{IN} rises above the RESET threshold.

Functional Description

The ISL6411 is a 3-in-1 multi-output, low dropout, regulator designed for wireless chipset power applications. It supplies three fixed output voltages 1.8V, 2.84V and 2.84V. Each LDO consists of a 1.2V reference, error amplifier, MOSFET driver, P-Channel pass transistor, dual-mode comparator and internal feedback voltage divider.

The 1.2V band gap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference to the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-Channel pass transistor. If the feedback voltage is lower then the reference voltage, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher then the reference voltage, the pass transistor gate is driven higher, allowing less current to pass to the output. The output voltage is fed back through an internal resistor divider connected to OUT1/2/3 pins.

Additional blocks include an output over-current protection, reverse battery protection, thermal sensor, fault detector, RESET function and shutdown logic.

Internal P-Channel Pass Transistors

The ISL6411 features a typical 0.5Ω $R_{DS(ON)}$ P-channel MOSFET pass transistors. This provides several advantages over similar designs using PNP bipolar pass transistors. The P-Channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable current in dropout when the pass transistor saturates. They also use high base drive currents under large loads. The ISL6411 does not suffer from these problems.

Integrated RESET for MAC/Baseband Processors

The ISL6411 includes a microprocessor supervisory block. This block eliminates the extra RESET IC and external components needed in wireless chipset applications. This block performs a single function; it asserts a RESET signal whenever the V_{IN} supply voltage decreases below a preset threshold, keeping it asserted for a programmable time (set by external capacitor CT) after the V_{IN} pin voltage has risen above the RESET threshold.

The push pull output stage of the reset circuit provides both an active-Low and an active-HIGH output. This function is guaranteed to be in the correct state for V_{IN} down to 1V. The reset comparator is designed to ignore transients on the V_{IN} pin. The RESET threshold for ISL6411 is 2.63V typical.

In addition to issuing a reset to the microprocessor during power-up, power down and brownout conditions, this block is relatively immune to short duration, negative-going V_{IN} transients/glitches.

Output Voltages

The ISL6411 provides fixed output voltages for use in Wireless Chipset applications. Internal trimmed resistor networks set the typical output voltages as shown here:

V_{OUT1} = 1.8V; V_{OUT2} = 2.84V; V_{OUT3} = 2.84V.

Shutdown

Driving the SHDN input LOW puts both LDO1 and LDO2 in shutdown mode. Driving the SHDN3 input LOW puts LDO3 in shutdown mode. Pulling the SHDN and SHDN3 pins LOW simultaneously, puts the complete chip into shutdown mode, and supply current drops to 5µA typical. Both SHDN and SHDN3 inputs have internal pull-up resistors, so that in normal operation the outputs are always enabled; external pull-up resistors are not required. During shutdown mode using the SHDN pin, the FAULT output will remain HIGH (refer to Figure 19).

Current Limit

The ISL6411 monitors and controls the pass transistor's gate voltage to limit the output current. The current limit for LDO1 is 550mA, LDO2 is 330mA and LDO3 is 250mA. The output can be shorted to ground without damaging the part due to the current limit and thermal protection features.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the ISL6411. When the junction temperature (T_J) exceeds +150°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The pass transistor turns on again after the IC's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection protects the ISL6411 against fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of +150°C.

Operating Region and Power Dissipation

The maximum power dissipation of ISL6411 depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipated in the device is:

PT = P1 + P2 + P3, where

P1 = Iout1 (Vin – Vout1)

P2 = Iout2 (Vin – Vout2)

P3 = Iout3 (Vin- Vout3)

The maximum power dissipation is:

Pmax = (Tjmax – Ta)/θJA

Where Tjmax = 150°C, Ta = ambient temperature, and θJA is the thermal resistance from the junction to the surrounding environment.

The ISL6411 package features an exposed thermal pad on its underside. This pad lowers the thermal resistance of the package by providing a direct heat conduction path from the die to the PC board. Additionally, the ISL6411's ground (GND/GND3) performs the dual function of providing an electrical connection to system ground and channeling heat away. Connect the exposed backside pad and GND to the system ground using a large pad or ground plane, or through multiple vias to the ground plane layer.

Reverse Input Protection

The ISL6411 has a unique protection scheme that limits the reverse supply current to less than 1mA when V_{IN} falls below GND. The circuitry monitors the polarity of these two pins, disconnecting the internal circuitry and parasitic diodes when the applied voltage is reversed. This feature prevents the device from overheating and damaging an improperly installed input supply.

Integrator Circuitry

The ISL6411 uses an external 33nF compensation capacitor for minimizing load and line regulation errors and for lowering output noise. When the output voltage shifts due to varying load current or input voltage, the integrator capacitor voltage is raised or lowered to compensate for the systematic offset at the error amplifier. Compensation is limited to ±5% to minimize transient overshoot when the device goes out of dropout, current limit, or thermal shutdown.

Fault-Detection Circuitry

The FAULT pin monitors all three LDO outputs regulation as well as fault conditions such as current limit and thermal shutdown. The FAULT output goes low if outputs are out of regulation or the device is in any of the fault modes. In addition, the fault-detection circuitry detects when the input-to-output voltage differential for LDO2/3 (<90mV) is insufficient to ensure good load and line regulation at the output. During shutdown mode using the SHDN pin, the FAULT output will remain HIGH (refer to Figure 19).

Applications Information

Capacitor Selection and Regulator Stability

Capacitors are required at the ISL6411's input and output for stable operation over the entire load range and the full temperature range. Use >1µF capacitor at the input of ISL6411. The input capacitor lowers the source impedance of the input supply. Larger capacitor values and lower ESR provides better PSRR and line transient response. The input capacitor must be located at a distance of not more then 0.5 inches from the VIN pins of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used as an input capacitor.

The output capacitor must meet the requirements of minimum amount of capacitance and ESR for all three

LDO's. The ISL6411 is specifically designed to work with small ceramic output capacitors. The output capacitor's ESR affects stability and output noise. Use an output capacitor with an ESR of 50mΩ or less to insure stability and optimum transient response. For stable operation, a ceramic capacitor whose value is minimum 3.3µF is recommended for Vout1 for 300mA output current and 2.2µF is recommended for Vout2 and Vout3 each at 200mA load current. There is no upper limit to the output capacitor value. Larger capacitor can reduce noise and improve load transient response, stability and PSRR. The output capacitor should be located very close to Vout pins to minimize impact of PC board inductances and should be returned to a clean analog ground.

Input-Output (Dropout) Voltage

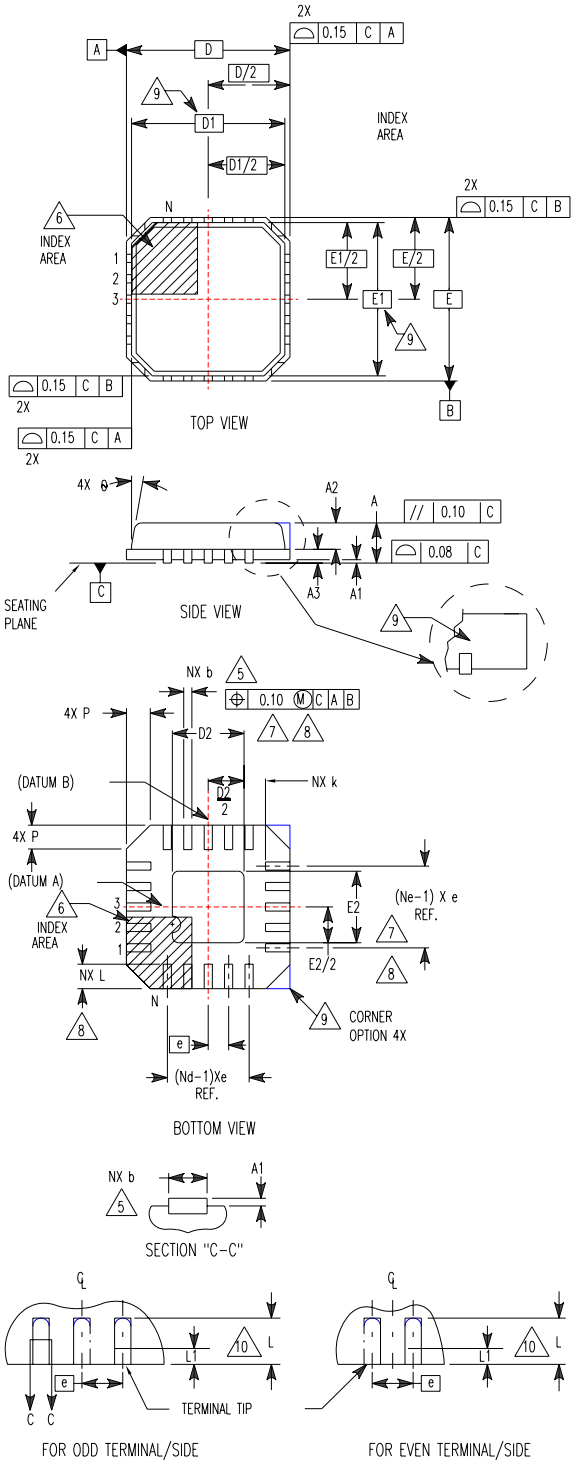
A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the ISL6411 uses a P-channel MOSFET pass transistor, its dropout voltage is a function of $R_{DS(ON)}$ (typically 0.5) multiplied by the load current.

Noise, PSSR and Transient Response

The ISL6411 is designed to operate with low dropout voltages and low quiescent current while still maintaining good noise, transient response, and AC rejection. When operating from noisy sources, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output bypass capacitors and through passive filtering techniques.

The ISL6411 load transient response graph is presented in application note An1036. Increasing the output capacitor value and decreasing the ESR attenuates the overshoot.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.