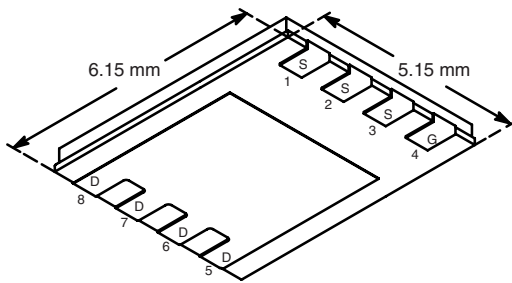




N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
100	0.0235 at V _{GS} = 10 V	27.5	7.7 nC
	0.0245 at V _{GS} = 7.5 V	27	
	0.0315 at V _{GS} = 4.5 V	24	

PowerPAK[®] SO-8

Bottom View

Ordering Information: Si7456CDP-T1-GE3 (Lead (Pb)-free and Halogen-free)

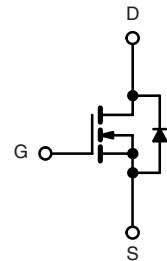
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
 FREE

APPLICATIONS

- DC/DC Primary Side Switch
- Telecom/Server 48 V, Full/Half-Bridge dc-to-dc
- Industrial



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	100	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	27.5
		T _C = 70 °C	22
		T _A = 25 °C	10.3 ^{b, c}
		T _A = 70 °C	8.2 ^{b, c}
Pulsed Drain Current	I _{DM}	50	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	4.5 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	15	mJ
Single Pulse Avalanche Energy	E _{AS}	11.2	
Maximum Power Dissipation	P _D	T _C = 25 °C	35.7
		T _C = 70 °C	22.8
		T _A = 25 °C	5.0 ^{b, c}
		T _A = 70 °C	3.2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	2.9	3.5	

Notes:

a. Based on T_C = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 70 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		47		mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.4			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.2		2.8	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA	
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	30			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.0195	0.0235	Ω	
		$V_{GS} = 7.5\text{ V}$, $I_D = 9\text{ A}$		0.0204	0.0245		
		$V_{GS} = 4.5\text{ V}$, $I_D = 8\text{ A}$		0.026	0.0315		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 10\text{ A}$		25		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		730		pF	
Output Capacitance	C_{oss}			425			
Reverse Transfer Capacitance	C_{rss}			30			
Total Gate Charge	Q_g	$V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		15	23	nC	
		$V_{DS} = 50\text{ V}$, $V_{GS} = 7.5\text{ V}$, $I_D = 10\text{ A}$		11.6	18		
Gate-Source Charge	Q_{gs}	$V_{DS} = 50\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 10\text{ A}$		7.7	12		
			Gate-Drain Charge	Q_{gd}			2.0
					3.7		
Gate Resistance	R_g		$f = 1\text{ MHz}$	1	5	10	Ω
Turn-On Delay Time	$t_{d(on)}$		$V_{DD} = 50\text{ V}$, $R_L = 5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		9	18	ns
Rise Time	t_r			13	26		
Turn-Off Delay Time	$t_{d(off)}$			22	44		
Fall Time	t_f			10	20		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}$, $R_L = 5\text{ }\Omega$ $I_D \cong 10\text{ A}$, $V_{GEN} = 7.5\text{ V}$, $R_g = 1\text{ }\Omega$		11	22		
Rise Time	t_r			14	28		
Turn-Off Delay Time	$t_{d(off)}$			20	40		
Fall Time	t_f			9	18		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			25	A	
Pulse Diode Forward Current ^a	I_{SM}				50		
Body Diode Voltage	V_{SD}	$I_S = 4\text{ A}$		0.79	1.1	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$		34	68	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			32	64	nC	
Reverse Recovery Fall Time	t_a			16		ns	
Reverse Recovery Rise Time	t_b			18			

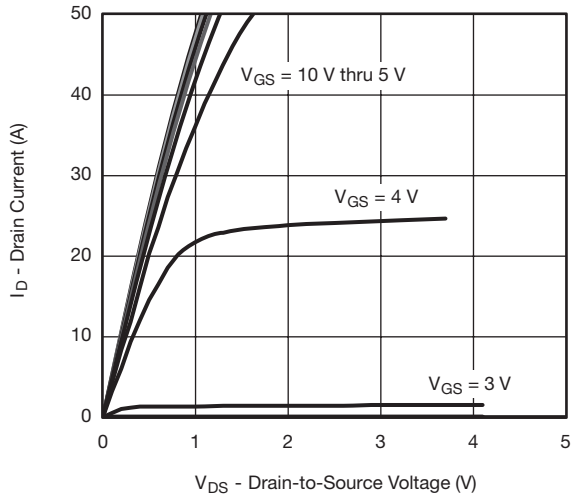
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

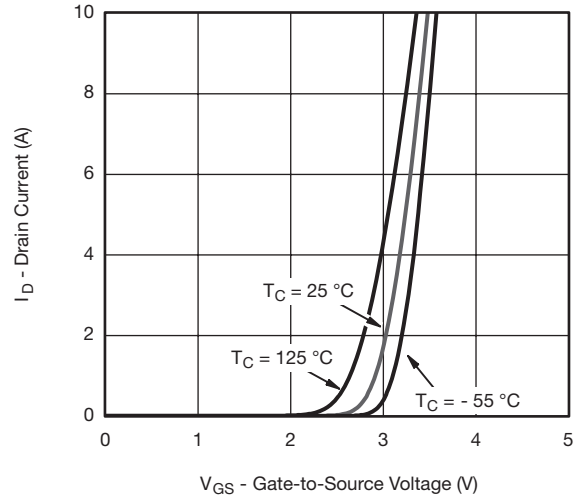
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



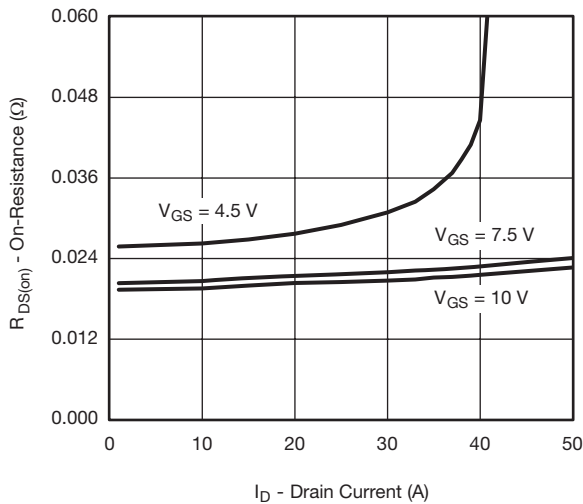
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



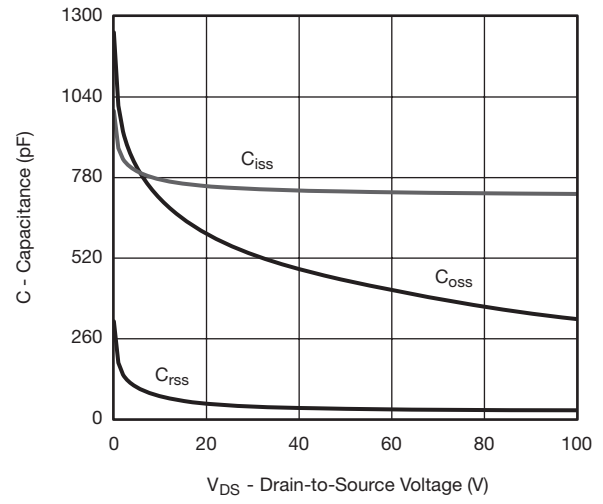
Output Characteristics



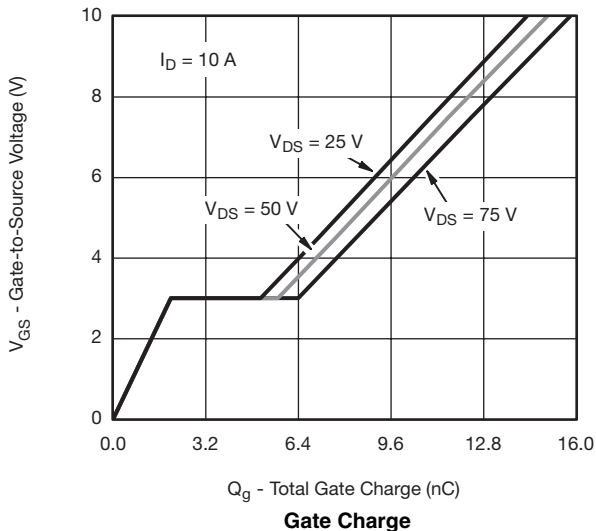
Transfer Characteristics



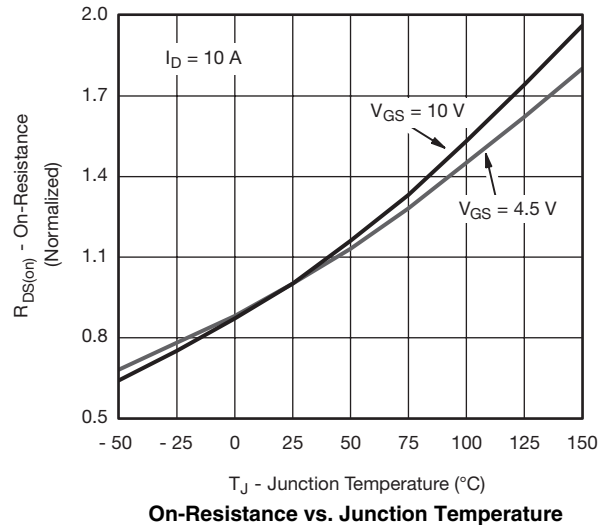
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

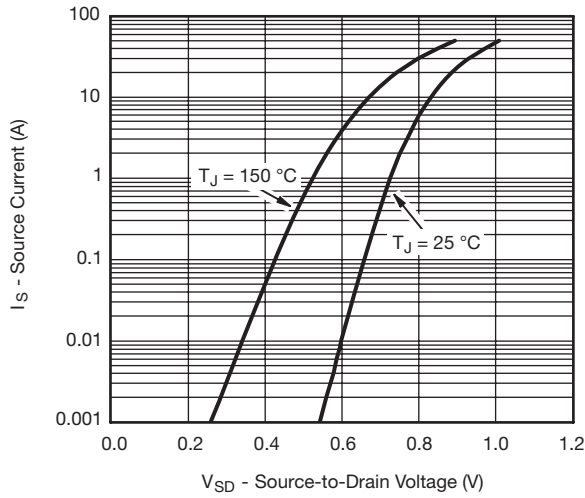


Gate Charge

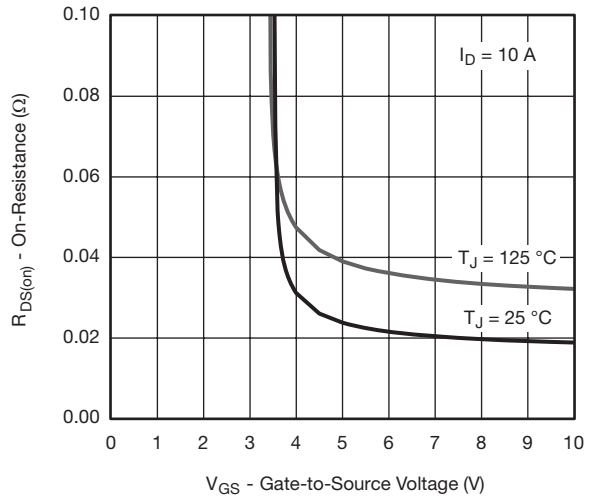


On-Resistance vs. Junction Temperature

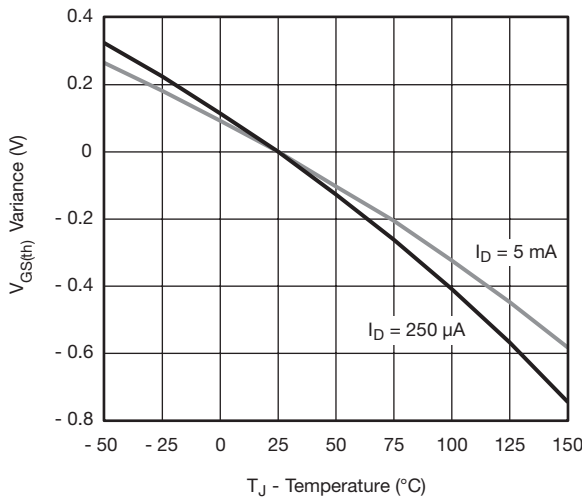
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



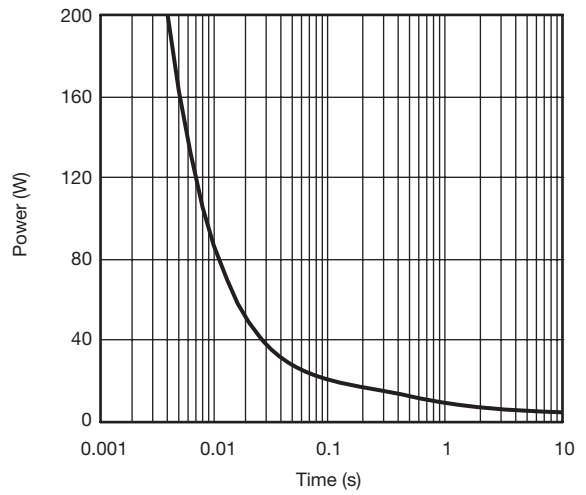
Source-Drain Diode Forward Voltage



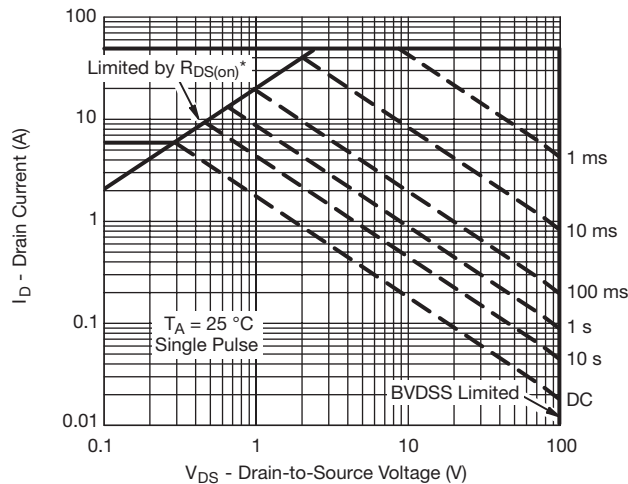
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

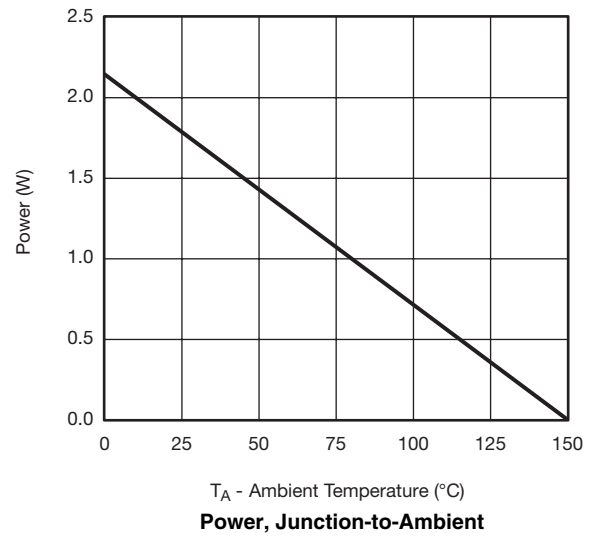
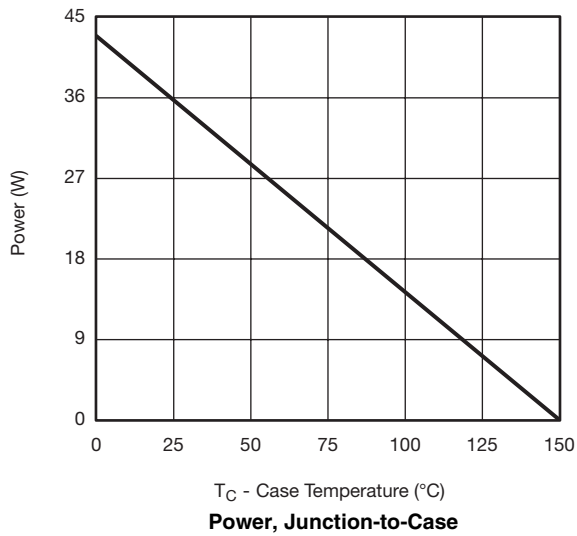
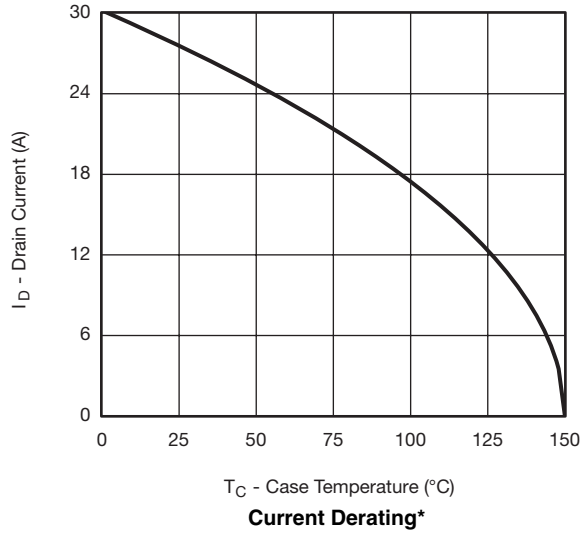


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



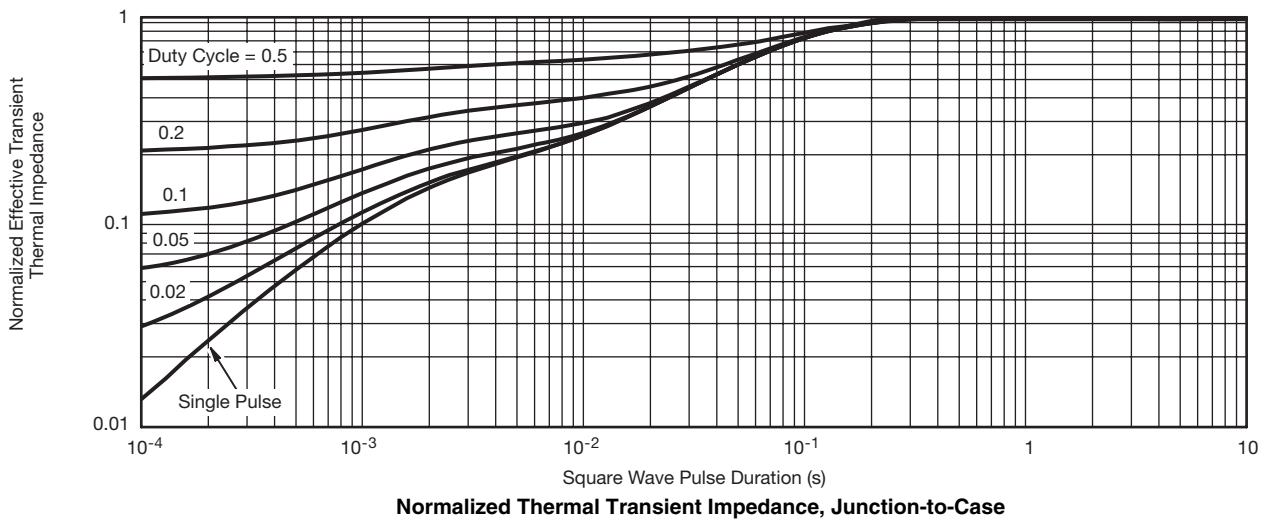
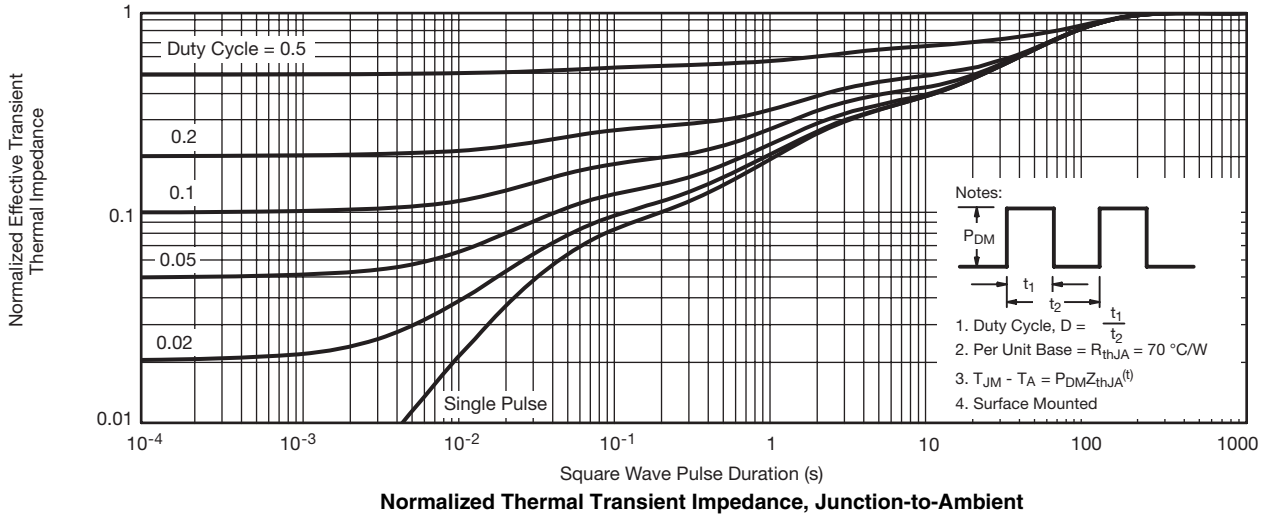
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

Si7456CDP

Vishay Siliconix



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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