

# DDR4 SDRAM VLP MiniRDIMM

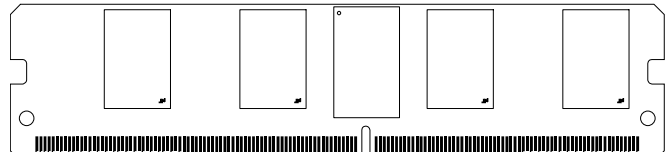
## MTA9ADF1G72PKIZ – 8GB

### Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, very low profile registered dual in-line mini memory module (VLP MiniRDIMM)
- Fast data transfer rate: PC4-2666, PC4-3200
- 8GB (1 Gig x 72)
- $V_{DD} = 1.20V$  (NOM)
- $V_{PP} = 2.5V$  (NOM)
- $V_{DDSPD} = 2.5V$  (NOM)
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die  $V_{REFDQ}$  generation and calibration
- Single-rank
- On-board I<sup>2</sup>C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

**Figure 1: 288-Pin VLP MiniRDIMM (MO-314, R/C-ZZ)**

Module Height: 18.75mm (0.738 in)



### Options

- Operating temperature
  - Industrial ( $-40^{\circ}C \leq T_{OPER} \leq +95^{\circ}C$ )
- Package
  - 288-pin MiniDIMM (halogen-free)
- Frequency/CAS latency
  - 0.625ns @ CL = 22 (DDR4-3200)
  - 0.75ns @ CL = 19 (DDR4-2666)

### Marking

- I
- Z
- -3G2
- -2G6

**Table 1: Key Timing Parameters**

Speed Grade	PC4-	Data Rate (MT/s)														t <sub>RCD</sub> (ns)	t <sub>RP</sub> (ns)	t <sub>RC</sub> (ns)
		CL =																
		24	22	21	20	19	18	17	16	15	14	13	12	11	10 \ 9			
-3G2	3200	3200, 2933	3200, 2933	–	2666	2666	2400	2400	2133	2133	1866	1866	1600	1600	1333 \ –	13.75	13.75	45.75
-2G9	2933	–	2933	2933	2666	2666	2400	2400	2133	2133	1866	1866	1600	1600	1333 \ –	14.32	14.32	46.32
-2G6	2666	–	–	–	2666	2666	2400	2400	2133	2133	1866	1866	1600	1600	1333 \ –	14.16	14.16	46.16

**Table 1: Key Timing Parameters (Continued)**

Speed Grade	PC4-	Data Rate (MT/s)														tRCD (ns)	tRP (ns)	tRC (ns)
		CL =																
		24	22	21	20	19	18	17	16	15	14	13	12	11	10 \ 9			
-2G3	2400	-	-	-	-	-	2400	2400	2133	2133	1866	1866	1600	1600	1333 \ -	14.16	14.16	46.16
-2G1	2133	-	-	-	-	-	-	-	2133	2133	1866	1866	1600	1600	1333 \ 1333	13.5	13.5	46.5

**Table 2: Addressing**

Parameter	8GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (1 Gig x 8), 16 banks
Module rank address	1 CS0_n

**Table 3: Part Numbers and Timing Parameters – 8GB Modules**

Base device: MT40A1G8,<sup>1</sup> 8Gb DDR4 SDRAM

Part Number <sup>2</sup>	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-tRCD-tRP)
MTA9ADF1G72PKIZ-3G2__	8GB	1 Gig x 72	25.6 GB/s	0.625/3200 MT/s	22-22-22
MTA9ADF1G72PKIZ-2G6__	8GB	1 Gig x 72	21.3 GB/s	0.75ns/2666 MT/s	19-19-19

- Notes:
1. The data sheet for the base device can be found on [micron.com](http://micron.com).
  2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA9ADF1G72PKIZ-3G2E1.

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## Pin Assignments

The pin assignment table below is a comprehensive list of all possible pin assignments for DDR4 MiniRDIMM modules. See the Functional Block Diagram for pins specific to this module.

**Table 4: Pin Assignments**

288-Pin DDR4 MiniRDIMM Front								288-Pin DDR4 MiniRDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NC	37	V <sub>SS</sub>	73	A1	109	DQ41	145	V <sub>REFCA</sub>	181	V <sub>SS</sub>	217	RFU	253	DQ45
2	NC	38	DQ24	74	V <sub>DD</sub>	110	V <sub>SS</sub>	146	NC	182	DQ28	218	V <sub>DD</sub>	254	V <sub>SS</sub>
3	RFU	39	V <sub>SS</sub>	75	CK0_t	111	DQS5_c	147	RFU	183	V <sub>SS</sub>	219	CK1_t	255	DQS14_t/ DM5_n
4	V <sub>SS</sub>	40	DQ25	76	CK0_c	112	DQS5_t	148	V <sub>SS</sub>	184	DQ29	220	CK1_c	256	DQS14_c
5	DQ0	41	V <sub>SS</sub>	77	V <sub>DD</sub>	113	V <sub>SS</sub>	149	DQ4	185	V <sub>SS</sub>	221	V <sub>DD</sub>	257	V <sub>SS</sub>
6	V <sub>SS</sub>	42	DQS3_c	78	RFU	114	DQ42	150	V <sub>SS</sub>	186	DQS12_t/ DM3_n	222	RFU	258	DQ46
7	DQ1	43	DQS3_t	79	V <sub>TT</sub>	115	V <sub>SS</sub>	151	DQ5	187	DQS12_c	223	V <sub>TT</sub>	259	V <sub>SS</sub>
8	V <sub>SS</sub>	44	V <sub>SS</sub>	80	EVENT_n	116	DQ43	152	V <sub>SS</sub>	188	V <sub>SS</sub>	224	PARITY	260	DQ47
9	DQS0_c	45	DQ26	81	V <sub>DD</sub>	117	V <sub>SS</sub>	153	DQS9_t/ DM0_n	189	DQ30	225	V <sub>DD</sub>	261	V <sub>SS</sub>
10	DQS0_t	46	V <sub>SS</sub>	82	A0	118	DQ48	154	DQS9_c	190	V <sub>SS</sub>	226	BA1	262	DQ52
11	V <sub>SS</sub>	47	DQ27	83	BA0	119	V <sub>SS</sub>	155	V <sub>SS</sub>	191	DQ31	227	A10/ AP	263	V <sub>SS</sub>
12	DQ2	48	V <sub>SS</sub>	84	V <sub>DD</sub>	120	DQ49	156	DQ6	192	V <sub>SS</sub>	228	V <sub>DD</sub>	264	DQ53
13	V <sub>SS</sub>	49	CB0	85	RAS_n/ A16	121	V <sub>SS</sub>	157	V <sub>SS</sub>	193	CB4	229	WE_n/ A14	265	V <sub>SS</sub>
14	DQ3	50	V <sub>SS</sub>	86	CS0_n	122	DQS6_c	158	DQ7	194	V <sub>SS</sub>	230	CAS_n/ A15	266	DQS15_t/ DM6_n
15	V <sub>SS</sub>	51	CB1	87	V <sub>DD</sub>	123	DQS6_t	159	V <sub>SS</sub>	195	CB5	231	V <sub>DD</sub>	267	DQS15_c
16	DQ8	52	V <sub>SS</sub>	88	ODT0	124	V <sub>SS</sub>	160	DQ12	196	V <sub>SS</sub>	232	A13	268	V <sub>SS</sub>
17	V <sub>SS</sub>	53	DQS8_c	89	CS1_n/ NC	125	DQ50	161	V <sub>SS</sub>	197	DQS17_t/ DM8_n	233	A17/ NC	269	DQ54
18	DQ9	54	DQS8_t	90	V <sub>DD</sub>	126	V <sub>SS</sub>	162	DQ13	198	DQS17_c	234	V <sub>DD</sub>	270	V <sub>SS</sub>
19	V <sub>SS</sub>	55	V <sub>SS</sub>	91	ODT1/ NC	127	DQ51	163	V <sub>SS</sub>	199	V <sub>SS</sub>	235	NC/CS3_n/ C1	271	DQ55
20	DQS1_c	56	CB2	92	CS2_n/CO/ NC	128	V <sub>SS</sub>	164	DQS10_t/ DM1_n	200	CB6	236	NC/ C2	272	V <sub>SS</sub>
21	DQS1_t	57	V <sub>SS</sub>	93	V <sub>DD</sub>	129	DQ56	165	DQS10_c	201	V <sub>SS</sub>	237	V <sub>DD</sub>	273	DQ60
22	V <sub>SS</sub>	58	CB3	94	RFU	130	V <sub>SS</sub>	166	V <sub>SS</sub>	202	CB7	238	RFU	274	V <sub>SS</sub>
23	DQ10	59	V <sub>SS</sub>	95	V <sub>SS</sub>	131	DQ57	167	DQ14	203	V <sub>SS</sub>	239	V <sub>SS</sub>	275	DQ61
24	V <sub>SS</sub>	60	ALERT_n	96	DQ32	132	V <sub>SS</sub>	168	V <sub>SS</sub>	204	RESET_n	240	DQ36	276	V <sub>SS</sub>
25	DQ11	61	CKE0	97	V <sub>SS</sub>	133	DQS7_c	169	DQ15	205	RFU	241	V <sub>SS</sub>	277	DQS16_t/ DM7_n
26	V <sub>SS</sub>	62	V <sub>DD</sub>	98	DQ33	134	DQS7_t	170	V <sub>SS</sub>	206	V <sub>DD</sub>	242	DQ37	278	DQS16_c
27	DQ16	63	ACT_n	99	V <sub>SS</sub>	135	V <sub>SS</sub>	171	DQ20	207	CKE1/ NC	243	V <sub>SS</sub>	279	V <sub>SS</sub>
28	V <sub>SS</sub>	64	BG0	100	DQS4_c	136	DQ58	172	V <sub>SS</sub>	208	BG1	244	DQS13_t/ DM4_n	280	DQ62
29	DQ17	65	V <sub>DD</sub>	101	DQS4_t	137	V <sub>SS</sub>	173	DQ21	209	V <sub>DD</sub>	245	DQS13_c	281	V <sub>SS</sub>



## 8GB (x72, ECC, SR) 288-Pin DDR4 VLP MiniRDIMM Pin Assignments

**Table 4: Pin Assignments (Continued)**

288-Pin DDR4 MiniRDIMM Front								288-Pin DDR4 MiniRDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
30	V <sub>SS</sub>	66	A12/BC_n	102	V <sub>SS</sub>	138	DQ59	174	V <sub>SS</sub>	210	A11	246	V <sub>SS</sub>	282	DQ63
31	DQS2_c	67	A9	103	DQ34	139	V <sub>SS</sub>	175	DQS11_t/ DM2_n	211	A7	247	DQ38	283	V <sub>SS</sub>
32	DQS2_t	68	V <sub>DD</sub>	104	V <sub>SS</sub>	140	SA0	176	DQS11_c	212	V <sub>DD</sub>	248	V <sub>SS</sub>	284	SA1
33	V <sub>SS</sub>	69	A8	105	DQ35	141	V <sub>DDSPD</sub>	177	V <sub>SS</sub>	213	A5	249	DQ39	285	SA2
34	DQ18	70	A6	106	V <sub>SS</sub>	142	SDA	178	DQ22	214	A4	250	V <sub>SS</sub>	286	SCL
35	V <sub>SS</sub>	71	V <sub>DD</sub>	107	DQ40	143	V <sub>PP</sub>	179	V <sub>SS</sub>	215	V <sub>DD</sub>	251	DQ44	287	V <sub>PP</sub>
36	DQ19	72	A3	108	V <sub>SS</sub>	144	V <sub>PP</sub>	180	DQ23	216	A2	252	V <sub>SS</sub>	288	V <sub>PP</sub>

## Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 modules. All pins listed may not be supported on this module. See Functional Block Diagram for pins specific to this module.

**Table 5: Pin Descriptions**

Symbol	Type	Description
Ax	Input	<b>Address inputs:</b> Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	<b>Auto precharge:</b> A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	<b>Burst chop:</b> A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	<b>Command input:</b> ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	<b>Bank address inputs:</b> Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	<b>Bank group address inputs:</b> Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	<b>Chip ID:</b> These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	<b>Clock:</b> Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	<b>Clock enable:</b> CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V <sub>REFCA</sub> has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	<b>Chip select:</b> All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

**Table 5: Pin Descriptions (Continued)**

Symbol	Type	Description
ODTx	Input	<b>On-die termination:</b> ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT ( $R_{TT}$ ) is applied only to each DQ, DQS <sub>t</sub> , DQS <sub>c</sub> , DM <sub>n</sub> /DBI <sub>n</sub> /TDQS <sub>t</sub> , and TDQS <sub>c</sub> signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, $R_{TT}$ is applied to each DQ, DQSU <sub>t</sub> , DQSU <sub>c</sub> , DQSL <sub>t</sub> , DQSL <sub>c</sub> , UDM <sub>n</sub> , and LDM <sub>n</sub> signal. The ODT pin will be ignored if the mode registers are programmed to disable $R_{TT}$ .
PARITY	Input	<b>Parity for command and address:</b> This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT <sub>n</sub> , RAS <sub>n</sub> /A16, CAS <sub>n</sub> /A15, WE <sub>n</sub> /A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS <sub>n</sub> LOW.
RAS <sub>n</sub> /A16 CAS <sub>n</sub> /A15 WE <sub>n</sub> /A14	Input	<b>Command inputs:</b> RAS <sub>n</sub> /A16, CAS <sub>n</sub> /A15, and WE <sub>n</sub> /A14 (along with CS <sub>n</sub> ) define the command and/or address being entered and have multiple functions. For example, for activation with ACT <sub>n</sub> LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT <sub>n</sub> HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET <sub>n</sub>	CMOS Input	<b>Active LOW asynchronous reset:</b> Reset is active when RESET <sub>n</sub> is LOW and inactive when RESET <sub>n</sub> is HIGH. RESET <sub>n</sub> must be HIGH during normal operation.
SAX	Input	<b>Serial address inputs:</b> Used to configure the temperature sensor/SPD EEPROM address range on the I <sup>2</sup> C bus.
SCL	Input	<b>Serial clock for temperature sensor/SPD EEPROM:</b> Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I <sup>2</sup> C bus.
DQx, CBx	I/O	<b>Data input/output and check bit input/output:</b> Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal $V_{REF}$ level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM <sub>n</sub> /DBI <sub>n</sub> / TDQS <sub>t</sub> (DMU <sub>n</sub> , DBIU <sub>n</sub> ), (DML <sub>n</sub> / DBIL <sub>n</sub> )	I/O	<b>Input data mask and data bus inversion:</b> DM <sub>n</sub> is an input mask signal for write data. Input data is masked when DM <sub>n</sub> is sampled LOW coincident with that input data during a write access. DM <sub>n</sub> is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI <sub>n</sub> is an input/output identifying whether to store/output the true or inverted data. If DBI <sub>n</sub> is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI <sub>n</sub> is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	<b>Serial Data:</b> Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS <sub>t</sub> DQS <sub>c</sub> DQSU <sub>t</sub> DQSU <sub>c</sub> DQSL <sub>t</sub> DQSL <sub>c</sub>	I/O	<b>Data strobe:</b> Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT <sub>n</sub>	Output	<b>Alert output:</b> Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT <sub>n</sub> goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT <sub>n</sub> goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT <sub>n</sub> pin must be connected to $V_{DD}$ on DIMMs.
EVENT <sub>n</sub>	Output	<b>Temperature event:</b> The EVENT <sub>n</sub> pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

**Table 5: Pin Descriptions (Continued)**

Symbol	Type	Description
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	<b>Termination data strobe:</b> When enabled via the mode register, the DRAM device enables the same $R_{TT}$ termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet (TDQS_t and TDQS_c are not valid for UDIMMs).
V <sub>DD</sub>	Supply	<b>Module power supply:</b> 1.2V (TYP).
V <sub>PP</sub>	Supply	<b>DRAM activating power supply:</b> 2.5V –0.125V / +0.250V.
V <sub>REFCA</sub>	Supply	Reference voltage for control, command, and address pins.
V <sub>SS</sub>	Supply	Ground.
V <sub>TT</sub>	Supply	Power supply for termination of address, command, and control V <sub>DD</sub> /2.
V <sub>DDSPD</sub>	Supply	Power supply used to power the I <sup>2</sup> C bus for SPD.
RFU	–	Reserved for future use.
NC	–	<b>No connect:</b> No internal electrical connection is present.
NF	–	<b>No function:</b> May have internal connection present, but has no function.





## DQ Map

Table 6: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	14	167	U2	0	27	47
	1	13	162		1	25	40
	2	15	169		2	26	45
	3	12	160		3	24	38
	4	10	23		4	31	191
	5	8	16		5	29	184
	6	11	25		6	30	189
	7	9	18		7	28	182
U4	0	41	109	U5	0	62	280
	1	40	107		1	61	275
	2	42	114		2	63	282
	3	43	116		3	60	273
	4	45	253		4	59	138
	5	46	258		5	56	129
	6	44	251		6	58	136
	7	47	260		7	57	131
U7	0	48	118	U8	0	36	240
	1	50	125		1	38	247
	2	49	120		2	37	242
	3	51	127		3	39	249
	4	52	262		4	32	96
	5	55	271		5	35	105
	6	53	264		6	33	98
	7	54	269		7	34	103
U9	0	CB4	193	U10	0	21	173
	1	CB6	200		1	23	180
	2	CB5	195		2	20	171
	3	CB7	202		3	22	178
	4	CB0	49		4	16	27
	5	CB2	55		5	19	36
	6	CB1	51		6	17	29
	7	CB3	58		7	18	34

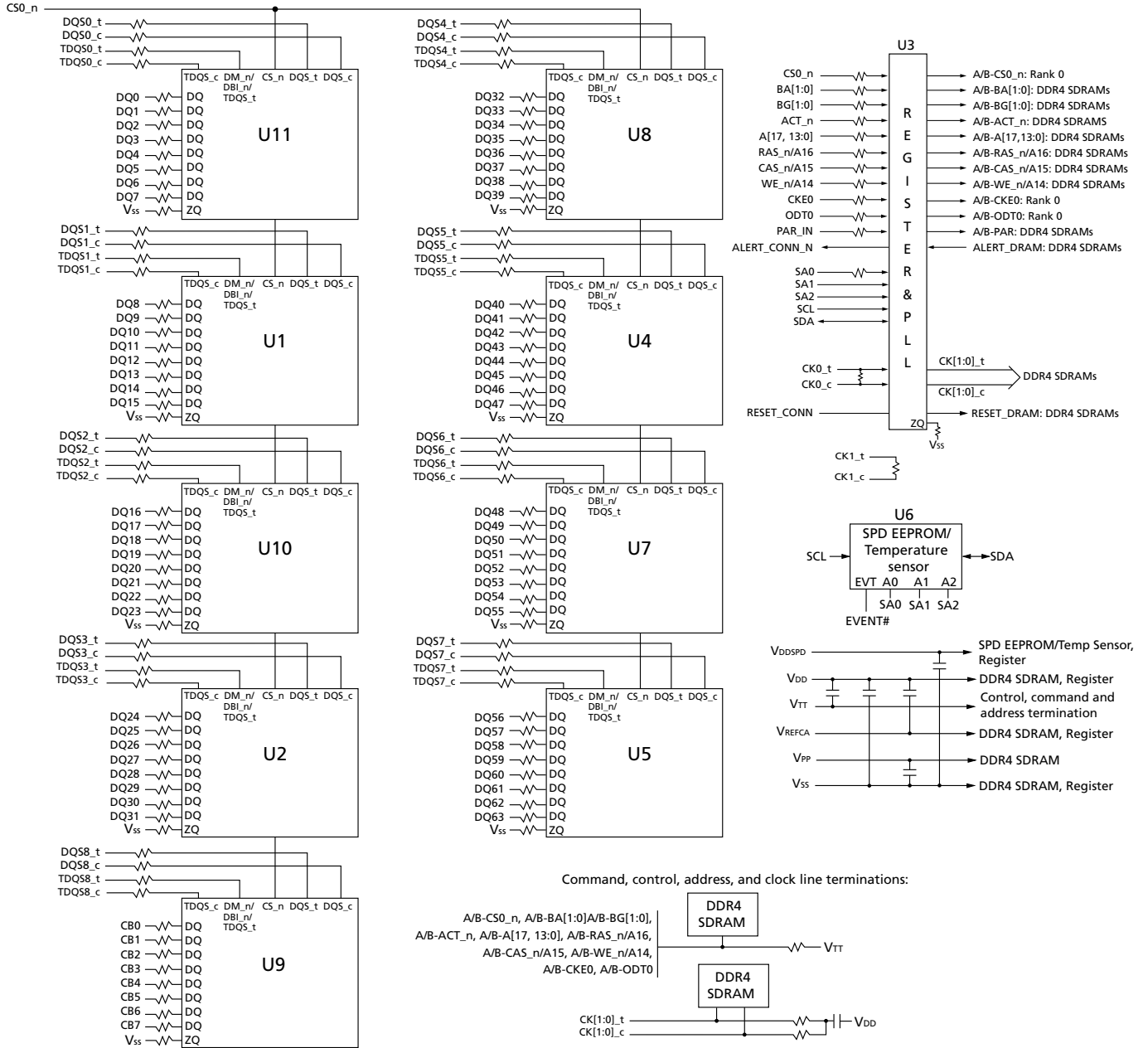


Table 6: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	0	5				
	1	3	14				
	2	1	7				
	3	2	12				
	4	4	149				
	5	7	158				
	6	5	151				
	7	6	156				

## Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external  $240\Omega \pm 1\%$  resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

## General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with two or four internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of 16 banks. 16-bit-wide DDR4 SDRAM devices have two internal bank groups consisting of four memory banks each, providing a total of eight banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an  $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single  $8n$ -bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS\_t and DQS\_c to capture data and CK\_t and CK\_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

## Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

## Module Manufacturing Location

Micron Technology manufactures modules at sites world-wide. Customers may receive modules from any of the following manufacturing locations:

**Table 7: DRAM Module Manufacturing Locations**

Manufacturing Site Location	Country of Origin Specified on Label
Boise, USA	USA
Aguadilla, Puerto Rico	Puerto Rico
Xian, China	China
Singapore	Singapore



## Address Mapping to DRAM

### Address Mirroring

To achieve optimum routing of the address bus on DDR4 multi rank modules, the address bus will be wired as shown in the table below, or mirrored. For quad rank modules, ranks 1 and 3 are mirrored and ranks 0 and 2 are non-mirrored. Highlighted address pins have no secondary functions allowing for normal operation when cross-wired. Data is still read from the same address it was written. However, Load Mode operations require a specific address. This requires the controller to accommodate for a rank that is "mirrored." Systems may reference DDR4 SPD to determine if the module has mirroring implemented or not. See the JEDEC DDR4 SPD specification for more details.

**Table 8: Address Mirroring**

Edge Connector Pin	DRAM Pin, Non-mirrored	DRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
A10	A10	A10
A11	A11	A13
A13	A13	A11
A12	A12	A12
A14	A14	A14
A15	A15	A15
A16	A16	A16
A17	A17	A17
BA0	BA0	BA1
BA1	BA1	BA0
BG0	BG0	BG1
BG1	BG1	BG0

## Registering Clock Driver Operation

Registered DDR4 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC DDR4 RCD specification.

To reduce the electrical load on the host memory controller's command, address, and control bus, Micron's RDIMMs utilize a DDR4 registering clock driver (RCD). The RCD presents a single load to the controller while redriving signals to the DDR4 SDRAM devices, which helps enable higher densities and increase signal integrity. The RCD also provides a low-jitter, low-skew PLL that redistributes a differential clock pair to multiple differential pairs of clock outputs.

### Control Words

The RCD device(s) used on DDR4 RDIMMs, LRDIMMs, and NVDIMMs contain configuration registers known as control words, which the host uses to configure the RCD based on criteria determined by the module design. Control words can be set by the host controller through either the DRAM address and control bus or the I<sup>2</sup>C bus interface. The RCD I<sup>2</sup>C bus interface resides on the same I<sup>2</sup>C bus interface as the module temperature sensor and EEPROM.

### Parity Operations

The RCD includes a parity-checking function that can be enabled or disabled in control word RC0E. The RCD receives a parity bit at the DPAR input from the memory controller and compares it with the data received on the qualified command and address inputs; it indicates on its open-drain ALERT<sub>n</sub> pin whether a parity error has occurred. If parity checking is enabled, the RCD forwards commands to the SDRAM when no parity error has occurred. If the parity error function is disabled, the RCD forwards sampled commands to the SDRAM regardless of whether a parity error has occurred. Parity is also checked during control word WRITE operations unless parity checking is disabled.

### Rank Addressing

The chip select pins (CS<sub>n</sub>) on Micron's modules are used to select a specific rank of DRAM. The RDIMM is capable of selecting ranks in one of three different operating modes, dependant on setting DA[1:0] bits in the DIMM configuration control word located within the RCD. Direct DualCS mode is utilized for single- or dual-rank modules. For quad-rank modules, either direct or encoded QuadCS mode is used.

## Temperature Sensor with SPD EEPROM Operation

### Thermal Sensor Operations

The integrated thermal sensor continuously monitors the temperature of the module PCB directly below the device and updates the temperature data register. Temperature data may be read from the bus host at any time, which provides the host real-time feedback of the module's temperature. Multiple programmable and read-only temperature registers can be used to create a custom temperature-sensing solution based on system requirements and JEDEC JC-42.2.

### EVENT\_n Pin

The temperature sensor also adds the EVENT\_n pin (open-drain), which requires a pull-up to  $V_{DDSPD}$ . EVENT\_n is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration registers. EVENT\_n is not used by the serial presence-detect (SPD) EEPROM.

EVENT\_n has three defined modes of operation: interrupt, comparator, and TCRT. In interrupt mode, the EVENT\_n pin remains asserted until it is released by writing a 1 to the clear event bit in the status register. In comparator mode, the EVENT\_n pin clears itself when the error condition is removed. Comparator mode is always used when the temperature is compared against the TCRT limit. In TCRT only mode, the EVENT\_n pin is only asserted if the measured temperature exceeds the TCRT limit; it then remains asserted until the temperature drops below the TCRT limit minus the TCRT hysteresis.

### SPD EEPROM Operation

DDR4 SDRAM modules incorporate SPD. The SPD data is stored in a 512-byte, JEDEC JC-42.4-compliant EEPROM that is segregated into four 128-byte, write-protectable blocks. The SPD content is aligned with these blocks as shown in the table below.

Block	Range		Description
0	0–127	000h–07Fh	Configuration and DRAM parameters
1	128–255	080h–0FFh	Module parameters
2	256–319	100h–13Fh	Reserved (all bytes coded as 00h)
	320–383	140h–17Fh	Manufacturing information
3	384–511	180h–1FFh	End-user programmable

The first 384 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR4 SDRAM Modules." The remaining 128 bytes of storage are available for use by the customer.

The EEPROM resides on a two-wire I<sup>2</sup>C serial interface and is not integrated with the memory bus in any manner. It operates as a slave device in the I<sup>2</sup>C bus protocol, with all operations synchronized by the serial clock. Transfer rates of up to 1 MHz are achievable at 2.5V (NOM).

Micron implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0 to 383) from being inadvertently programmed or corrupted. The upper 128 bytes remain available for customer use and are unprotected.

## Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 9: Absolute Maximum Ratings**

Symbol	Parameter	Min	Max	Units	Notes
V <sub>DD</sub>	V <sub>DD</sub> supply voltage relative to V <sub>SS</sub>	-0.4	1.5	V	1
V <sub>DDQ</sub>	V <sub>DDQ</sub> supply voltage relative to V <sub>SS</sub>	-0.4	1.5	V	1
V <sub>PP</sub>	Voltage on V <sub>PP</sub> pin relative to V <sub>SS</sub>	-0.4	3.0	V	2
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.4	1.5	V	

**Table 10: Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units	Notes
V <sub>DD</sub>	V <sub>DD</sub> supply voltage	1.14	1.20	1.26	V	1
V <sub>PP</sub>	DRAM activating power supply	2.375	2.5	2.75	V	2
V <sub>REFCA(DC)</sub>	Input reference voltage – command/address bus	0.49 × V <sub>DD</sub>	0.5 × V <sub>DD</sub>	0.51 × V <sub>DD</sub>	V	3
I <sub>VTT</sub>	Termination reference current from V <sub>TT</sub>	-750	-	750	mA	
V <sub>TT</sub>	Termination reference voltage (DC) – command/address bus	0.49 × V <sub>DD</sub> - 20mV	0.5 × V <sub>DD</sub>	0.51 × V <sub>DD</sub> + 20mV	V	4
I <sub>IN</sub>	Input leakage current; any input excluding ZQ; 0V < V <sub>IN</sub> < 1.1V	-2	-	2	μA	5
I <sub>ZQ</sub>	Input leakage current; ZQ	-50	-	10	μA	6, 7
I <sub>OZpd</sub>	Output leakage current; V <sub>OUT</sub> = V <sub>DD</sub> ; DQ is disabled	-	-	10	μA	
I <sub>OZpu</sub>	Output leakage current; V <sub>OUT</sub> = V <sub>SS</sub> ; DQ is disabled; ODT is disabled with ODT input HIGH	-50	-	-	μA	
I <sub>VREFCA</sub>	V <sub>REFCA</sub> leakage; V <sub>REFCA</sub> = V <sub>DD</sub> /2 (after DRAM is initialized)	-2	-	2	μA	7

- Notes:
1. V<sub>DDQ</sub> balls on DRAM are tied to V<sub>DD</sub>.
  2. V<sub>PP</sub> must be greater than or equal to V<sub>DD</sub> at all times.
  3. V<sub>REFCA</sub> must not be greater than 0.6 × V<sub>DD</sub>. When V<sub>DD</sub> is less than 500mV, V<sub>REF</sub> may be less than or equal to 300mV.
  4. V<sub>TT</sub> termination voltages in excess of specification limit adversely affect command and address signals' voltage margins and reduce timing margins.
  5. Command and address inputs are terminated to V<sub>DD</sub>/2 in the registering clock driver. Input current is dependent on termination resistance set in the registering clock driver.
  6. Tied to ground. Not connected to edge connector.
  7. Multiply by number of DRAM die on module.





Table 11: Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T <sub>C</sub>	Industrial operating case temperature	-40 to 85	°C	1, 2, 3
		>85 to 95	°C	1, 2, 3, 4
T <sub>OPER</sub>	Normal operating temperature range	0 to 85	°C	5, 6, 7
	Extended temperature operating range (optional)	>85 to 95	°C	5, 7
T <sub>STG</sub>	Non-operating storage temperature	-55 to 100	°C	8
RH <sub>STG</sub>	Non-operating storage relative humidity (noncondensing)	5 to 95	%	
N/A	Change rate of storage temperature	20	°C/hour	

- Notes:
1. Maximum operating case temperature; T<sub>C</sub> is measured in the center of the package.
  2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T<sub>C</sub> during operation.
  3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T<sub>C</sub> during operation.
  4. If T<sub>C</sub> exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
  5. The refresh rate must double when 85°C < T<sub>OPER</sub> ≤ 95°C.
  6. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to 85°C under all operating conditions for the commercial offering; The industrial temperature offering allows the case temperature to go below 0°C to -40°C.
  7. For additional information, refer to technical note TN-00-08: "Thermal Applications" available at [micron.com](http://micron.com).
  8. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.



## DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available at [micron.com](http://micron.com). Module speed grades correlate with component speed grades, as shown below.

**Table 12: Module and Component Speed Grades**

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-3G2	-062E
-2G9	-068
-2G6	-075
-2G3	-083
-2G1	-093E

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the edge connector of the module, not at the DRAM. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

## I<sub>DD</sub> Specifications

**Table 13: DDR4 I<sub>DD</sub> Specifications and Conditions – 8GB (Die Revision B)**

Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) component data sheet

Parameter	Symbol	2666	Units
One bank ACTIVATE-PRECHARGE current	I <sub>DD0</sub>	459	mA
One bank ACTIVATE-PRECHARGE, word line boost, I <sub>pp</sub> current	I <sub>PP0</sub>	27	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>DD1</sub>	567	mA
Precharge standby current	I <sub>DD2N</sub>	315	mA
Precharge standby ODT current	I <sub>DD2NT</sub>	450	mA
Precharge power-down current	I <sub>DD2P</sub>	225	mA
Precharge quiet standby current	I <sub>DD2Q</sub>	270	mA
Active standby current	I <sub>DD3N</sub>	414	mA
Active standby I <sub>pp</sub> current	I <sub>PP3N</sub>	27	mA
Active power-down current	I <sub>DD3P</sub>	351	mA
Burst read current	I <sub>DD4R</sub>	1314	mA
Burst write current	I <sub>DD4W</sub>	1188	mA
Burst refresh current (1 x REF)	I <sub>DD5R</sub>	504	mA
Burst refresh I <sub>pp</sub> current (1 x REF)	I <sub>PP5R</sub>	45	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I <sub>DD6N</sub>	270	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I <sub>DD6E</sub>	315	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I <sub>DD6R</sub>	180	mA
Auto self refresh current (25°C)	I <sub>DD6A</sub>	77.4	mA
Auto self refresh current (45°C)	I <sub>DD6A</sub>	180	mA
Auto self refresh current (75°C)	I <sub>DD6A</sub>	270	mA
Auto self refresh I <sub>pp</sub> current	I <sub>PP6X</sub>	45	mA
Bank interleave read current	I <sub>DD7</sub>	1620	mA
Bank interleave read I <sub>pp</sub> current	I <sub>PP7</sub>	135	mA
Maximum power-down current	I <sub>DD8</sub>	225	mA



**Table 14: DDR4 I<sub>DD</sub> Specifications and Conditions – 8GB (Die Revision E)**

Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) component data sheet

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I <sub>DD0</sub>	423	mA
One bank ACTIVATE-PRECHARGE, word line boost, I <sub>pp</sub> current	I <sub>PP0</sub>	27	mA
One bank ACTIVATE-READ-PRECHARGE current	I <sub>DD1</sub>	567	mA
Precharge standby current	I <sub>DD2N</sub>	297	mA
Precharge standby ODT current	I <sub>DD2NT</sub>	396	mA
Precharge power-down current	I <sub>DD2P</sub>	198	mA
Precharge quiet standby current	I <sub>DD2Q</sub>	234	mA
Active standby current	I <sub>DD3N</sub>	387	mA
Active standby I <sub>pp</sub> current	I <sub>PP3N</sub>	27	mA
Active power-down current	I <sub>DD3P</sub>	297	mA
Burst read current	I <sub>DD4R</sub>	1602	mA
Burst write current	I <sub>DD4W</sub>	1350	mA
Burst refresh current (1 x REF)	I <sub>DD5R</sub>	450	mA
Burst refresh I <sub>pp</sub> current (1 x REF)	I <sub>PP5R</sub>	45	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I <sub>DD6N</sub>	306	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I <sub>DD6E</sub>	522	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I <sub>DD6R</sub>	189	mA
Auto self refresh current (25°C)	I <sub>DD6A</sub>	77.4	mA
Auto self refresh current (45°C)	I <sub>DD6A</sub>	189	mA
Auto self refresh current (75°C)	I <sub>DD6A</sub>	279	mA
Auto self refresh I <sub>pp</sub> current	I <sub>PP6X</sub>	45	mA
Bank interleave read current	I <sub>DD7</sub>	1710	mA
Bank interleave read I <sub>pp</sub> current	I <sub>PP7</sub>	117	mA
Maximum power-down current	I <sub>DD8</sub>	162	mA



## Registering Clock Driver Specifications

**Table 15: Registering Clock Driver Electrical Characteristics**

DDR4 RCD01 devices or equivalent

Parameter	Symbol	Pins	Min	Nom	Max	Units
DC supply voltage	$V_{DD}$	–	1.14	1.2	1.26	V
DC reference voltage	$V_{REF}$	$V_{REFCA}$	$0.49 \times V_{DD}$	$0.5 \times V_{DD}$	$0.51 \times V_{DD}$	V
DC termination voltage	$V_{TT}$	–	$V_{REF} - 40mV$	$V_{REF}$	$V_{REF} + 40mV$	V
High-level input voltage	$V_{IH, CMOS}$	DRST_n	$0.65 \times V_{DD}$	–	$V_{DD}$	V
Low-level input voltage	$V_{IL, CMOS}$		0	–	$0.35 \times V_{DD}$	V
DRST_n pulse width	$t_{IN-IT\_Power\_stable}$	–	1.0	–	–	$\mu s$
AC high-level output voltage	$V_{OH(AC)}$	All outputs except ALERT_n	$V_{TT} + (0.15 \times V_{DD})$	–	–	V
AC low-level output voltage	$V_{OL(AC)}$		–	–	$V_{TT} + (0.15 \times V_{DD})$	V
AC differential output high measurement level (for output slew rate)	$V_{OHdiff(AC)}$	Yn_t - Yn_c, BCK_t - BCK_c	–	$0.3 \times V_{DD}$	–	mV
AC differential output low measurement level (for output slew rate)	$V_{OLDiff(AC)}$		–	$-0.3 \times V_{DD}$	–	mV

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of DDR4 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. See the JEDEC RCD01 specification for complete operating electrical characteristics. Registering clock driver parametric values are specified for device default control word settings, unless otherwise stated. The RCOA control word setting does not affect parametric values.



## SPD EEPROM Operating Conditions

For the latest SPD data, refer to Micron's SPD page: [micron.com/spd](http://micron.com/spd).

**Table 16: SPD EEPROM DC Operating Conditions**

Parameter/Condition	Symbol	Min	Nom	Max	Units
Supply voltage	$V_{DDSPD}$	–	2.5	–	V
Input low voltage: logic 0; all inputs	$V_{IL}$	–0.5	–	$V_{DDSPD} \times 0.3$	V
Input high voltage: logic 1; all inputs	$V_{IH}$	$V_{DDSPD} \times 0.7$	–	$V_{DDSPD} + 0.5$	V
Output low voltage: 3mA sink current $V_{DDSPD} > 2V$	$V_{OL}$	–	–	0.4	V
Input leakage current: (SCL, SDA) $V_{IN} = V_{DDSPD}$ or $V_{SSSPD}$	$I_{LI}$	–	–	$\pm 5$	$\mu A$
Output leakage current: $V_{OUT} = V_{DDSPD}$ or $V_{SSSPD}$ , SDA in High-Z	$I_{LO}$	–	–	$\pm 5$	$\mu A$

- Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.
  2. All voltages referenced to  $V_{DDSPD}$ .

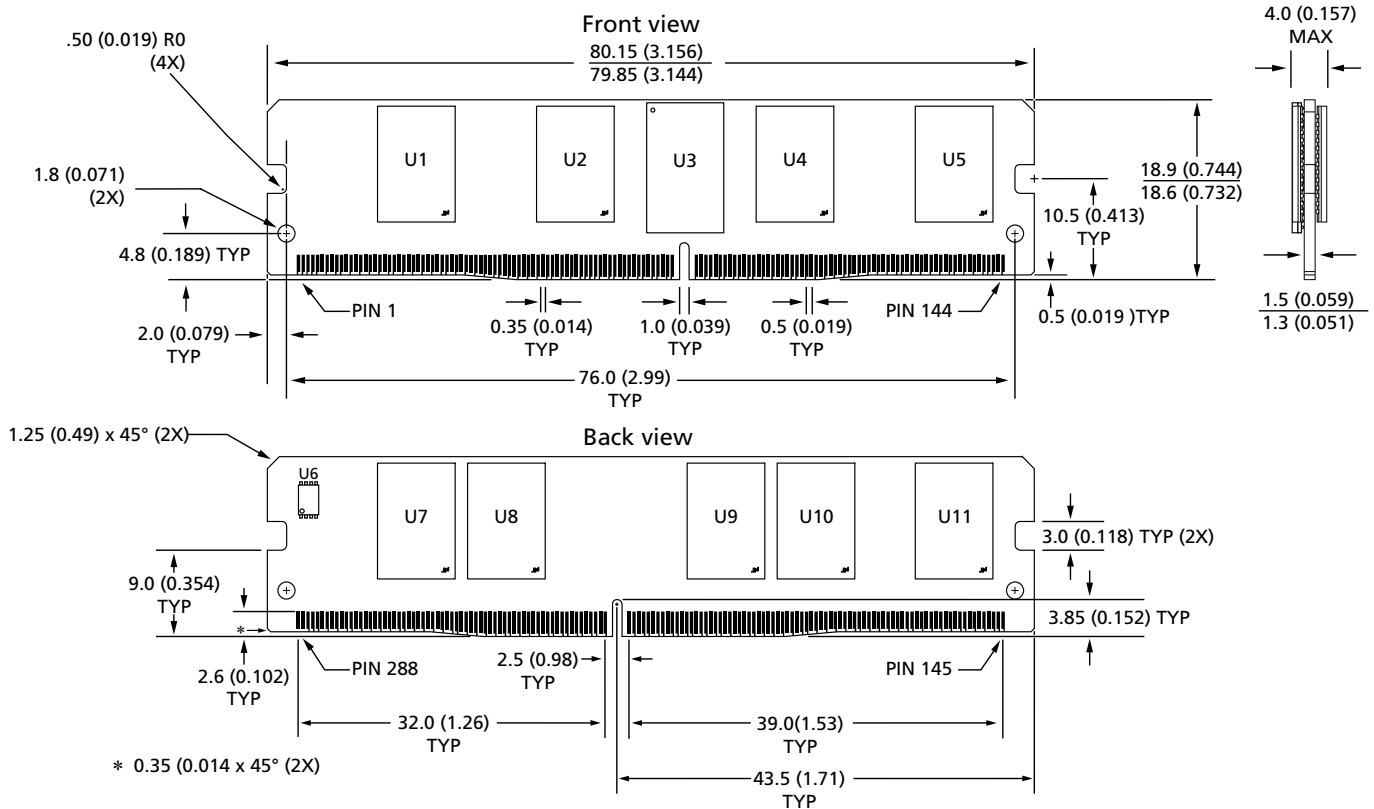
**Table 17: SPD EEPROM AC Operating Conditions**

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	$t_{SCL}$	10	1000	kHz
Clock pulse width HIGH time	$t_{HIGH}$	260	–	ns
Clock pulse width LOW time	$t_{LOW}$	500	–	ns
Detect clock LOW timeout	$t_{TIMEOUT}$	25	35	ms
SDA rise time	$t_R$	–	120	ns
SDA fall time	$t_F$	–	120	ns
Data-in setup time	$t_{SU:DAT}$	50	–	ns
Data-in hold time	$t_{HD:DI}$	0	–	ns
Data out hold time	$t_{HD:DAT}$	0	350	ns
Start condition setup time	$t_{SU:STA}$	260	–	ns
Start condition hold time	$t_{HD:STA}$	260	–	ns
Stop condition setup time	$t_{SU:STO}$	260	–	ns
Time the bus must be free before a new transition can start	$t_{BUF}$	500	–	ns
Write time	$t_W$	–	5	ms
Warm power cycle time off	$t_{POFF}$	1	–	ms
Time from power on to first command	$t_{INIT}$	10	–	ms

- Note:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

## Module Dimensions

**Figure 3: 288-Pin DDR4 VLP MiniRDIMM**



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.  
 2. The dimensional diagram is for reference only.

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